Smart High-Side Power Switch
Two Channels: 2 x 30mΩ
Current Sense

Product Summary

Operating Voltage	$V_{bb(on)}$	5.0...34V	
Active channels:		one	two parallel
On-state Resistance	R_{ON}	30mΩ	15mΩ
Load Current (ISO)	$I_{L(ISO)}$	12A	24A
Current Limitation	$I_{L(SCr)}$	24A	24A

Package

P-DSO-20-12 (Power SO 20)

General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input, diagnostic feedback and proportional load current sense monolithically integrated in Smart SIPMOS® technology.
- Providing embedded protective functions

Applications

- µC compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive, inductive and capacitve loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

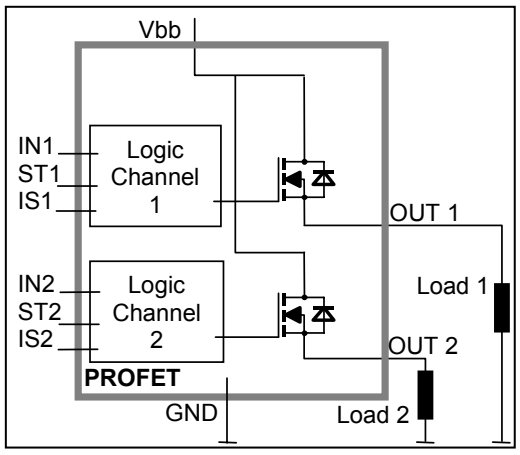
- CMOS compatible input
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Fast demagnetization of inductive loads
- Logic ground independent from load ground

Protection Functions

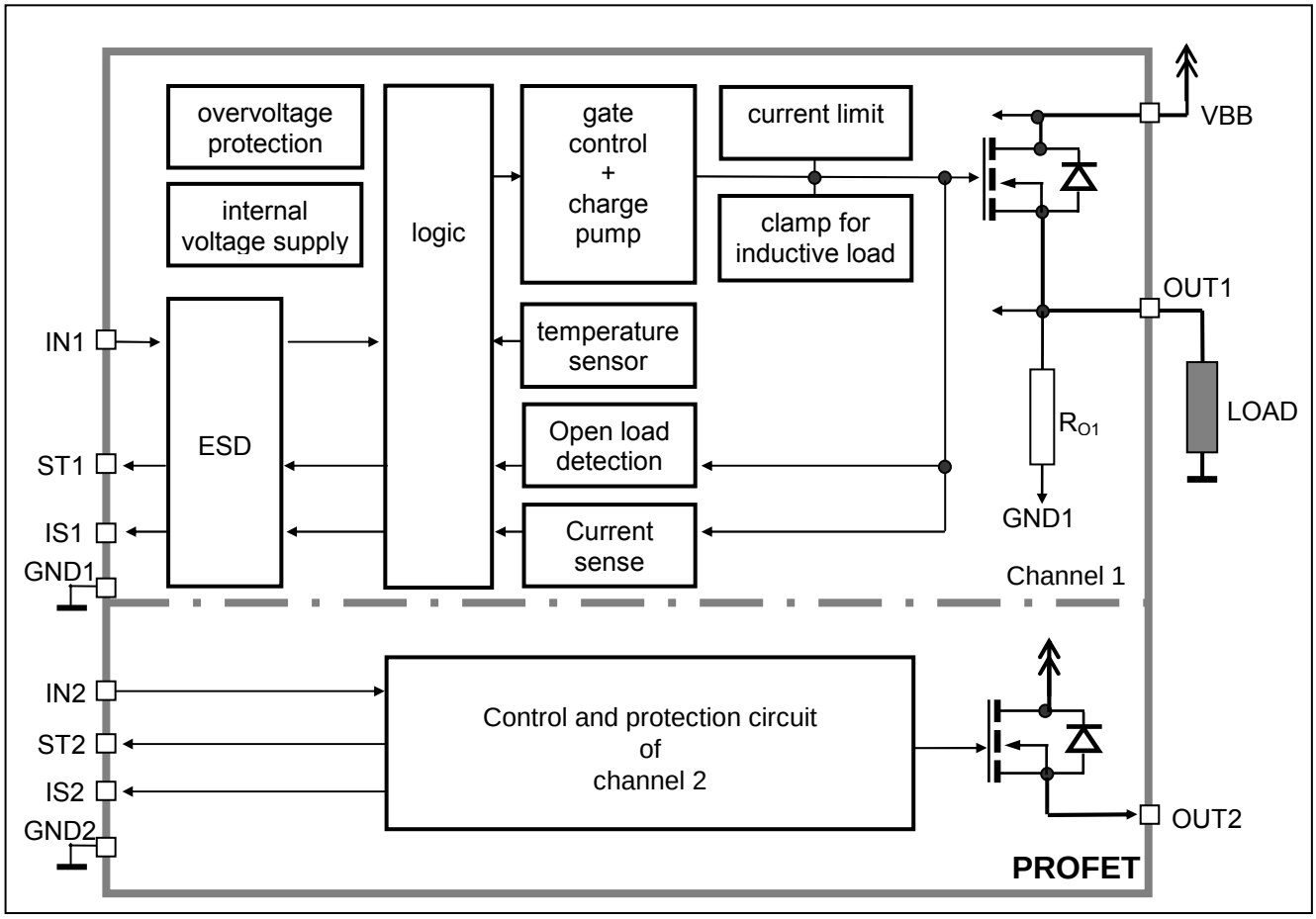
- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Proportinal load current sense
- Diagnostic feedback with open drain output
- Open load detection in OFF-state with external resistor
- Feedback of thermal shutdown in ON-state



Functional diagram

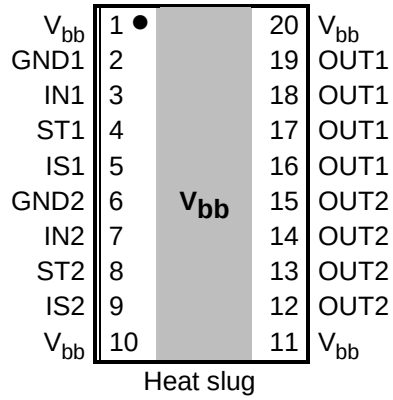


Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12,	V_{bb}	**Positive power supply voltage**. For high current applications the heat slug should be used as Vbb connection.
3	IN1	**Input 1,2**, activates channel 1,2 in case of logic high signal
7	IN2	
16,17, 18,19	OUT1	**Output 1,2**, protected high-side power output of channel 1,2. All pins of each output have to be connected in parallel for operation according ths spec (e.g. k_{ilis}). Design the wiring for the max. short circuit current
12,13, 14,15	OUT2	
4	ST1	**Diagnostic feedback 1,2** of channel 1,2 open drain, invers to input level
8	ST2	
2	GND1	**Ground 1,2** of chip channel 1,2
6	GND2	
5	IS1	**Sense current output 1,2;** proportional to the load current, zero in the case of current limitation of the load current
9	IS2	
Heatslug	V_{bb}	**Positiv powersupply voltage.** Good way to design a very low thermal resistance.

Pin configuration

(top view)



Maximum Ratings at T_j = 25°C unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 5)	V_{bb}	43	V
Supply voltage for full short circuit protection $T_{j,start}$ = -40 ...+150°C	V_{bb}	34	V
Load current (Short-circuit current, see page 5)	I_L	self-limited	A
Load dump protection[1] $V_{LoadDump} = V_A + V_s$, V_A = 13.5 V R_I[2] = 2 Ω, t_d = 200 ms; IN = low or high, each channel loaded with R_L = 1.0 Ω,	$V_{Load\,dump}$[3]	60	V
Operating temperature range Storage temperature range	T_j T_{stg}	-40 ...+150 -55 ...+150	°C
Power dissipation (DC)[4] T_a = 25°C: (all channels active) T_a = 85°C:	P_{tot}	3.8 2.0	W
Maximal switchable inductance, single pulse V_{bb} = 12V, $T_{j,start}$ = 150°C[4], I_L = 4 A, E_{AS} = 1.13J, 0 Ω one channel: I_L = 12 A, E_{AS} = 430mJ, 0 Ω one channel: I_L = 24 A, E_{AS} = 800mJ, 0 Ω two parallel channels: see diagrams on page 10	Z_L	 100 4.4 2.0	mH
Electrostatic discharge capability (ESD) IN: (Human Body Model) ST, IS: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 R=1.5kΩ; C=100pF	V_{ESD}	1.0 4.0 8.0	kV
Input voltage (DC)	V_{IN}	-10 ... +16	V
Current through input pin (DC) Current through status pin (DC) Current through current sense pin (DC) see internal circuit diagram page 9	I_{IN} I_{ST} I_{IS}	±2.0 ±5.0 ±14	mA

1) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins a 150Ω resistor for the GND connection is recommended.

2) R_I = internal resistance of the load dump test pulse generator

3) $V_{Load\,dump}$ is set up without the DUT connected to the generator per ISO 7637-1 and DIN 40839

4) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for V_{bb} connection. PCB is vertical without blown air.

Thermal Characteristics

Parameter and Conditions		Symbol	Values			Unit
			min	typ	max	
Thermal resistance						
junction -case	each channel:	R_{thjs}	--	--	1	K/W
junction - ambient[4]	one channel active:	R_{thja}	--	37	--	
	all channels active:		--	30	--	

Electrical Characteristics

Parameter and Conditions, each of the two channels at T_j = -40...+150°C, V_{bb} = 12 V unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Load Switching Capabilities and Characteristics					
On-state resistance (V_{bb} to OUT); I_L = 5 A					
each channel, T_j = 25°C:	R_{ON}	--	27	30	mΩ
T_j = 150°C:			54	60	
two parallel channels, T_j = 25°C:			14	15	
Output voltage drop limitation at small load currents, see page 14					
I_L = 0.5 A T_j =-40...+150°C:	$V_{ON(NL)}$	--	50	--	mV
Nominal load current, ISO Norm					
one channel active:	$I_{L(NOM)}$	11	12	--	A
two parallel channels active:		22	24		
ISO 10483-1, 6.7: *Von* =0.5V T_C = 85°C					
Output current while GND disconnected or pulled up[5]; V_{bb} = 30 V, V_{IN} = 0, see diagram page 10	$I_{L(GNDhigh)}$	--	--	8	mA
Turn-on time[6] IN ⌐‾ to 90% V_{OUT}:	t_{on}	25	70	150	µs
Turn-off time IN ‾⌐ to 10% V_{OUT}:	t_{off}	25	80	200	
R_L = 12 Ω					
Slew rate on[6] 10 to 30% V_{OUT}, R_L = 12 Ω:	dV/dt_{on}	0.1	--	1	V/µs
Slew rate off[6] 70 to 40% V_{OUT}, R_L = 12 Ω:	$-dV/dt_{off}$	0.1	--	1	V/µs

5) not subject to production test, specified by design

6) See timing diagram on page 11.

Parameter and Conditions, each of the two channels at T_j = -40...+150°C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	
Operating Parameters					
Operating voltage[7]	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown	$V_{bb(under)}$	3.2	--	5.0	V
Undervoltage restart T_j =-40...+25°C: T_j =+150°C:	$V_{bb(u\ rst)}$	--	4.5	5.5 6.0	V
Undervoltage restart of charge pump see diagram page 13 T_j =-40...+25°C: T_j =150°C:	$V_{bb(ucp)}$	-- --	4.7 --	6.5 7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.5	--	V
Overvoltage shutdown	$V_{bb(over)}$	34	--	43	V
Overvoltage restart	$V_{bb(o\ rst)}$	33	--	--	V
Overvoltage hysteresis	$\Delta V_{bb(over)}$	--	1	--	V
Overvoltage protection[8] T_j =-40: I_{bb}=40 mA T_j =+25...+150°C:	$V_{bb(AZ)}$	41 43	-- 47	-- 52	V
Standby current[9] T_j =-40°C...25°C: V_{IN} = 0 T_j =150°C:	$I_{bb(off)}$	-- --	8 24	30 50	µA
Leakage output current (included in $I_{bb(off)}$); V_{IN} = 0	$I_{L(off)}$	--	--	20	µA
Operating current [10], V_{IN} = 5V, $I_{GND} = I_{GND1} + I_{GND2}$, one channel on: two channels on:	I_{GND}	-- --	1.2 2.4	3 6	mA
Protection Functions[11]					
Current limit, (see timing diagrams, page 12) T_j =-40°C: T_j =25°C: T_j =+150°C:	$I_{L(lim)}$	48 40 31	56 50 37	65 58 45	A
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 12)	$I_{L(SCr)}$	-- --	24 24	-- --	A
Initial short circuit shutdown time $T_{j,start}$ =25°C: (see timing diagrams on page 12)	$t_{off(SC)}$	--	4.0	--	ms

7) At supply voltage increase up to V_{bb}= 4.7 V typ without charge pump, $V_{OUT} \approx V_{bb}$ - 2 V

8) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150 Ω resistor in the GND connection is recommended). See also $V_{ON(CL)}$ in table of protection functions and circuit diagram page 9.

9) Measured with load; for the whole device; all channels off

10) Add I_{ST}, if I_{ST} > 0

11) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Parameter and Conditions, each of the two channels at T_j = -40...+150°C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	
Output clamp (inductive load switch off)[12] at $V_{ON(CL)} = V_{bb} - V_{OUT}$, I_L= 40 mA T_j =-40°C:	$V_{ON(CL)}$	41	--	--	V
T_j =25°C...150°C:		43	47	52	
Thermal overload trip temperature	T_{jt}	150	--	--	°C
Thermal hysteresis	ΔT_{jt}	--	10	--	K
Reverse Battery					
Reverse battery voltage [13]	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ($V_{out} > V_{bb}$) I_L = - 4.0 A, T_j = +150°C	$-V_{ON}$	--	600	--	mV
Diagnostic Characteristics					
Current sense ratio[14], static on-condition, V_{IS} = 0...5 V, $V_{bb(on)}$ = 6.5[15]...27V, $k_{ILIS} = I_L / I_{IS}$ T_j = -40°C, I_L = 5 A:	k_{ILIS}	4350	4800	5800	
T_j= -40°C, I_L= 0.5 A:		3100	4800	7800	
T_j= 25...+150°C, I_L= 5 A:		4350	4800	5350	
T_j= 25...+150°C, I_L = 0.5 A:		3800	4800	6300	
Current sense output voltage limitation T_j = -40 ...+150°C I_{IS} = 0, I_L = 5 A:	$V_{IS(lim)}$	5.4	6.1	6.9	V
Current sense leakage/offset current T_j = -40 ...+150°C V_{IN}=0, V_{IS} = 0, I_L = 0:	$I_{IS(LL)}$	0	--	1	µA
V_{IN}=5 V, V_{IS} = 0, I_L = 0:	$I_{IS(LH)}$	0	--	15	
V_{IN}=5 V, V_{IS} = 0, V_{OUT} = 0 (short circuit)	$I_{IS(SH)}$ [16]	0	--	10	
Current sense settling time to $I_{IS\ static}$±10% after positive input slope[16], I_L = 0 ⎍ 5 A	$t_{son(IS)}$	--	--	300	µs

12) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$

13) Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 9).

14) This range for the current sense ratio refers to all devices. The accuracy of the k_{ILIS} can be raised at least by a factor of two by matching the value of k_{ILIS} for every single device.
In the case of current limitation the sense current I_{IS} is zero and the diagnostic feedback potential V_{ST} is High. See figure 2c, page 12.

15) Valid if $V_{bb(u\ rst)}$ was exceeded before.

16) not subject to production test, specified by design

Parameter and Conditions, each of the two channels at T_j = -40...+150°C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values**			**Unit**
		min	typ	max	
Current sense settling time to 10% of I_{IS} static after negative input slope[17], I_L = 5 ⎺|_ 0 A	$t_{soff(IS)}$	--	30	100	µs
Current sense rise time (60% to 90%) after change of load current[17], I_L = 2.5 _|⎺ 5 A	$t_{slc(IS)}$	--	10	--	µs
Open load detection voltage[18] (off-condition)	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (pin 16,17,18,19 to 2 resp. 12,13,14,15 to 6), V_{OUT}=5 V	R_O	5	15	40	kΩ

Input and Status Feedback[19]

Input resistance (see circuit page 9)	R_I	3.0	4.5	7.0	kΩ
Input turn-on threshold voltage	$V_{IN(T+)}$	--	--	3.5	V
Input turn-off threshold voltage	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current V_{IN} = 0.4 V:	$I_{IN(off)}$	1	--	50	µA
On state input current V_{IN} = 5 V:	$I_{IN(on)}$	20	50	90	µA
Delay time for status with open load after Input neg. slope (see diagram page 14)	$t_{d(ST\ OL3)}$	--	400	--	µs
Status delay after positive input slope[17]	$t_{don(ST)}$	--	13	--	µs
Status delay after negative input slope[17]	$t_{doff(ST)}$	--	1	--	µs
Status output (open drain)					
Zener limit voltage T_j =-40...+150°C, I_{ST} = +1.6 mA:	$V_{ST(high)}$	5.4	6.1	6.9	V
ST low voltage T_j =-40...+25°C, I_{ST} = +1.6 mA:	$V_{ST(low)}$	--	--	0.4	
T_j = +150°C, I_{ST} = +1.6 mA:		--	--	0.7	
Status leakage current, V_{ST} = 5 V, T_j=25 ... +150°C:	$I_{ST(high)}$	--	--	2	µA

17) not subject to production test, specified by design

18) External pull up resistor required for open load detection in off state.

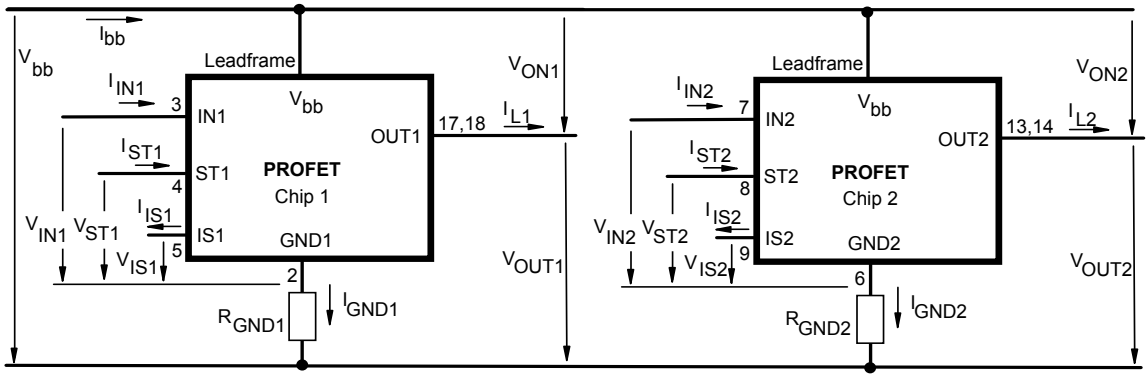
19) If ground resistors R_{GND} are used, add the voltage drop across these resistors.

Truth Table

	Input 1	Output 1	Status 1	Current Sense 1
	Input 2	Output 2	Status 2	Current Sense 2
	level	level	level	I_{IS}
Normal operation	L H	L H	H L	0 nominal
Current-limitation	L H	L H	H H	0 0
Short circuit to GND	L H	L L[20)]	H H	0 0
Over-temperature	L H	L L	H H	0 0
Short circuit to V_{bb}	L H	H H	L[21)] L	0 <nominal [22)]
Open load	L H	L[23)] H	H (L[24)]) L	0 0
Undervoltage	L H	L L	H L	0 0
Overvoltage	L H	L L	H L	0 0
Negative output voltage clamp	L	L	H	0

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal after the time delay shown in the diagrams (see fig 5. page 13)
Parallel switching of channel 1 and 2 is possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor. The current sense outputs IS1 and IS2 have to be connected with a single pull-down resistor.

Terms



Leadframe (V_{bb}) is connected to pin 1,10,11,20
External R_{GND} optional; two resistors R_{GND1}, R_{GND2} = 150 Ω or a single resistor R_{GND} = 75 Ω for reverse battery protection up to the max. operating voltage.

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20) The voltage drop over the power transistor is V_{bb}-V_{OUT} > 3V typ. Under this condition the sense current I_{IS} is zero

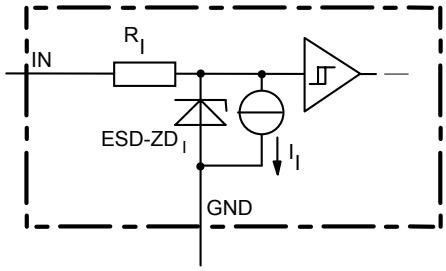
21) An external short of output to V_{bb}, in the off state, causes an internal current from output to ground. If R_{GND} is used, an offset voltage at the GND and ST pins will occur and the $V_{ST\ low}$ signal may be errorious.

22) Low ohmic short to V_{bb} may reduce the output current I_L and therefore also the sense current I_{IS}.

23) Power Transistor off, high impedance

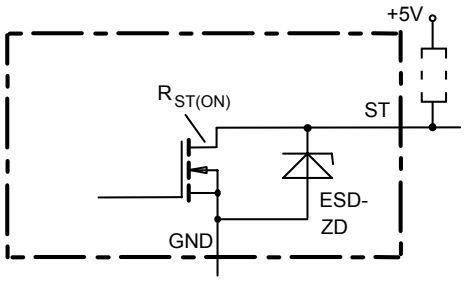
24) with external resistor between V_{BB} and OUT

Input circuit (ESD protection), IN1 or IN2



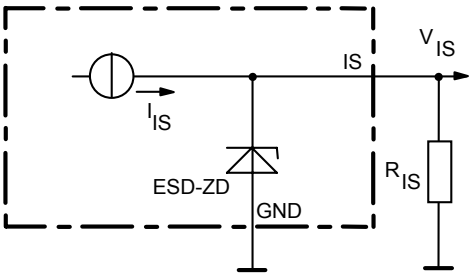
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Status output, ST1 or ST2



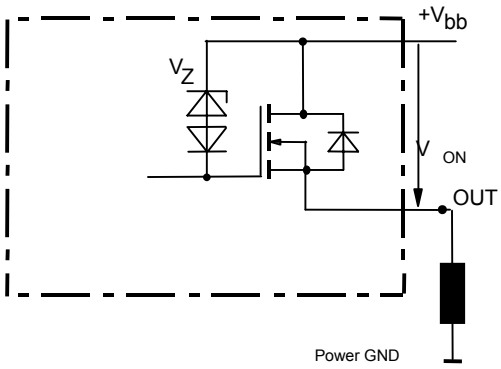
ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)}$ < 375 Ω at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Current sense output, IS1 or IS2



ESD-Zener diode: 6.1 V typ., max 14 mA;
R_{IS} = 1 kΩ nominal

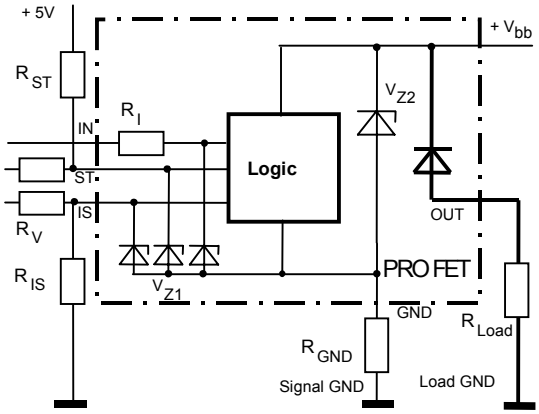
Inductive and overvoltage output clamp, OUT1 or OUT2



V_{ON} clamped to $V_{ON(CL)}$ = 47 V typ.

Overvoltage and reverse batt. Protection

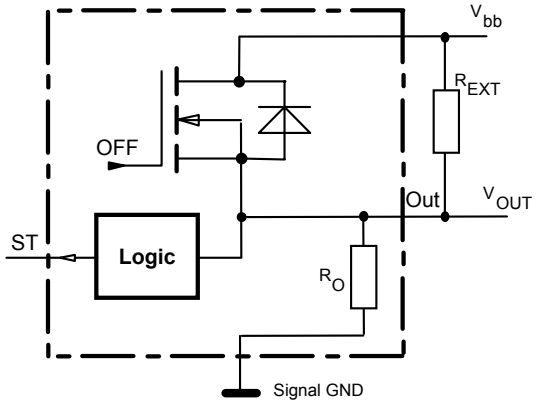
For each channel



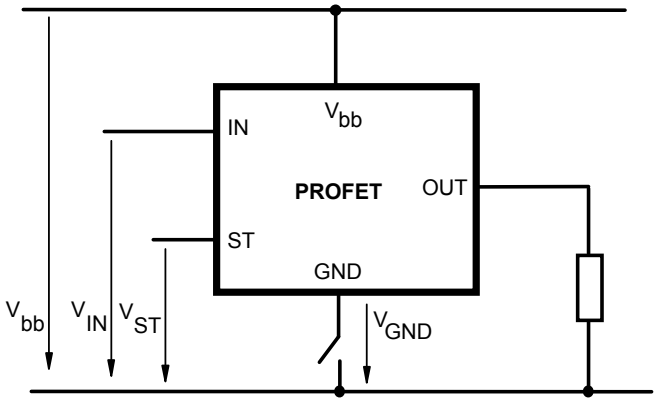
V_{Z1} = 6.1 V typ., V_{Z2} = 47 V typ., R_{GND} = 150 Ω,
R_{ST}=15kΩ, R_I=4.5kΩ typ., R_{IS}=1kΩ, R_V=15kΩ,
In case of reverse battery the current has to be limited by the load. Temperature protection is not active

Open-load detection OUT1 or OUT2

OFF-state diagnostic condition:
V_{OUT} > 3 V typ.; IN low



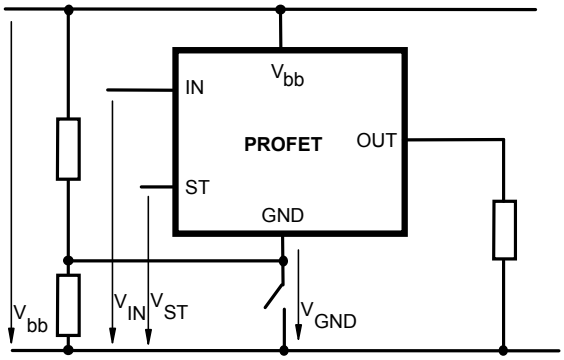
GND disconnect, each channel



Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$. Due to $V_{GND} > 0$, no V_{ST} = low signal available.

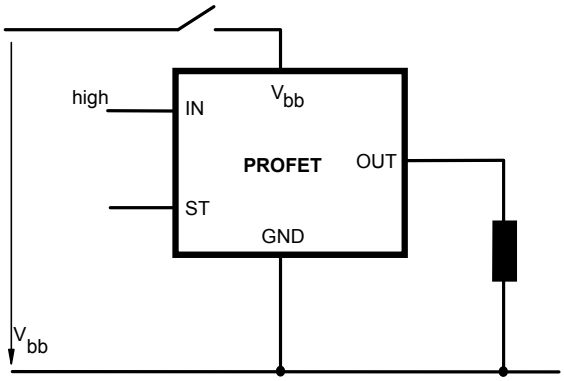
GND disconnect with GND pull up

each channel



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off Due to $V_{GND} > 0$, no V_{ST} = low signal available.

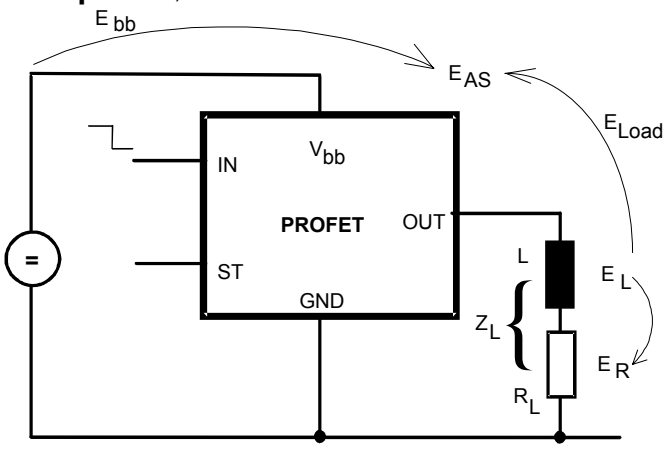
V_{bb} disconnect with energized inductive load, each channel



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 10) each switch is protected against loss of V_{bb}.

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation, each channel



Energy stored in load inductance:

$$E_L = {}^1/_2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

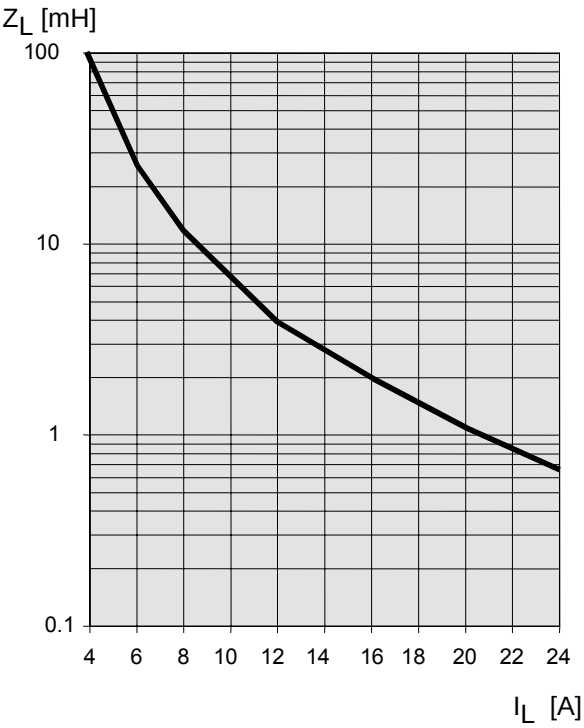
$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \cdot i_L(t)\, dt,$$

with an approximate solution for $R_L > 0\,\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L}\left(V_{bb} + |V_{OUT(CL)}|\right)\ ln\left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

Maximum allowable load inductance for a single switch off (one channel)[4)]

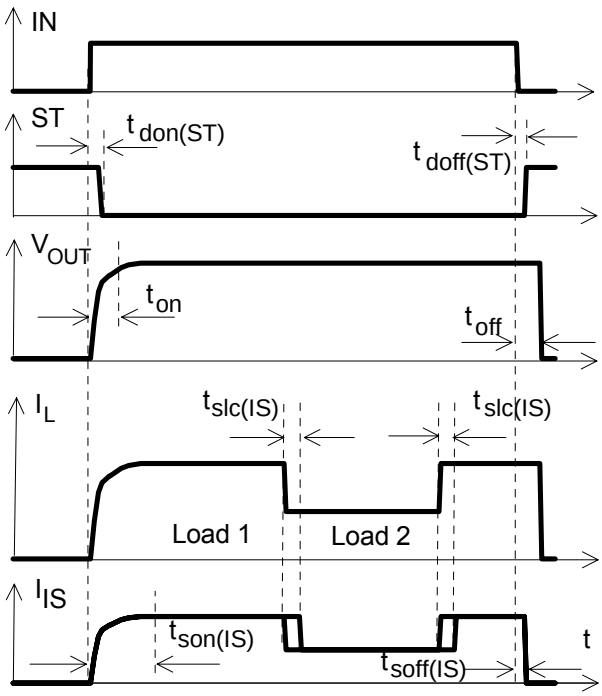
$L = f(I_L)$; $T_{j,start} = 150°C$, $V_{bb} = 12\,V$, $R_L = 0\,\Omega$



Timing diagrams

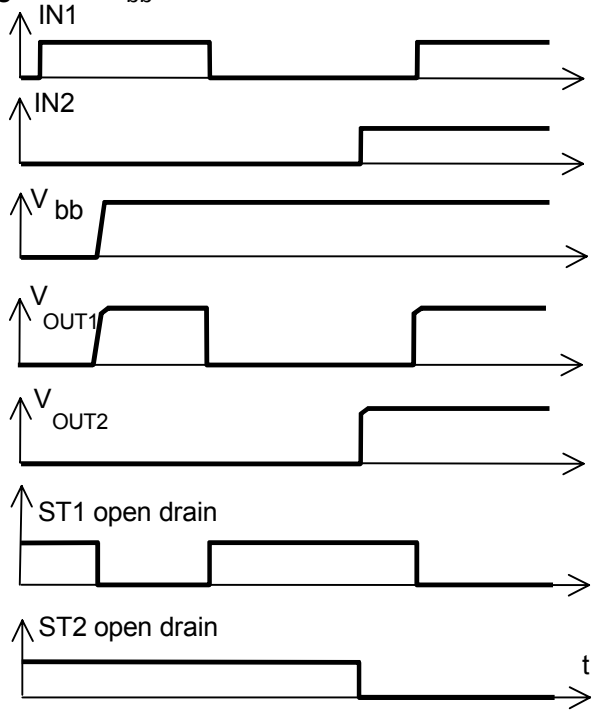
Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: Switching a resistive load, change of load current in on-condition:



The sense signal is not valid during settling time after turn or change of load current.

Figure 1b: V_{bb} turn on:



proper turn on under all conditions

Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

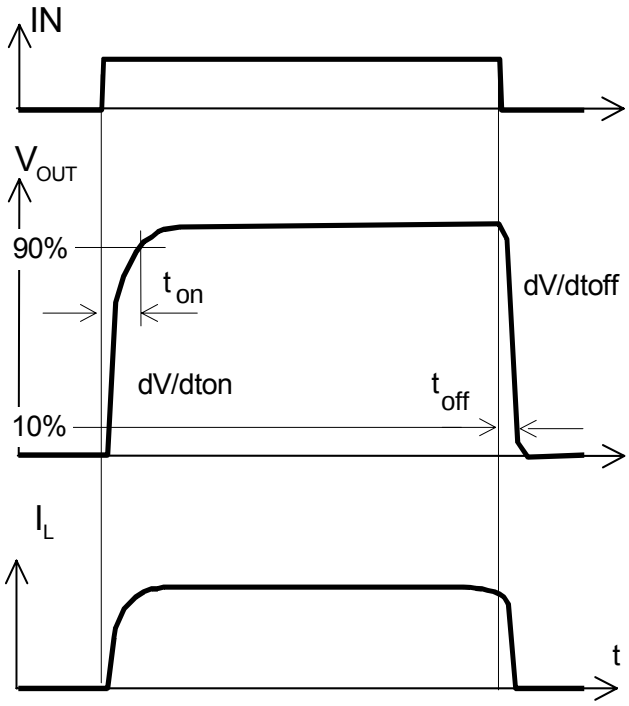
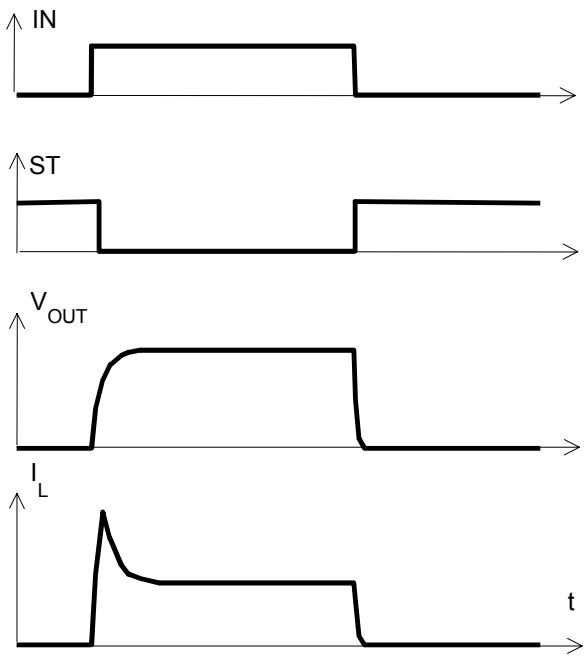


Figure 2b: Switching a lamp:



The initial peak current should be limited by the lamp and not by the current limit of the device.

Figure 2c: Switching a lamp with current limit:

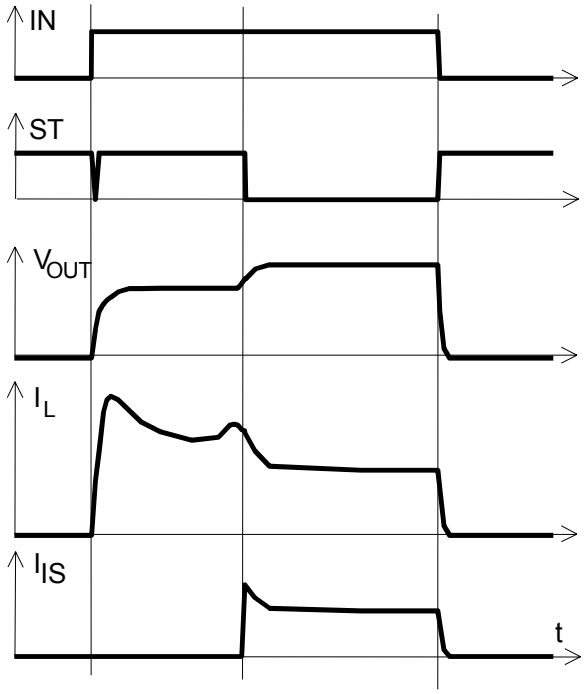
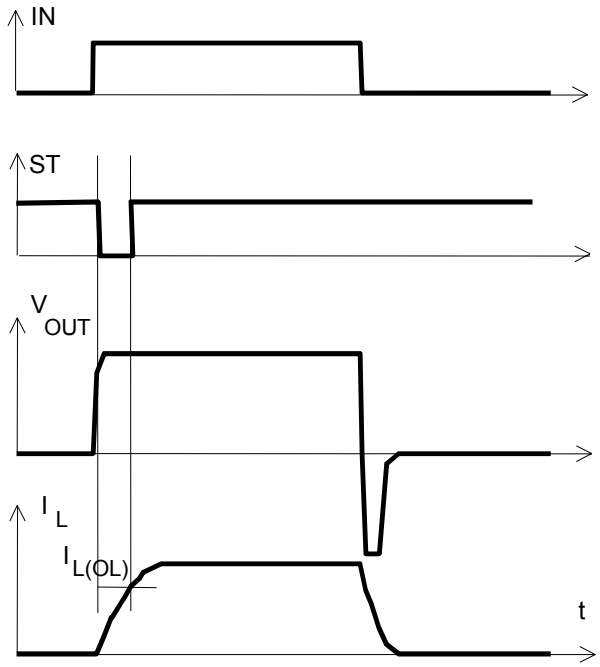
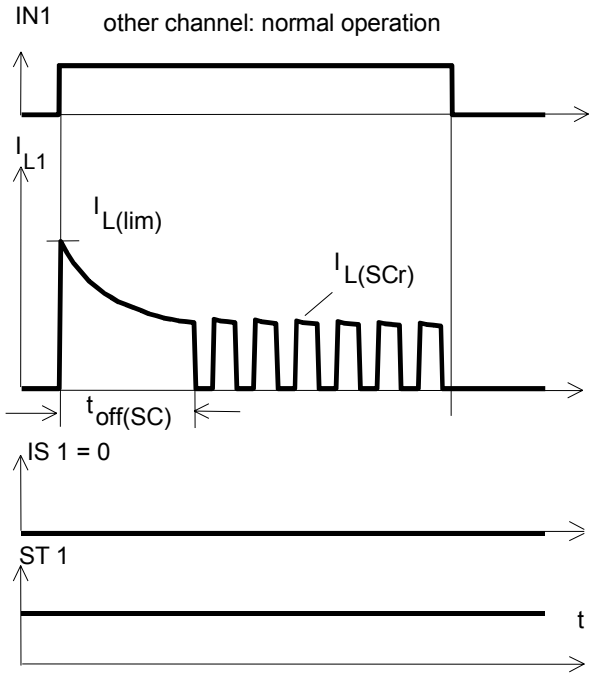


Figure 2d: Switching an inductive load



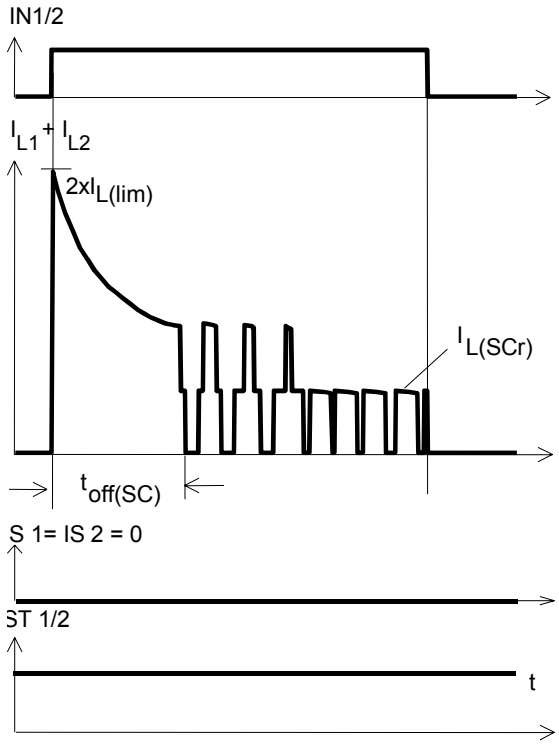
*) if the time constant of load is too large, open-load-status may occur

Figure 3a: Turn on into short circuit:
shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions

Figure 3b: Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)



ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature:
Reset if $T_j < T_{jt}$

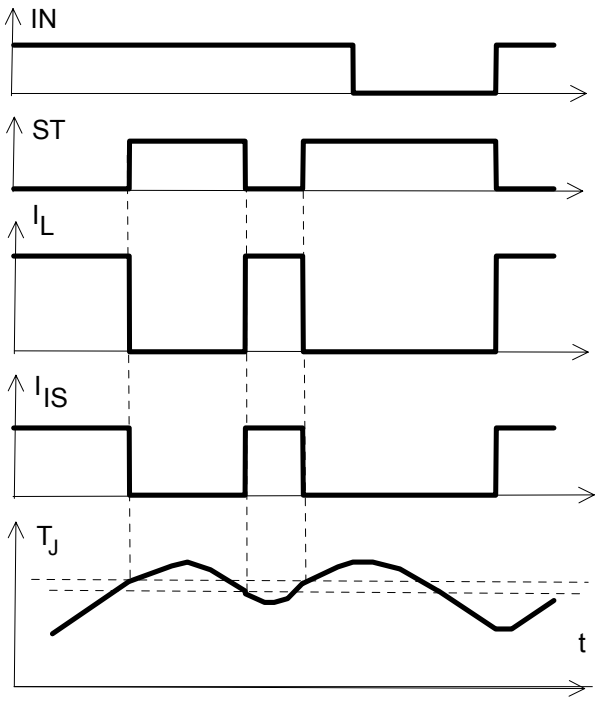


Figure 5a: Open load: detection (with R_{EXT}), turn on/off to open load

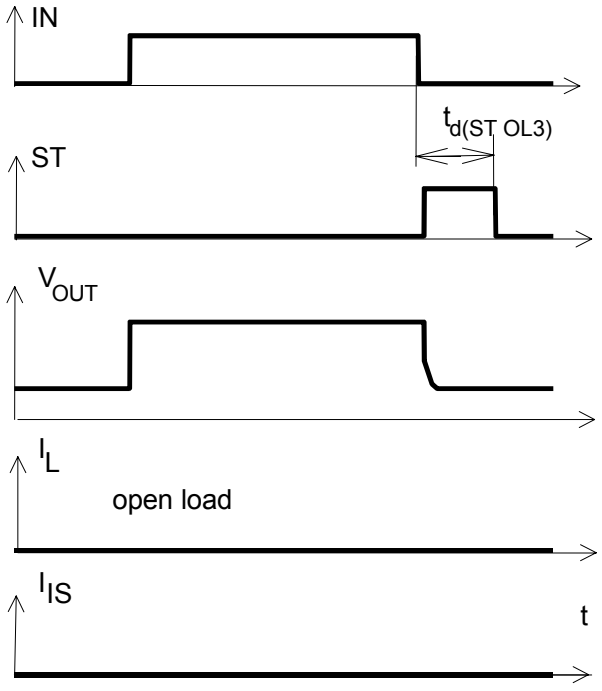


Figure 6a: Undervoltage:

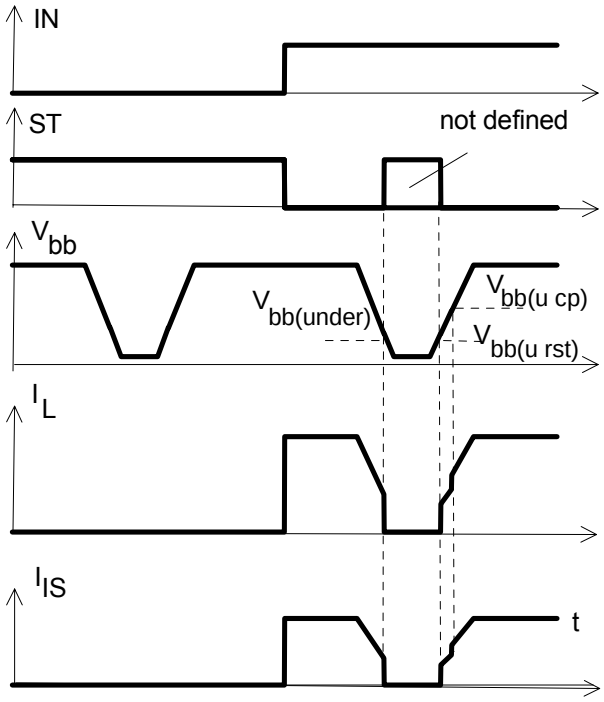
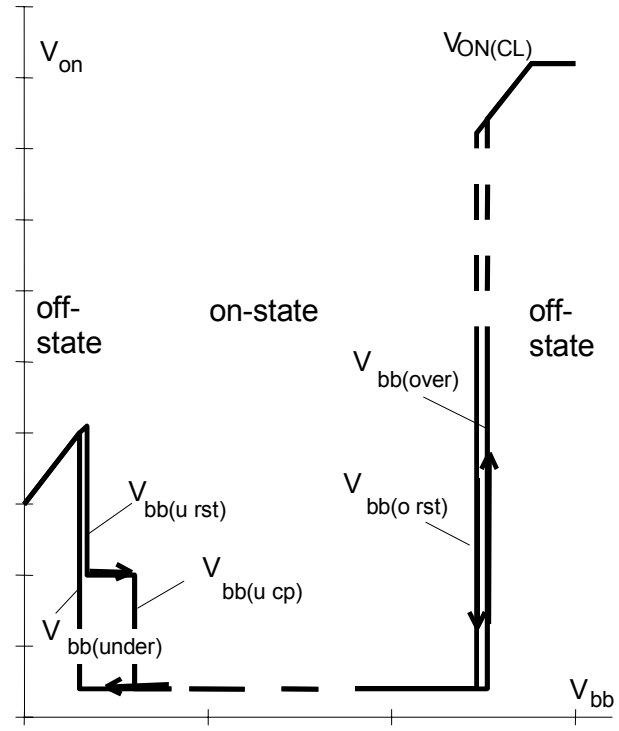


Figure 6b: Undervoltage restart of charge pump



charge pump starts at $V_{bb(ucp)}$ =4.7 V typ.

Figure 7a: Overvoltage:

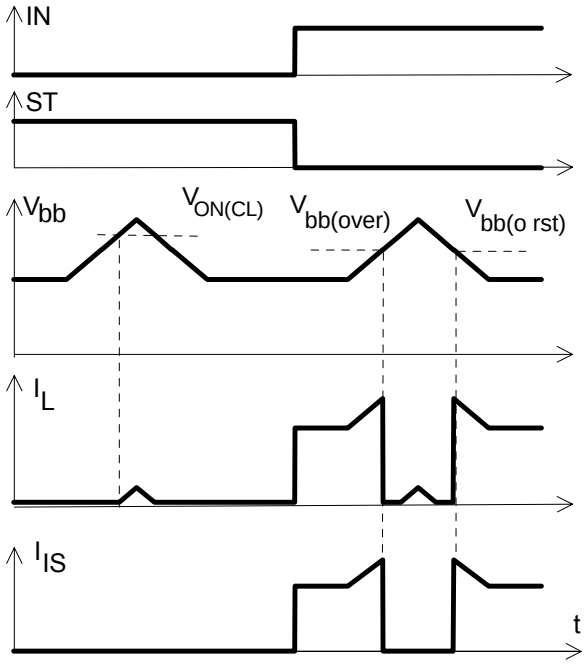


Figure 8a: Current sense versus load current[25]::

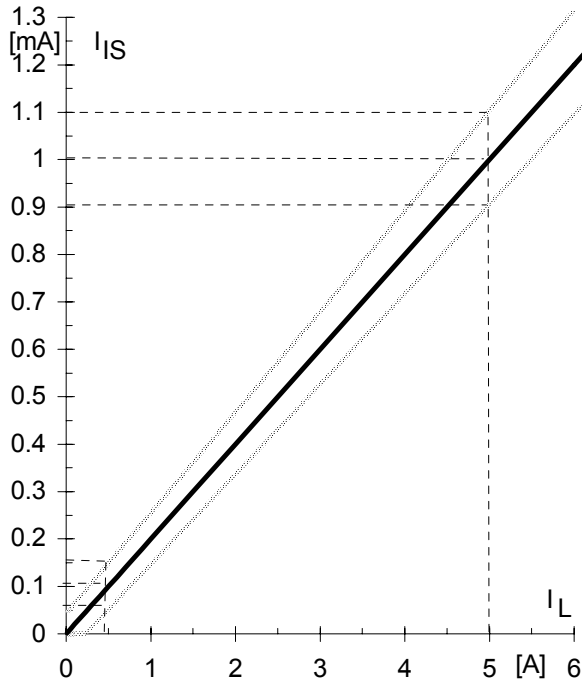


Figure 8b: Current sense ratio:

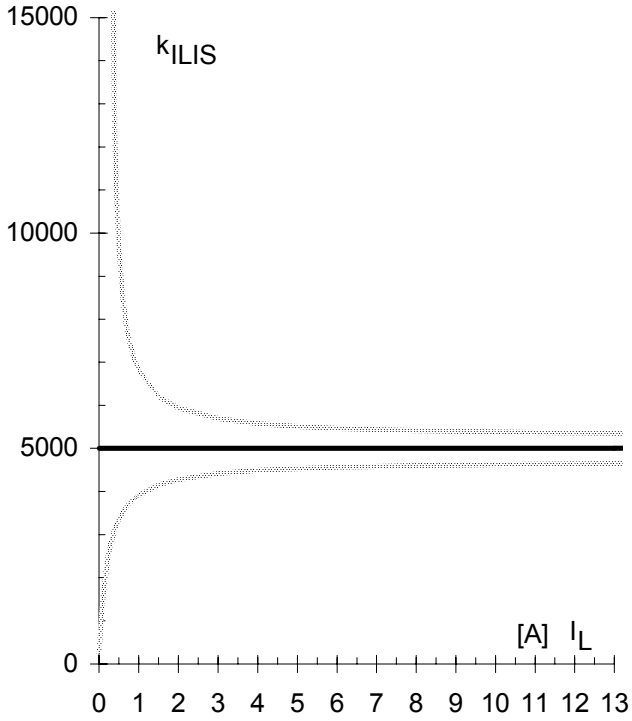
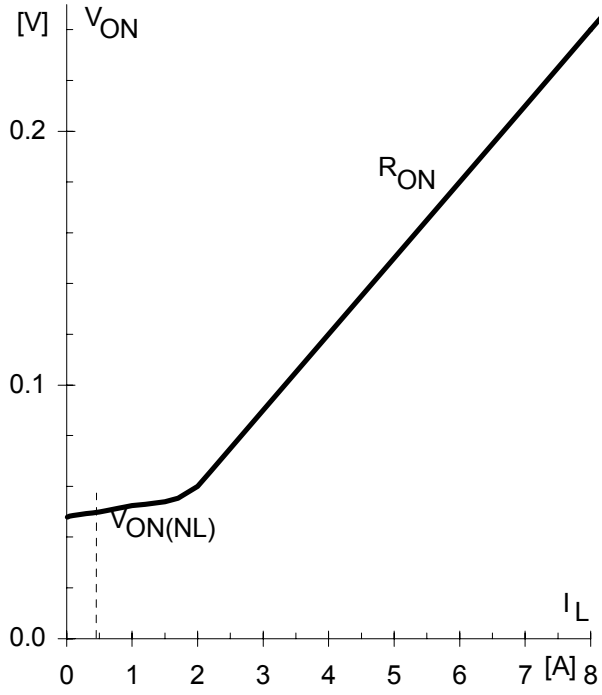


Figure 9a: Output voltage drop versus load current:



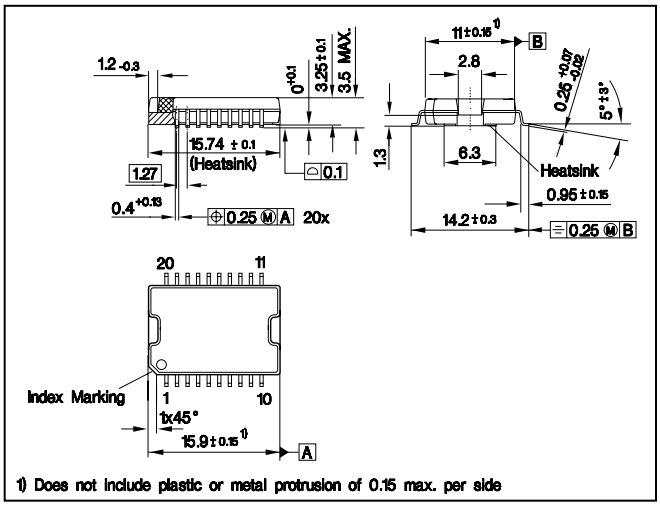
[25] This range for the current sense ratio refers to all devices. The accuracy of the k_{ILIS} can be raised at least by a factor of two by matching the value of k_{ILIS} for every single device.

Package and Ordering Code

Standard: P-DSO-20-12 (Power SO 20)

Sales Code	BTS 840
Ordering Code	Q67060-S7013

All dimensions in millimetres



Published by
Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81669 München
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