FAIRCHILD SEMICONDUCTOR™

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CD4066BC
Quad Bilateral Switch

General Description

The CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation 80Ω
- Matched "ON" resistance $\Delta R_{ON} = 5\Omega$ (typ.) over 15V signal input
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio 65 dB (typ.) @ $f_{is} = 10$ kHz, $R_L = 10$ kΩ
- Control Line Biasing:
  Switch On (Logic 1), $V_C = V_{DD}$
  Switch Off (Logic 0), $V_C = V_{SS}$
- High degree linearity 0.1% distortion (typ.)
  High degree linearity @ $f_{is} = 1$ kHz, $V_{is} = 5V_{p-p}$,
  High degree linearity $V_{DD}-V_{SS} = 10V$, $R_L = 10$ kΩ
- Extremely low "OFF" switch leakage: 0.1 nA (typ.) @ $V_{DD}-V_{SS} = 10V$, $T_A = 25°C$
- Extremely high control input impedance $10^{12}\Omega$(typ.)
- Low crosstalk between switches −50 dB (typ.) @ $f_{is} = 0.9$ MHz, $R_L = 1$ kΩ
- Frequency response, switch "ON" 40 MHz (typ.)

Applications

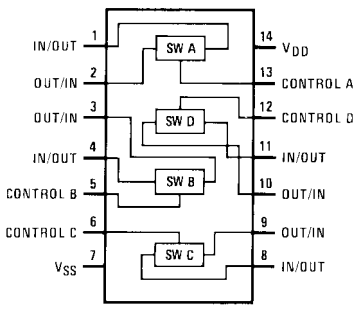
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Ordering Code:

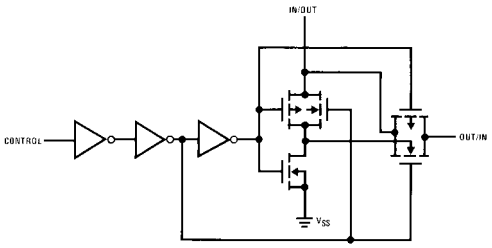
Order Number	Package Number	Package Description
CD4066BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4066BCSJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4066BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Schematic Diagram



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Absolute Maximum Ratings

(Note 1)
(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{CC}+0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	
		V_{DD} = 10V		0.5		0.01	0.5		15	µA
		V_{DD} = 15V		1.0		0.01	1.0		30	
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ to (V_{DD} − V_{SS}/2)								
		V_C = V_{DD}, V_{SS} to V_{DD}								
		V_{DD} = 5V		800		270	1050		1300	
		V_{DD} = 10V		310		120	400		550	Ω
		V_{DD} = 15V		200		80	240		320	
ΔR_{ON}	Δ"ON" Resistance Between	R_L = 10 kΩ to (V_{DD} − V_{SS}/2)								
	Any 2 of 4 Switches	V_{CC} = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
		V_{DD} = 10V				10				Ω
		V_{DD} = 15V				5				
I_{IS}	Input or Output Leakage	V_C = 0		±50		±0.1	±50		±500	nA
	Switch "OFF"									
CONTROL INPUTS										
V_{ILC}	LOW Level Input	V_{IS} = V_{SS} and V_{DD}								
	Voltage	V_{OS} = V_{DD} and V_{SS}								
		I_{IS} = ± 10µA								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	
V_{IHC}	HIGH Level Input	V_{DD} = 5V	3.5		3.5	2.75		3.5		
	Voltage	V_{DD} = 10V (Note 7)	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		
I_{IN}	Input Current	V_{DD}−V_{SS} = 15V		−0.1		-10^{-5}	−0.1		−0.1	µA
		V_{DD}≥V_{IS}≥V_{SS}		0.1		10^{-5}	0.1		0.1	
		V_{DD}≥V_C≥V_{SS}								

AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal	$V_C = V_{DD}$, $C_L = 50$ pF, (Figure 1)				
	Input to Signal Output	$R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time	$R_L = 1.0$ kΩ, $C_L = 50$ pF, (Figure 2, Figure 3)				
	Control Input to Signal	$V_{DD} = 5V$			125	ns
	Output High Impedance to	$V_{DD} = 10V$			60	ns
	Logical Level	$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time	$R_L = 1.0$ kΩ, $C_L = 50$ pF, (Figure 2, Figure 3)				
	Control Input to Signal	$V_{DD} = 5V$			125	ns
	Output Logical Level to	$V_{DD} = 10V$			60	ns
	High Impedance	$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$		0.1		%
		$R_L = 10$ kΩ, $V_{IS} = 5V_{p-p}$, f= 1 kHz, (Figure 4)				
	Frequency Response-Switch	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$,		40		MHz
	"ON" (Frequency at −3 dB)	$R_L = 1$ kΩ, $V_{IS} = 5V_{p-p}$,				
		$20 \log_{10} V_{OS}/V_{OS}$ (1 kHz)−dB,				
		(Figure 4)				
	Feedthrough — Switch "OFF"	$V_{DD} = 5.0V$, $V_{CC} = V_{SS} = -5.0V$,		1.25		
	(Frequency at −50 dB)	$R_L = 1$ kΩ, $V_{IS} = 5.0V_{p-p}$, $20 \log_{10}$,				
		$V_{OS}/V_{IS} = -50$ dB, (Figure 4)				
	Crosstalk Between Any Two	$V_{DD} = V_{C(A)} = 5.0V$; $V_{SS} = V_{C(B)} = 5.0V$,		0.9		MHz
	Switches (Frequency at −50 dB)	R_L1 kΩ, $V_{IS(A)} = 5.0$ V_{p-p}, $20 \log_{10}$,				
		$V_{OS(B)}/V_{IS(A)} = -50$ dB (Figure 5)				
	Crosstalk; Control Input to	$V_{DD} = 10V$, $R_L = 10$ kΩ, $R_{IN} = 1.0$ kΩ,		150		mV_{p-p}
	Signal Output	$V_{CC} = 10V$ Square Wave, $C_L = 50$ pF				
		(Figure 6)				
	Maximum Control Input	$R_L = 1.0$ kΩ, $C_L = 50$ pF, (Figure 7)				
		$V_{OS(f)} = ½ V_{OS}$(1.0 kHz)				
		$V_{DD} = 5.0V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{IS}	Signal Input Capacitance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8.0		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: These devices should not be connected to circuits with the power "ON".

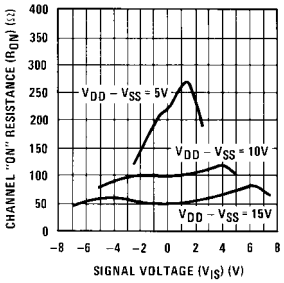
Note 5: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 6: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

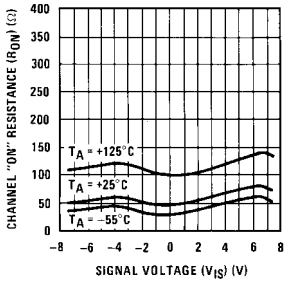
Note 7: Conditions for V_{IHC}: a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OL} = standard B series I_{OL}.

Typical Performance Characteristics

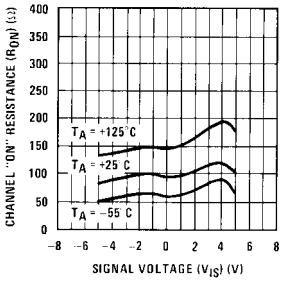
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



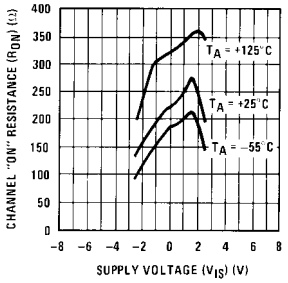
"ON" Resistance as a Function of Temperature for $V_{DD}–V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD}–V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD}–V_{SS} = 5V$



Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

AC Test Circuits and Switching Time Waveforms

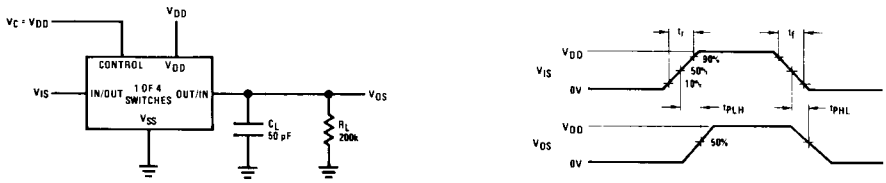


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

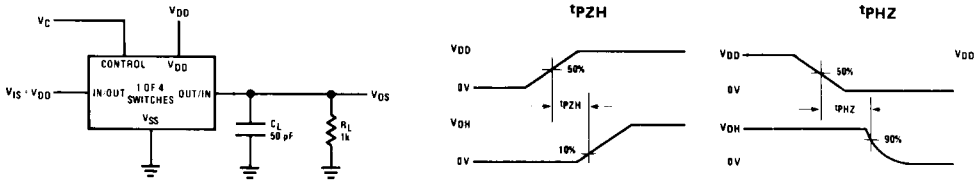


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

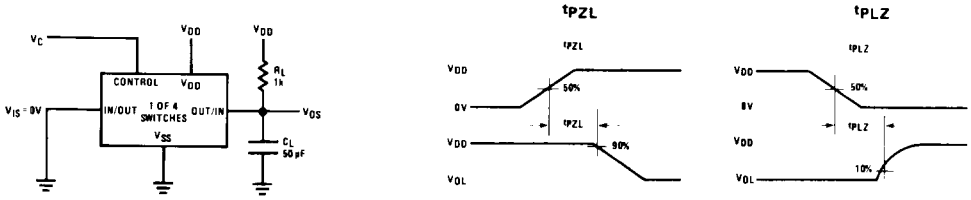
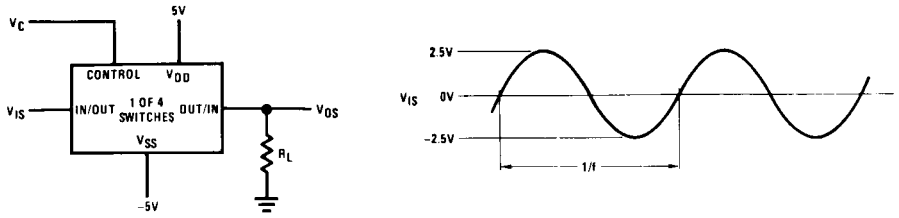


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$ for distortion and frequency response tests

$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

AC Test Circuits and Switching Time Waveforms (Continued)

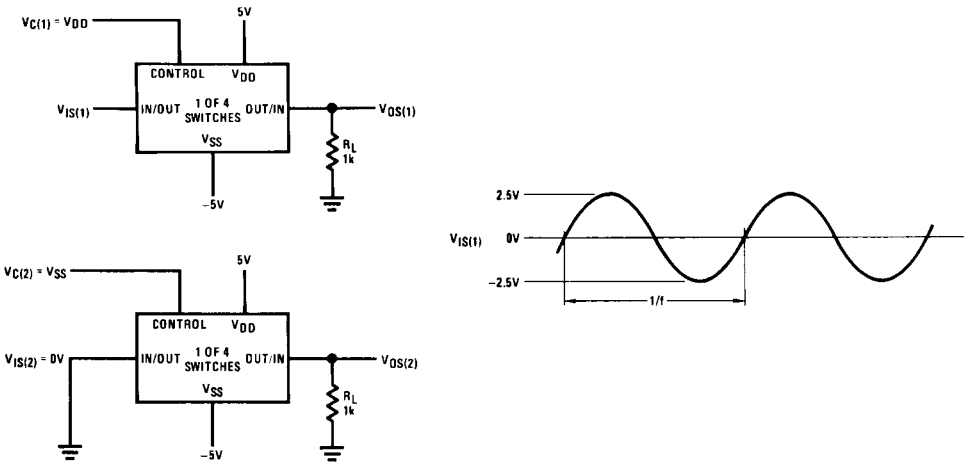


FIGURE 5. Crosstalk Between Any Two Switches

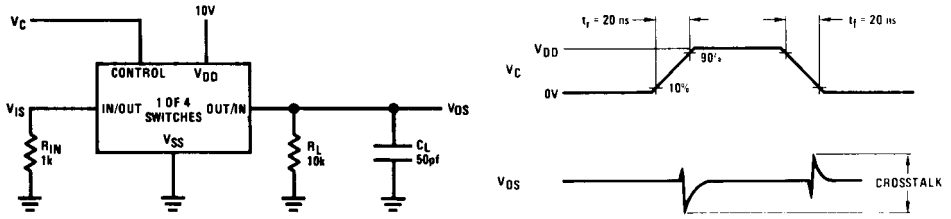


FIGURE 6. Crosstalk: Control Input to Signal Output

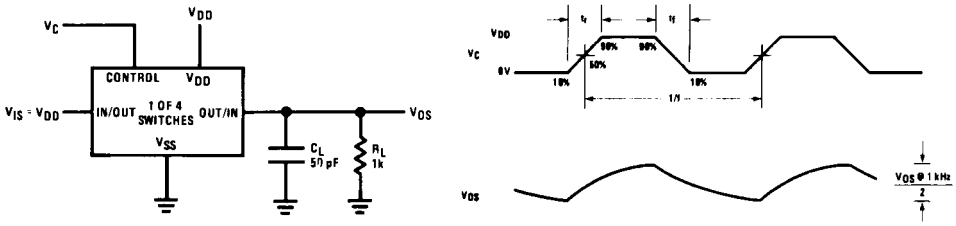
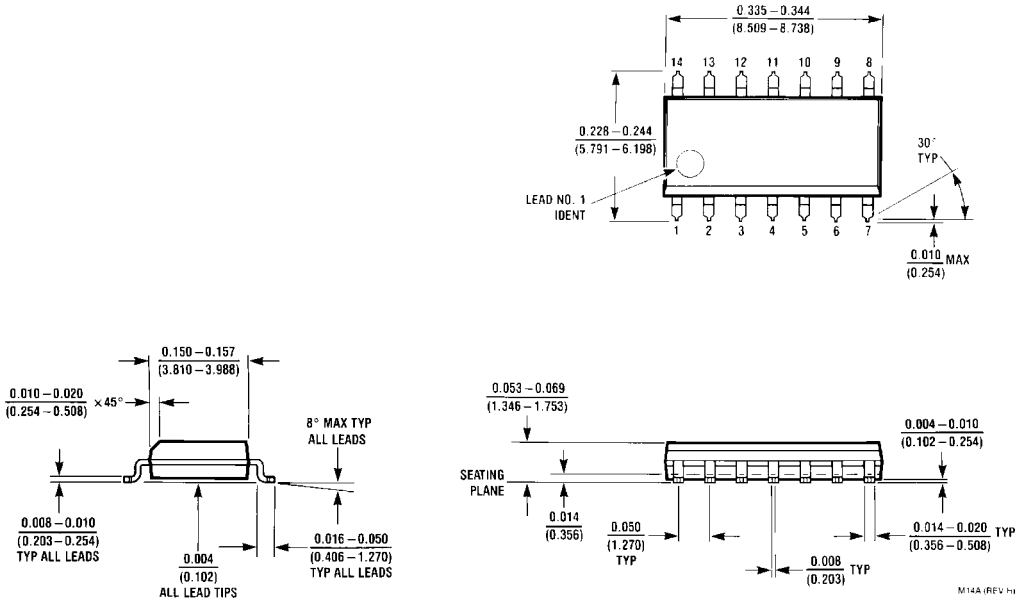


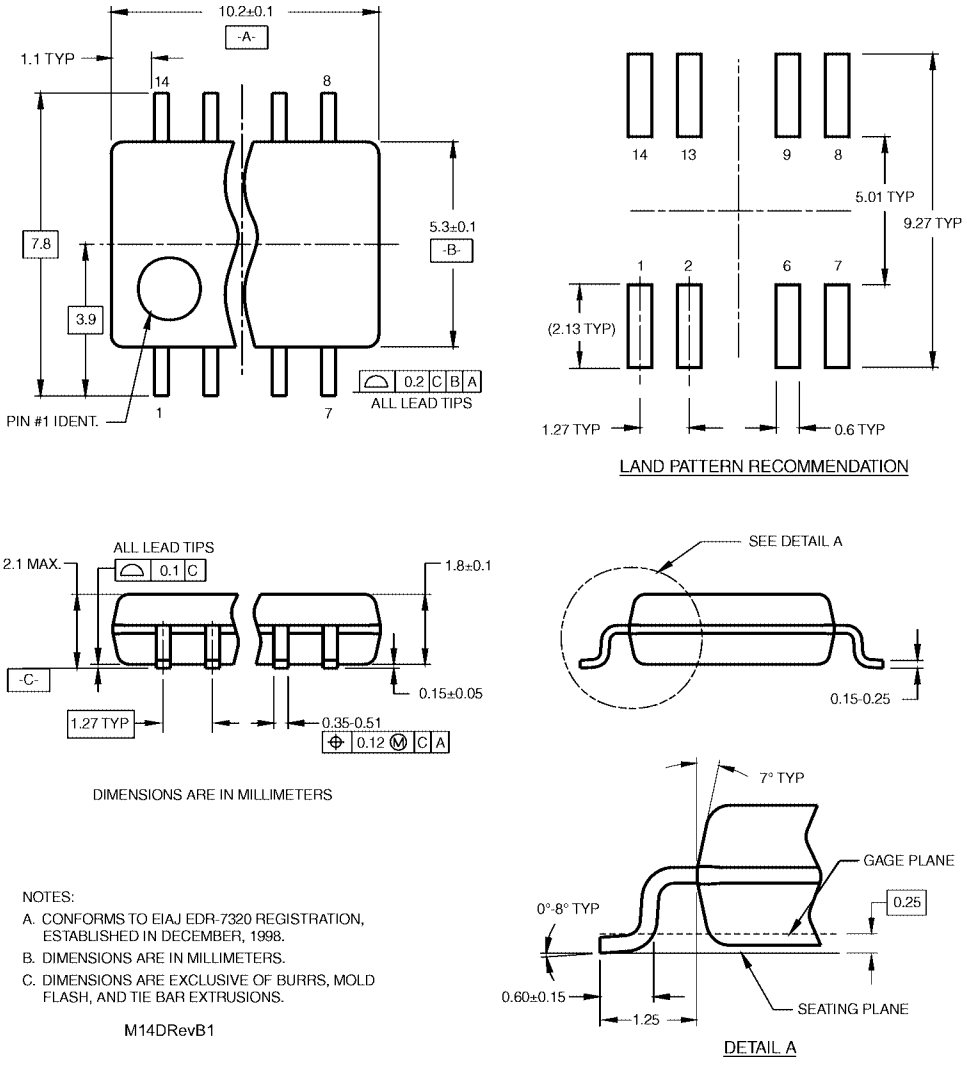
FIGURE 7. Maximum Control Input Frequency

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

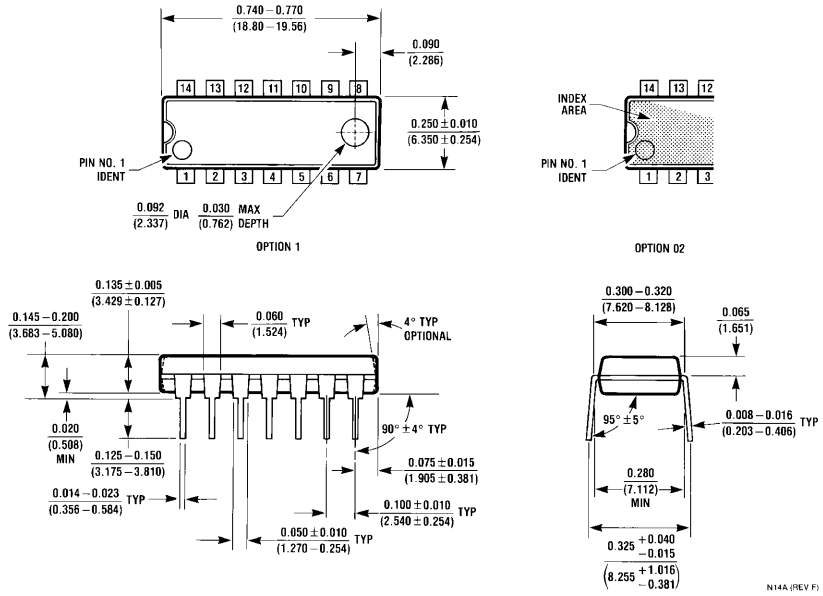
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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