## Document Title

**32Kx8 bit Low Power CMOS Static RAM**

## Revision History

| Revision No | History | Draft Data | Remark |
|---|---|---|---|
| 0.0 | Initial draft | May 18, 1997 | Design target |
| 0.1 | First revision<br>- KM62256DL/DLI $I_{SB1}$ = 100 → 50µA<br>KM62256DL-L $I_{SB1}$ = 20 → 10µA<br>KM62256DLI-L $I_{SB1}$ = 50 → 15µA<br>- $C_{IN}$ = 6 → 8pF, $C_{IO}$ = 8 → 10pF<br>- KM62256D-4/5/7 Family<br>tOH = 5 → 10ns<br>- KM62256DL/DLI $I_{DR}$ = 50→30µA<br>KM62256DL-L/DLI-L $I_{DR}$ = 30 → 15µA | April 1, 1997 | Preliminily |
| 1.0 | Finalize<br>- Remove $I_{CC}$ write value<br>- Improved operating current<br>$I_{CC2}$ = 70 → 60mA<br>- Improved standby current<br>KM62256DL/DLI $I_{SB1}$ = 50 → 30µA<br>KM62256DL-L $I_{SB1}$ = 10 → 5µA<br>KM62256DLI-L $I_{SB1}$ = 15 → 5µA<br>- Improved data retention current<br>KM62256DL/DLI $I_{DR}$ = 30 → 5µA<br>KM62256DL-L/DLI-L $I_{DR}$ = 15 → 3µA<br>- Remove 45ns part from commercial product and 100ns part from industrial product.<br>Replace test load 100pF to 50pF for 55ns part | November 11, 1997 | Final |

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## *32Kx8 bit Low Power CMOS Static RAM*

## FEATURES

- Process Technology: TFT
- Organization: 32Kx8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 28-DIP-600B, 28-SOP-450
  28-TSOP1-0813.4 F/R

## GENERAL DESCRIPTION

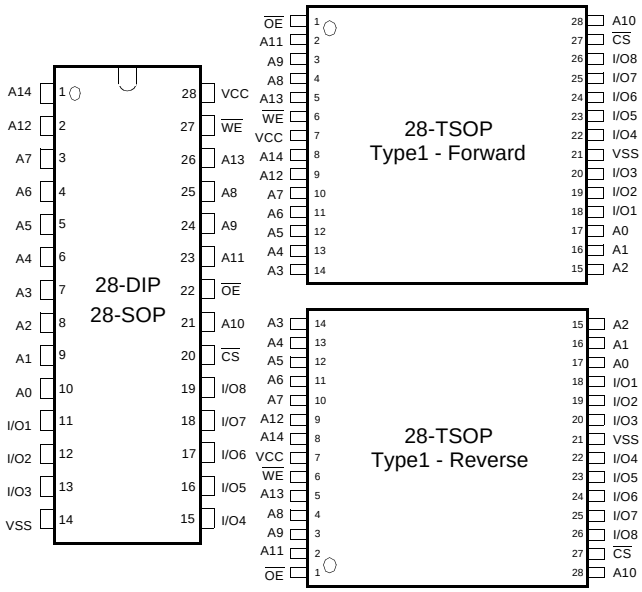
The K6T0808C1D families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

## PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | | PKG Type |
|---|---|---|---|---|---|---|
| | | | | Standby ($I_{SB1}$, Max) | Operating ($I_{CC2}$, Max) | |
| K6T0808C1D-L | Commercial (0~70°C) | 4.5 to 5.5V | 55[1]/70ns | 30µA | 60mA | 28-DIP-600B, 28-SOP-450 28-TSOP1-0813.4 F/R |
| K6T0808C1D-B | | | | 5µA | | |
| K6T0808C1D-P | Industrial (-40~85°C) | | 70ns | 30µA | | 28-SOP-450 28-TSOP1-0813.4 F/R |
| K6T0808C1D-F | | | | 5µA | | |

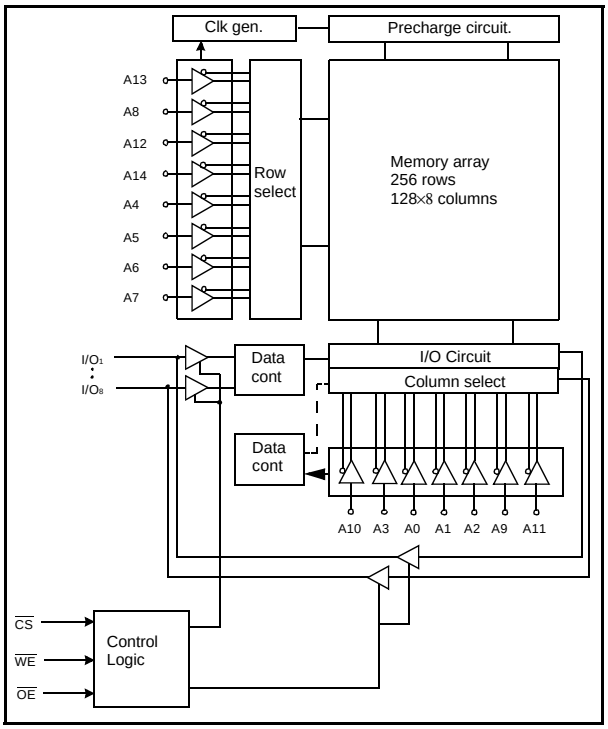
1. The parameter is tested with 50pF test load.

## PIN DESCRIPTION




| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| $\overline{CS}$ | Chip Select Input | $I/O_1$~$I/O_8$ | Data Inputs/Outputs |
| $\overline{OE}$ | Output Enable Input | Vcc | Power |
| $\overline{WE}$ | Write Enable Input | Vss | Ground |
| $A_0$~$A_{14}$ | Address Inputs | NC | No connect |

## FUNCTIONAL BLOCK DIAGRAM

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## PRODUCT LIST

| Commercial Temperature Products(0~70°C) | | Industrial Temperature Products(-40~85°C) | |
|---|---|---|---|
| **Part Name** | **Function** | **Part Name** | **Function** |
| K6T0808C1D-DL55 | 28-DIP, 55ns, L-pwr | K6T0808C1D-GP70 | 28-SOP, 70ns, L-pwr |
| K6T0808C1D-DB55 | 28-DIP, 55ns, LL-pwr | K6T0808C1D-GF70 | 28-SOP, 70ns, LL-pwr |
| K6T0808C1D-DL70 | 28-DIP, 70ns, L-pwr | K6T0808C1D-TP70 | 28-TSOP1-F, 70ns, L-pwr |
| K6T0808C1D-DB70 | 28-DIP, 70ns, LL-pwr | K6T0808C1D-TF70 | 28-TSOP1-F, 70ns, LL-pwr |
| K6T0808C1D-GL55 | 28-SOP, 55ns, L-pwr | K6T0808C1D-RP70 | 28-TSOP1-R, 70ns, L-pwr |
| K6T0808C1D-GB55 | 28-SOP, 55ns, LL-pwr | K6T0808C1D-RF70 | 28-TSOP1-R, 70ns, LL-pwr |
| K6T0808C1D-GL70 | 28-SOP, 70ns, L-pwr | | |
| K6T0808C1D-GB70 | 28-SOP, 70ns, LL-pwr | | |
| K6T0808C1D-TL55 | 28-TSOP1-F, 55ns, L-pwr | | |
| K6T0808C1D-TB55 | 28-TSOP1-F, 55ns, LL-pwr | | |
| K6T0808C1D-TL70 | 28-TSOP1-F, 70ns, L-pwr | | |
| K6T0808C1D-TB70 | 28-TSOP1-F, 70ns, LL-pwr | | |
| K6T0808C1D-RL55 | 28-TSOP1-R, 55ns, L-pwr | | |
| K6T0808C1D-RB55 | 28-TSOP1-R, 55ns, LL-pwr | | |
| K6T0808C1D-RL70 | 28-TSOP1-R, 70ns, L-pwr | | |
| K6T0808C1D-RB70 | 28-TSOP1-R, 70ns, LL-pwr | | |

## FUNCTIONAL DESCRIPTION

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Mode | Power |
|---|---|---|---|---|---|
| H | X[1)] | X[1)] | High-Z | Deselected | Standby |
| L | H | H | High-Z | Output Disabled | Active |
| L | L | H | Dout | Read | Active |
| L | X[1)] | L | Din | Write | Active |

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit | Remark |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$,$V_{OUT}$ | -0.5 to 7.0 | V | - |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.5 to 7.0 | V | - |
| Power Dissipation | $P_D$ | 1.0 | W | - |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C | - |
| Operating Temperature | $T_A$ | 0 to 70 | °C | K6T0808C1D-L/-B |
| | | -40 to 85 | °C | K6T0808C1D-P/-F |
| Soldering temperature and time | $T_{SOLDER}$ | 260°C, 10sec (Lead Only) | - | - |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS[1)]

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | Vcc | 4.5 | 5.0 | 5.5 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | 2.2 | - | Vcc+0.5V[2)] | V |
| Input low voltage | $V_{IL}$ | -0.5[3)] | - | 0.8 | V |

Note:
1. Commercial Product: $T_A$=0 to 70°C, otherwise specified
   Industrial Product: $T_A$=-40 to 85°C, otherwise specified
2. Overshoot: $V_{CC}$+3.0V in case of pulse width≤30ns
3. Undershoot: -3.0V in case of pulse width≤30ns
4. Overshoot and undershoot are sampled, not 100% tested

## CAPACITANCE[1)] (f=1MHz, $T_A$=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}$=0V | - | 10 | pF |

1. Capacitance is sampled not, 100% tested

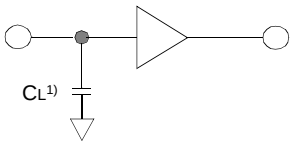
## DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | | -1 | - | 1 | µA |
| Operating power supply current | $I_{CC}$ | $I_{IO}$=0mA, $\overline{CS}$=$V_{IL}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$, Read | | - | 5 | 10 | mA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100% duty, $I_{IO}$=0mA, $\overline{CS}$≤0.2V, $V_{IN}$≤0.2V, $V_{IN}$≥Vcc -0.2V | Read | - | 2 | 5 | mA |
| | | | Write | | - | 20 | |
| | $I_{CC2}$ | Cycle time=Min,100% duty, $I_{IO}$=0mA, $\overline{CS}$=$V_{IL}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$ | | - | 45 | 60 | mA |
| Output low voltage | $V_{OL}$ | $I_{OL}$=2.1mA | | - | - | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | | 2.4 | - | - | V |
| Standby Current(TTL) | $I_{SB}$ | $\overline{CS}$=$V_{IH}$, Other inputs=$V_{IH}$ or $V_{IL}$ | | - | - | 1 | mA |
| Standby Current (CMOS) | $I_{SB1}$ | $\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc | Low Power | - | 1 | 30 | µA |
| | | | Low Low Power | - | 0.2 | 5 | µA |

## AC OPERATING CONDITIONS

**TEST CONDITIONS** (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load (See right): $C_L$=100pF+1TTL
$C_L$=50pF+1TTL




1. Including scope and jig capacitance

## AC CHARACTERISTICS (Vcc=4.5~5.5V, Commercial product: $T_A$=0 to 70°C, Industrial product: $T_A$=-40 to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 55[1]ns | | 70ns | | |
| | | | Min | Max | Min | Max | |
| Read | Read cycle time | $t_{RC}$ | 55 | - | 70 | - | ns |
| | Address access time | $t_{AA}$ | - | 55 | - | 70 | ns |
| | Chip select to output | $t_{CO}$ | - | 55 | - | 70 | ns |
| | Output enable to valid output | $t_{OE}$ | - | 25 | - | 35 | ns |
| | Chip select to low-Z output | $t_{LZ}$ | 10 | - | 10 | - | ns |
| | Output enable to low-Z output | $t_{OLZ}$ | 5 | - | 5 | - | ns |
| | Chip disable to high-Z output | $t_{HZ}$ | 0 | 20 | 0 | 30 | ns |
| | Output disable to high-Z output | $t_{OHZ}$ | 0 | 20 | 0 | 30 | ns |
| | Output hold from address change | $t_{OH}$ | 10 | - | 10 | - | ns |
| Write | Write cycle time | $t_{WC}$ | 55 | - | 70 | - | ns |
| | Chip select to end of write | $t_{CW}$ | 45 | - | 60 | - | ns |
| | Address set-up time | $t_{AS}$ | 0 | - | 0 | - | ns |
| | Address valid to end of write | $t_{AW}$ | 45 | - | 60 | - | ns |
| | Write pulse width | $t_{WP}$ | 40 | - | 50 | - | ns |
| | Write recovery time | $t_{WR}$ | 0 | - | 0 | - | ns |
| | Write to output high-Z | $t_{WHZ}$ | 0 | 20 | 0 | 25 | ns |
| | Data to write time overlap | $t_{DW}$ | 25 | - | 30 | - | ns |
| | Data hold from write time | $t_{DH}$ | 0 | - | 0 | - | ns |
| | End write to output low-Z | $t_{OW}$ | 5 | - | 5 | - | ns |

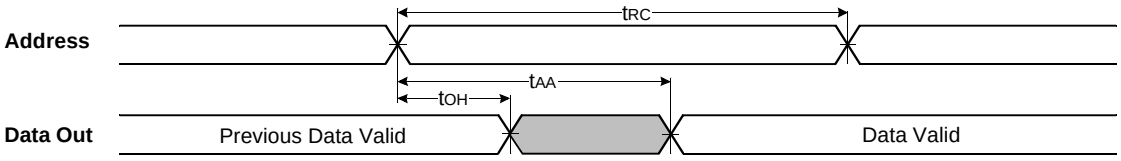
1. The parameter is tested with 50pF test load.

## DATA RETENTION CHARACTERISTICS

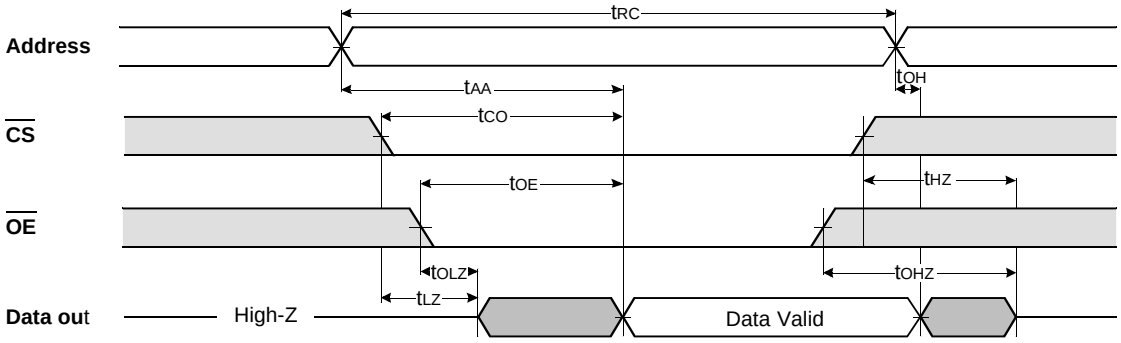
| Item | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS}$≥Vcc-0.2V | | 2.0 | - | 5.5 | V |
| Data retention current | $I_{DR}$ | Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V | L-Ver | - | 1 | 15 | µA |
| | | | LL-Ver | - | 0.2 | 3 | |
| Data retention set-up time | $t_{SDR}$ | See data retention waveform | | 0 | - | - | ms |
| Recovery time | $t_{RDR}$ | | | 5 | - | - | |

## TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$V_{IL}$, $\overline{WE}$=$V_{IH}$)



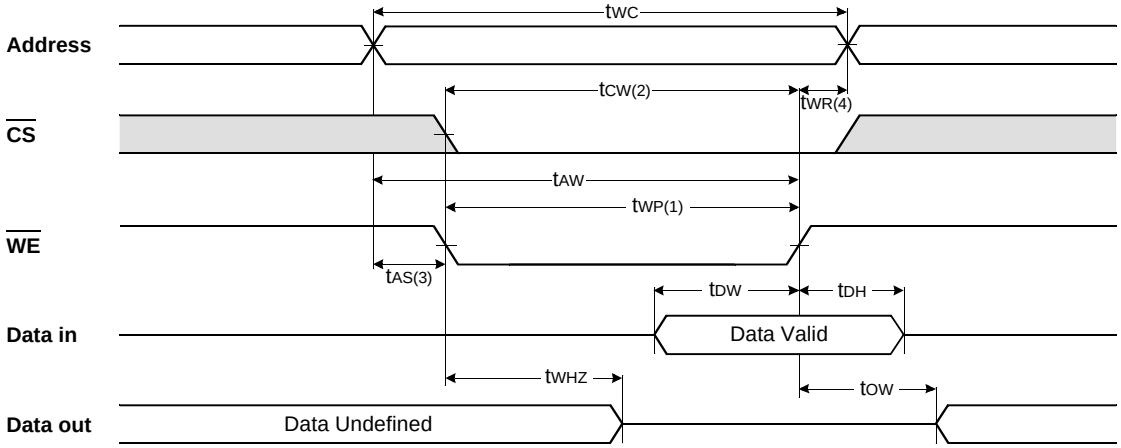

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



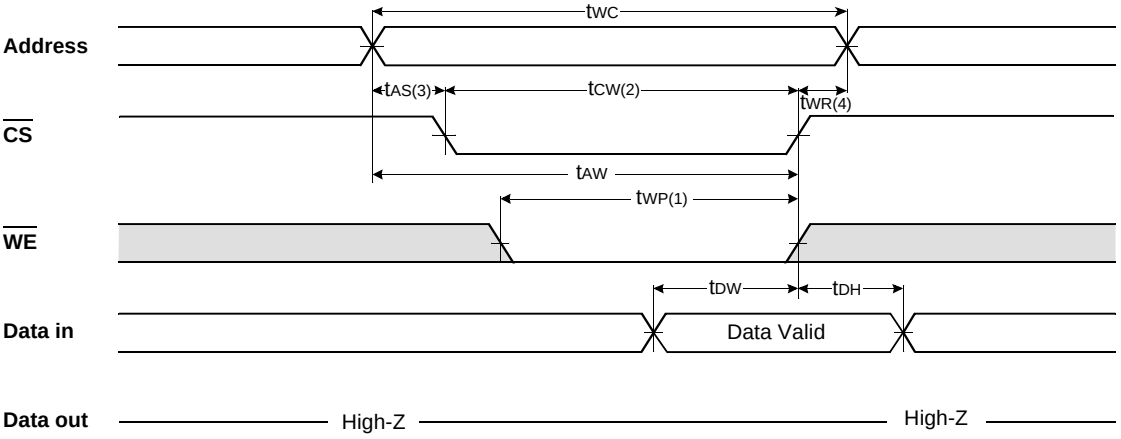

**NOTES (**READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

**TIMING WAVEFORM OF WRITE CYCLE(1)** ($\overline{WE}$ Controlled)




**TIMING WAVEFORM OF WRITE CYCLE(2)** ($\overline{CS}$ Controlled)

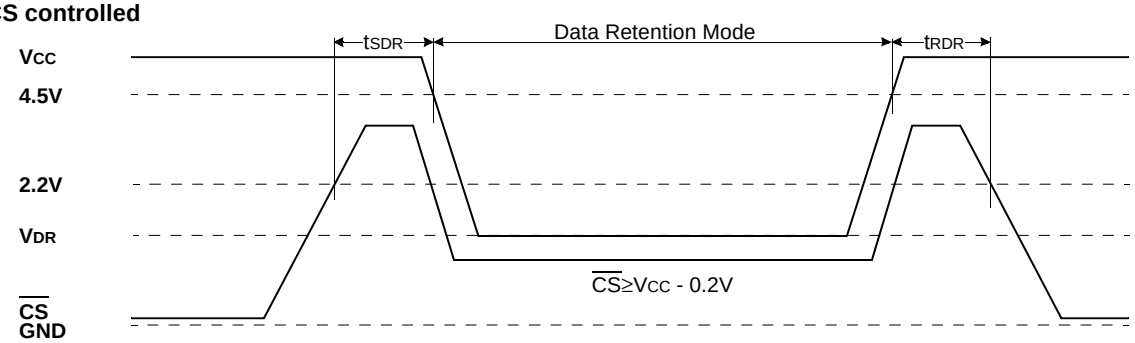



**NOTES** (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, $t_{WP}$ is measured from the begining of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS}$ going low to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end or write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

## DATA RETENTION WAVE FORM

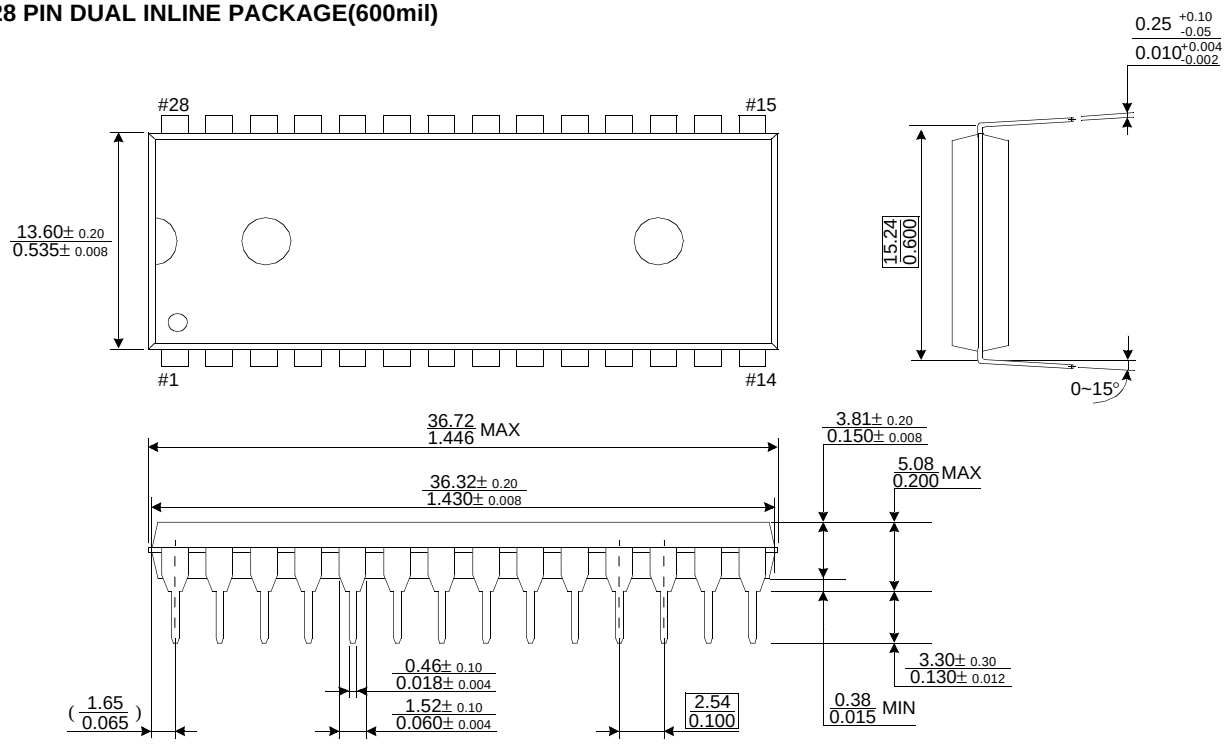
**$\overline{CS}$ controlled**



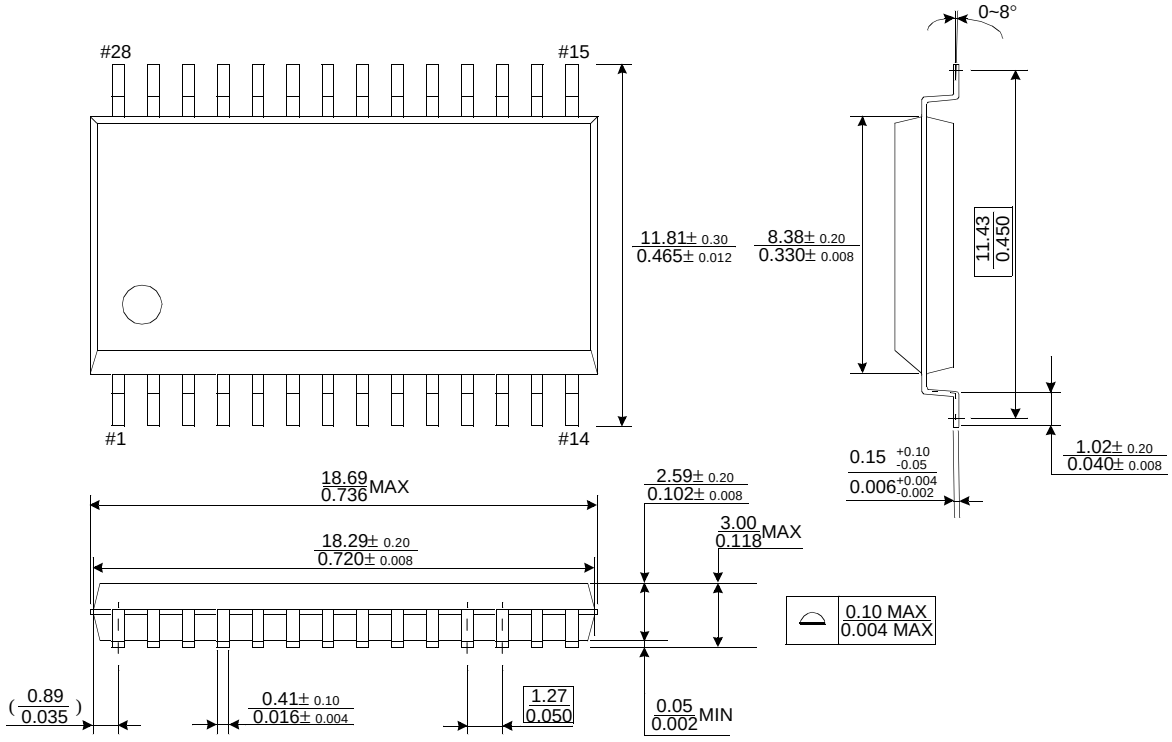
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 28 PIN DUAL INLINE PACKAGE(600mil)



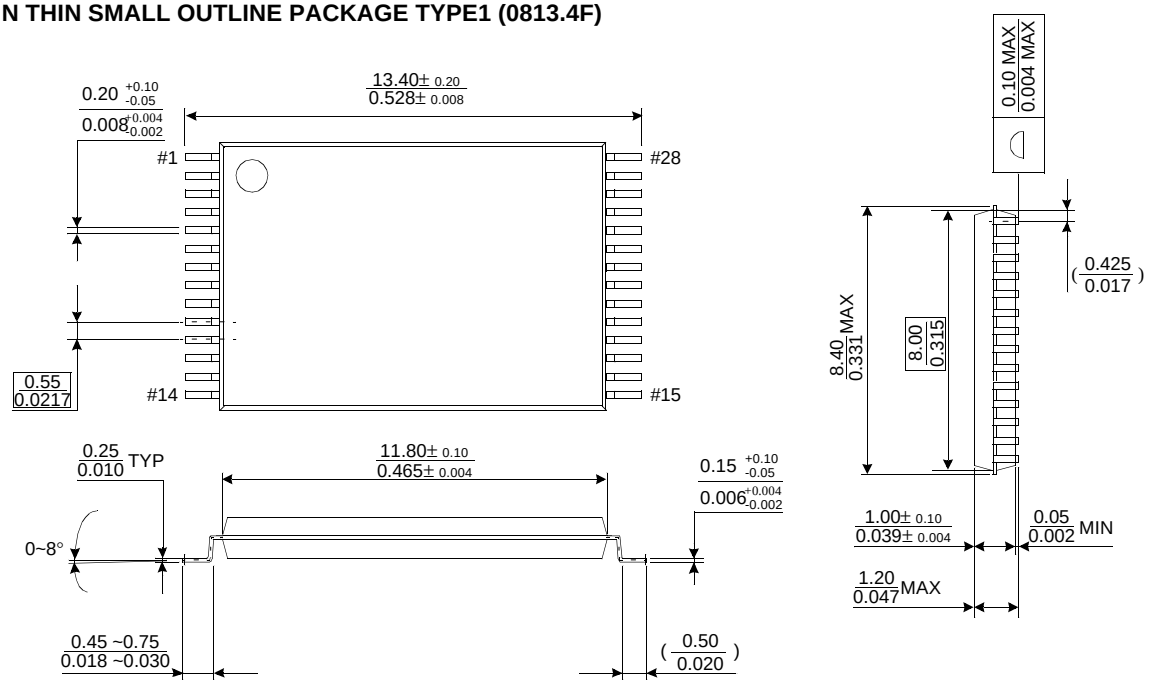

### 28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



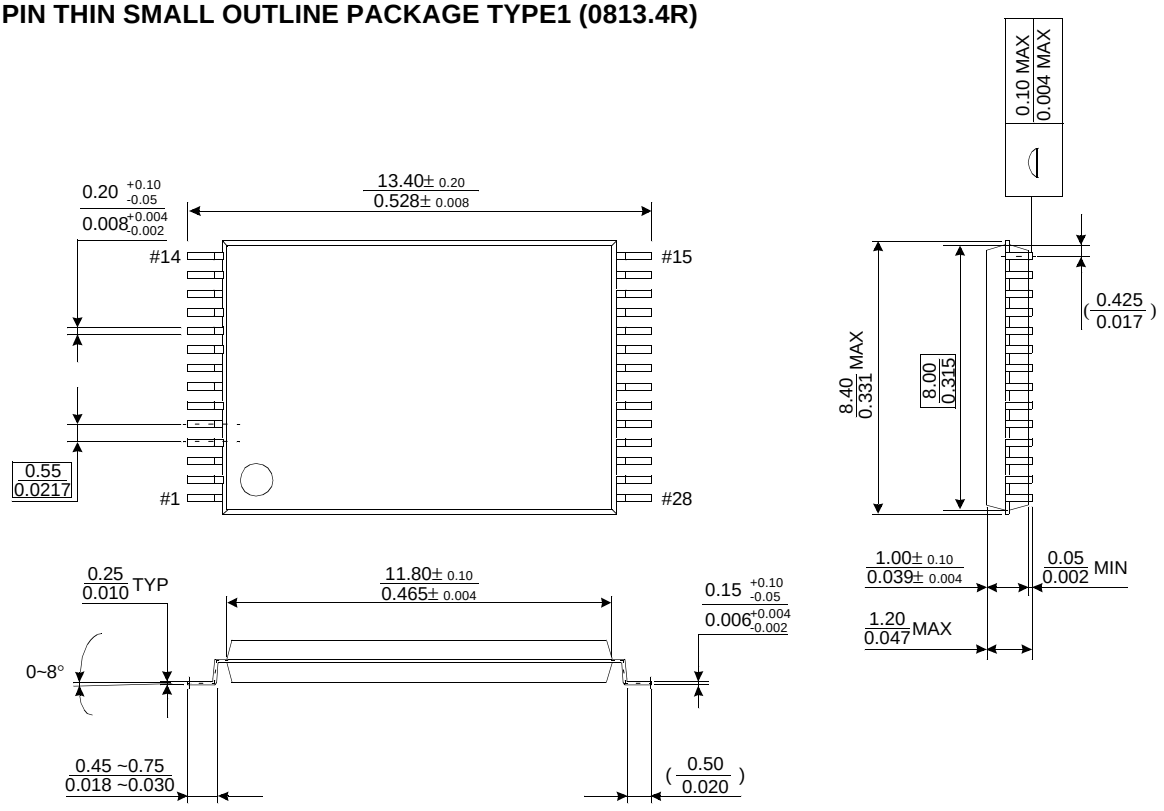
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)




### 28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)



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Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

**Kategorilere göz atın**

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