MCM6064
MCM60L64

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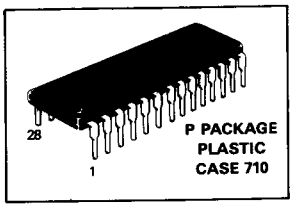
Advance Information

8K x 8 Bit CMOS Static Random Access Memory



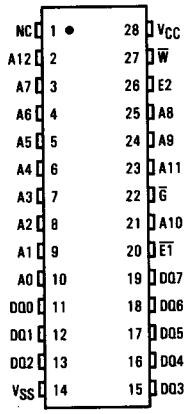
The MCM6064 is a 65,536 bit low-power static random access memory organized as 8192 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The maximum operating current is 5 mA/MHz and corresponding maximum power consumption is 27.5 mW/MHz.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. For MCM6064 typical standby current is 3 μA, with a maximum of 100 μA. For MCM60L64 typical standby current is 1 μA. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

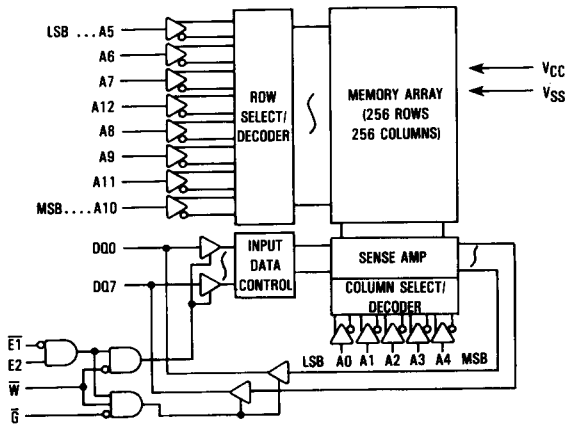
The MCM6064 is available in a 600 mil, 28 pin plastic dual-in-line package.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—248 mW (Maximum Active)
- Two Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L64)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Pin Compatible with 2764 EPROM Family
- Three State Outputs
- Fast Access Times:
  MCM6064-10 and MCM60L64-10=100 ns (Max)
  MCM6064-12 and MCM60L64-12=120 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	μA
DC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL})	I_{CC}	—	—	10	mA
AC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0) MCM6064-10: t_{AVAV} = 100 ns MCM6064-12: t_{AVAV} = 120 ns	I_{CCA}	 — —	 — —	 45 40	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} −0.2 or E2 ≤ 0.2 V) MCM6064 MCM60L64	I_{SB2}	— —	3 1	100 30	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

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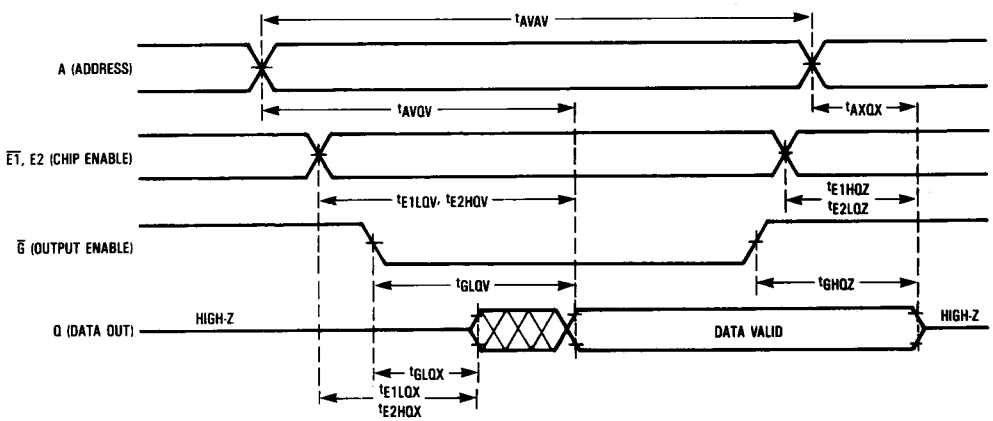
READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	100	–	120	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	100	–	120	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	100	–	120	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	100	–	120	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	50	–	60	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	20	–	20	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	35	0	40	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	0	40	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



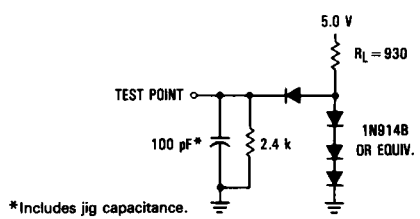
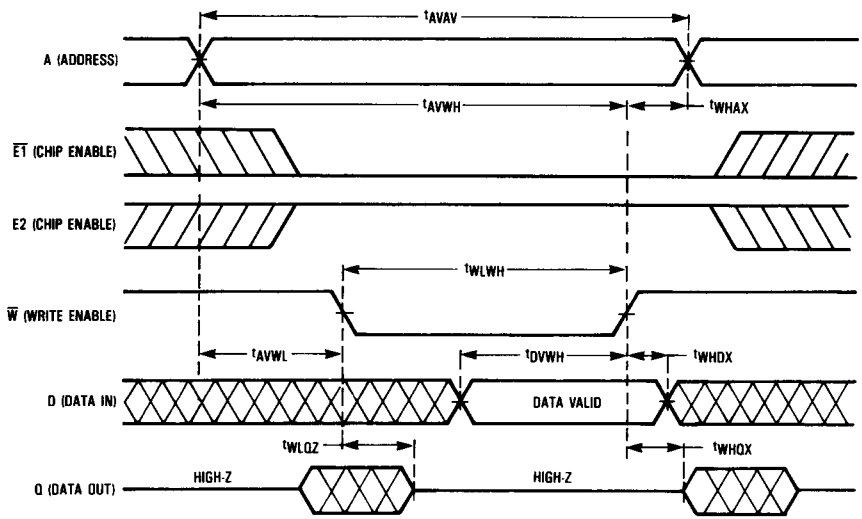


Figure 1. AC Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	80	–	85	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	40	–	50	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	35	0	40	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

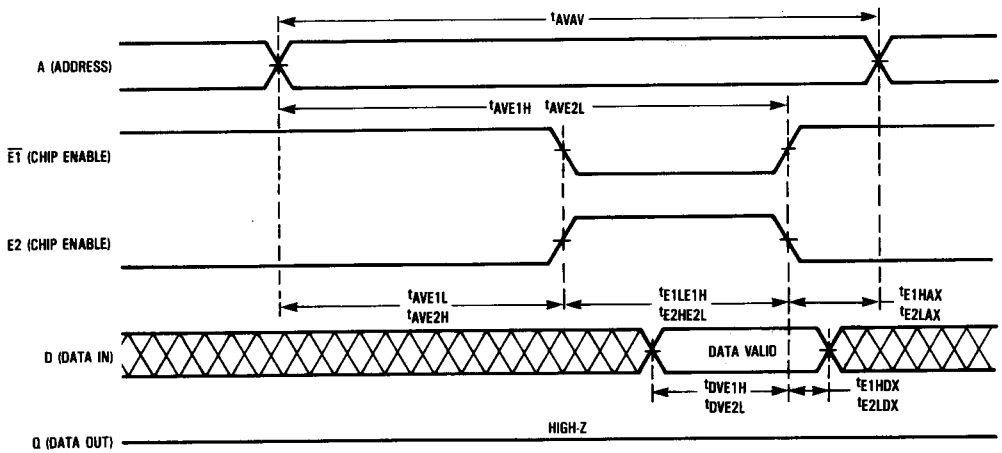
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



WRITE CYCLE 2 ($\overline{E1}$, E2 CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	120	–	ns	–
Address Setup Time	t_{AVE1L}, t_{AVE2H}	t_{AS}	0	–	0	–	ns	2
Address Valid to End of Write	t_{AVE1H}, t_{AVE2L}	t_{AW}	80	–	85	–	ns	2
Chip Enable to End of Write	t_{E1LE1H}, t_{E2HE2L}	t_{CW}	80	–	85	–	ns	2, 3
Data Valid to End of Write	t_{DVE1H}, t_{DVE2L}	t_{DW}	40	–	50	–	ns	2
Data Hold Time	t_{E1HDX}, t_{E2LDX}	t_{DH}	0	–	0	–	ns	2, 4
Write Recovery Time	t_{E1HAX}, t_{E2LAX}	t_{WR}	0	–	0	–	ns	2, 5

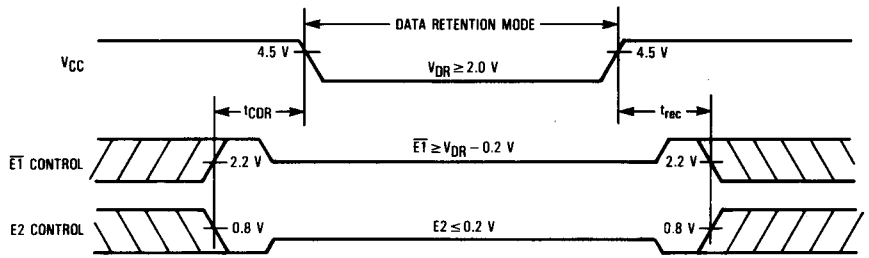
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{W}$ must be high during all address transitions.



DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V)	V_{DR}	2.0	—	5.5	V
Data Retention Current ($\overline{E1} \geq V_{CC} - 0.2$ or E2 ≤ 0.2 V)	I_{CCDR}				μA
MCM6064: V_{CC} = 3.0 V		—	—	50	
V_{CC} = 5.5 V		—	—	100	
MCM60L64: V_{CC} = 3.0 V		—	—	15	
V_{CC} = 5.5 V		—	—	30	
Chip Disable to Data Retention Time	t_{CDR}	0	—	—	ns
Operation Recovery Time	t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6064 or 60L64 X XX

Motorola Memory Prefix

Part Number
(With L = Low Power Version)

Speed (10 = 100 ns, 12 = 120 ns)

Package (P = Plastic)

Full Part Numbers — MCM6064P10 MCM60L64P10
MCM6064P12 MCM60L64P12

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