HEF4051B

8-channel analog multiplexer/demultiplexer

Rev. 04 — 12 January 2005 Product data sheet

1. General description

The HEF4051B is an 8-channel analog multiplexer/demultiplexer with three address inputs (A0 to A2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z).

The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low-impedance ON-state) by A0 to A2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of A0 to A2. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A0 to A2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 V to 15 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

2. Features

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Multiple package option
- Specified from –40 °C to +85 °C

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3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C; R_L = 10 kΩ; C_L = 50 pF; $\overline{E}$ = V_{DD} (square wave); V_{is} = V_{DD} = 15 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time HIGH to OFF for $\overline{E}$ to Z or $\overline{E}$ to Yn		-	85	170	ns
t_{PLZ}	output disable time LOW to OFF for $\overline{E}$ to Z or $\overline{E}$ to Yn		-	115	230	ns
t_{PZH}, t_{PZL}	output enable time OFF to HIGH or LOW for $\overline{E}$ to Z or $\overline{E}$ to Yn		-	40	80	ns
C_i	input capacitance digital inputs		-	-	7.5	pF

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4051BP	–40 °C to +85 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
HEF4051BT	–40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF4051BTS	–40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
HEF4051BTT	–40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

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5. Functional diagram

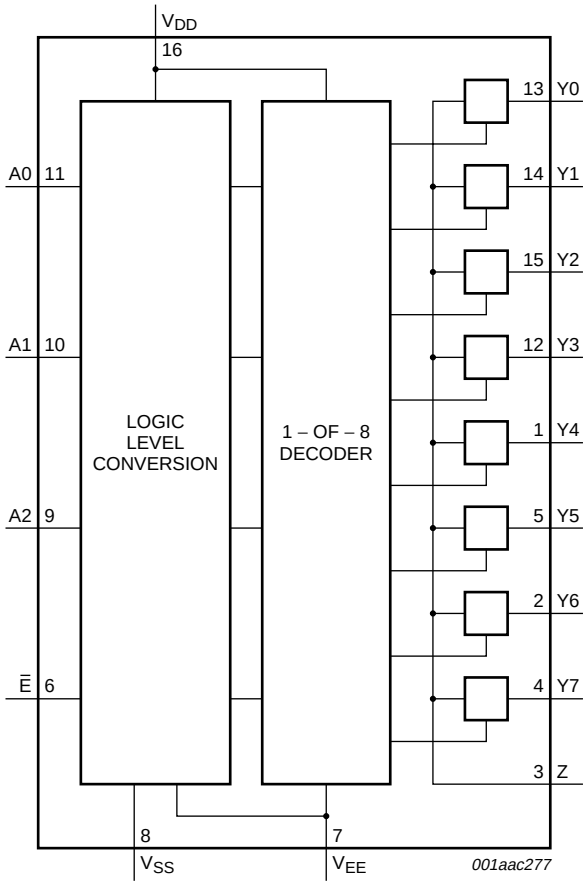

Fig 1. Functional diagram

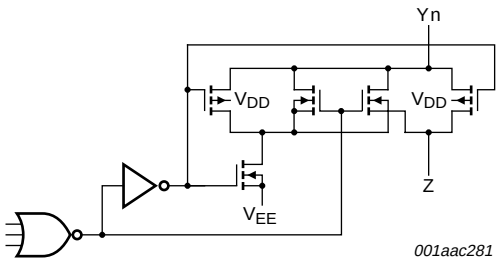

Fig 2. Schematic diagram (one switch)

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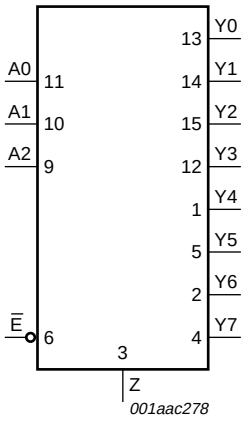

Fig 3. Logic symbol

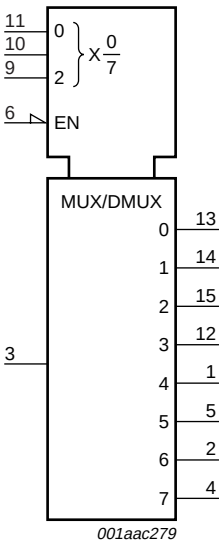

Fig 4. IEC logic symbol

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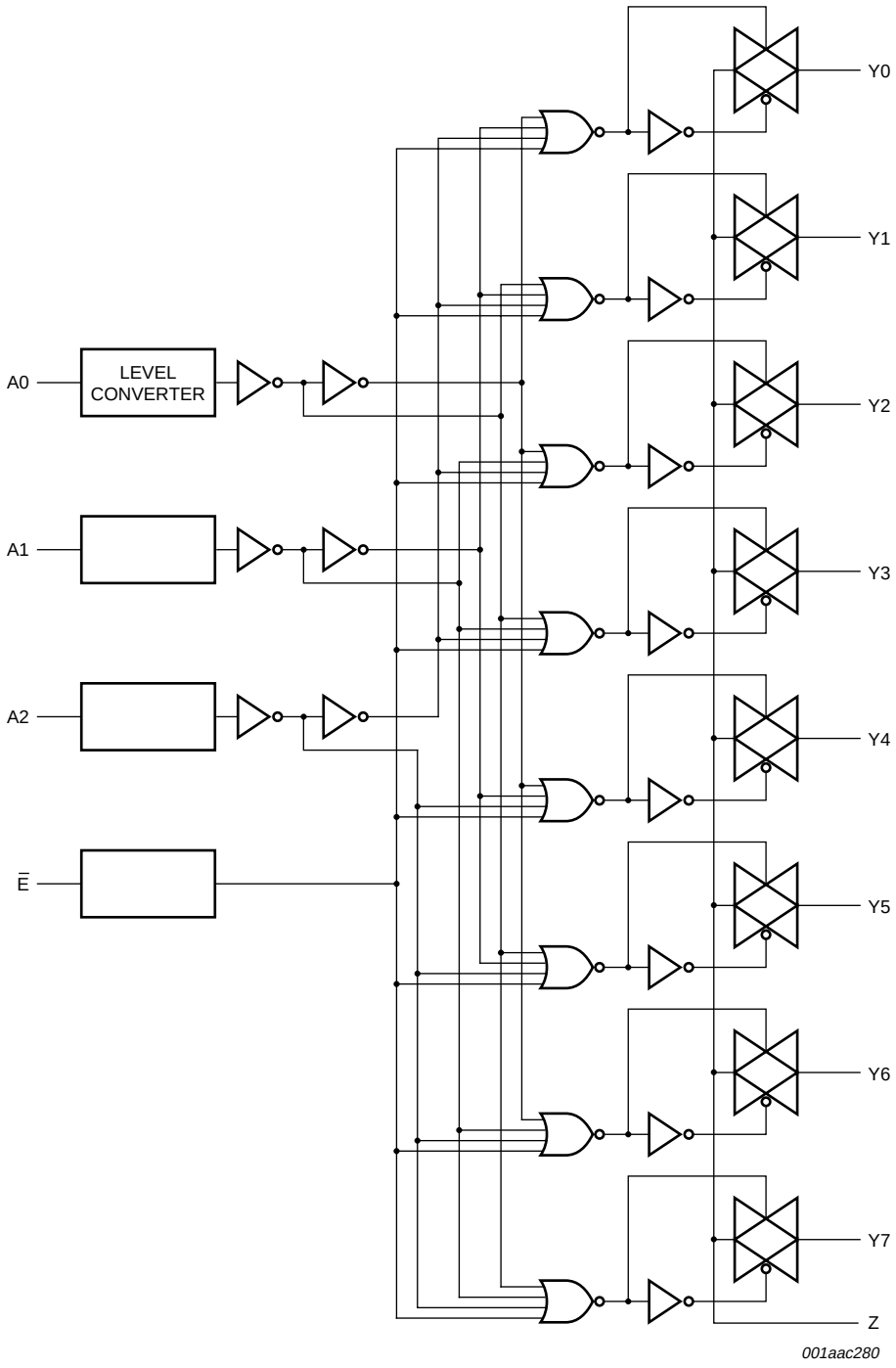

Fig 5. Logic diagram

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6. Pinning information

6.1 Pinning

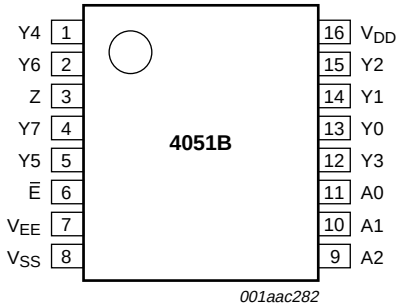

Fig 6. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Y4	1	independent input/output
Y6	2	independent input/output
Z	3	common input/output
Y7	4	independent input/output
Y5	5	independent input/output
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage of switches
V_{SS}	8	ground (0 V)
A2	9	address input
A1	10	address input
A0	11	address input
Y3	12	independent input/output
Y0	13	independent input/output
Y1	14	independent input/output
Y2	15	independent input/output
V_{DD}	16	supply voltage

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7. Functional description

Table 4: Function table [1]

Inputs				Channel ON
$\overline{E}$	A2	A1	A0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	–0.5	+18	V
V_{EE}	supply voltage of switches	referenced to V_{DD}	[1]	–18	+0.5	V
V_I	voltage on any input			–0.5	V_{DD} + 0.5	V
I	DC current into any input or output			-	±10	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +85 °C				
	DIP16		[2]	-	700	mW
	SO16, SSOP16 and TSSOP16		[2]	-	500	mW
P_o	power dissipation per output			-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

[2] For DIP16 packages: above 70 °C, derate linearly with 12 mW/K.
For SO16 packages: above 70 °C, derate linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C, derate linearly with 5.5 mW/K.

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9. Static characteristics

Table 6: Static characteristics

V_{SS} = 0 V; unless otherwise specified

Symbol	Parameter	Conditions	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
			Min	Max	Min	Max	Min	Max	
I_{DD}	quiescent device current	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; I_O = 0 A							
		V_{DD} = 5 V	-	20	-	20	-	150	µA
		V_{DD} = 10 V	-	40	-	40	-	300	µA
		V_{DD} = 15 V	-	80	-	80	-	600	µA
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA							
		V_O = 0.5 V or 4.5 V; V_{DD} = 5 V	-	1.5	-	1.5	-	1.5	V
		V_O = 1.0 V or 9.0 V; V_{DD} = 10 V	-	3.0	-	3.0	-	3.0	V
		V_O = 1.5 V or 13.5 V; V_{DD} = 15 V	-	4.0	-	4.0	-	4.0	V
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA							
		V_O = 0.5 V or 4.5 V; V_{DD} = 5 V	3.5	-	3.5	-	3.5	-	V
		V_O = 1.0 V or 9.0 V; V_{DD} = 10 V	7.0	-	7.0	-	7.0	-	V
		V_O = 1.5 V or 13.5 V; V_{DD} = 15 V	11.0	-	11.0	-	11.0	-	V
I_{LI}	Input leakage current	V_I = 0 V or 15 V; V_{DD} = 15 V	-	0.3	-	0.3	-	1.0	µA
I_{OZ}	3-state output leakage current	V_{DD} = 15 V							
		output returned to V_{DD}	-	1.6	-	1.6	-	12.0	µA
		output returned to V_{SS}	-	−1.6	-	−1.6	-	−12.0	µA
C_i	input capacitance digital inputs		-	-	-	7.5	-	-	pF

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Table 7: Static characteristics for R_{ON}

T_{amb} = 25 °C; R_{ON} test conditions see Figure 8

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	ON resistance	V_{is} = 0 V to $V_{DD} - V_{EE}$				
		$V_{DD} - V_{EE}$ = 5 V	-	350	2500	Ω
		$V_{DD} - V_{EE}$ = 10 V	-	80	245	Ω
		$V_{DD} - V_{EE}$ = 15 V	-	60	175	Ω
		V_{is} = 0 V				
		$V_{DD} - V_{EE}$ = 5 V	-	115	340	Ω
		$V_{DD} - V_{EE}$ = 10 V	-	50	160	Ω
		$V_{DD} - V_{EE}$ = 15 V	-	40	115	Ω
		$V_{is} = V_{DD} - V_{EE}$				
		$V_{DD} - V_{EE}$ = 5 V	-	120	365	Ω
		$V_{DD} - V_{EE}$ = 10 V	-	65	200	Ω
		$V_{DD} - V_{EE}$ = 15 V	-	50	155	Ω
ΔR_{ON}	ON resistance difference between any two channels	V_{is} = 0 V to $V_{DD} - V_{EE}$				
		$V_{DD} - V_{EE}$ = 5 V	-	25	-	Ω
		$V_{DD} - V_{EE}$ = 10 V	-	10	-	Ω
		$V_{DD} - V_{EE}$ = 15 V	-	5	-	Ω
$I_{L(OFF)}$	OFF-state leakage current	$V_{SS} = V_{EE}$; $V_{DD} - V_{EE}$ = 15 V				
		all channels OFF; $\overline{E}$ at V_{DD}	-	-	1000	nA
		any channel; $\overline{E}$ at V_{SS}	-	-	200	nA

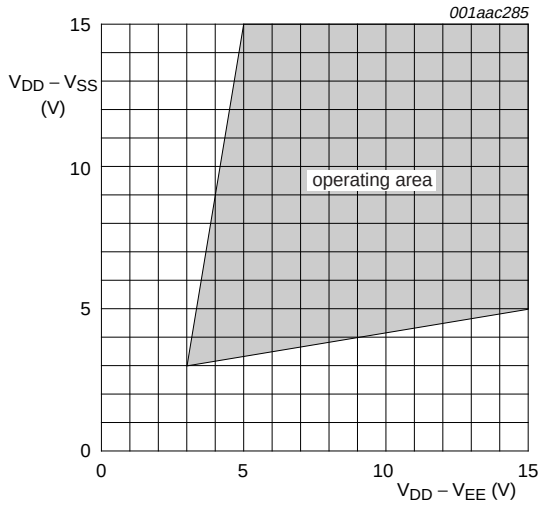

Fig 7. Operating area as a function of the supply voltages

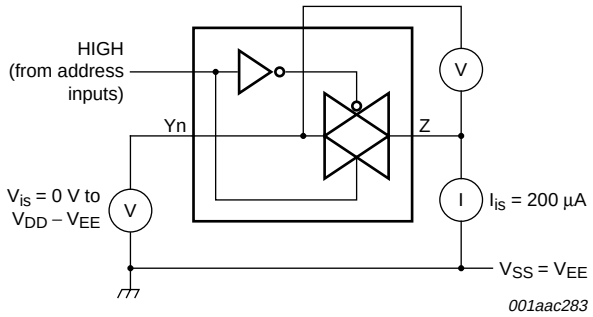

Fig 8. Test set-up for measuring R_{ON}

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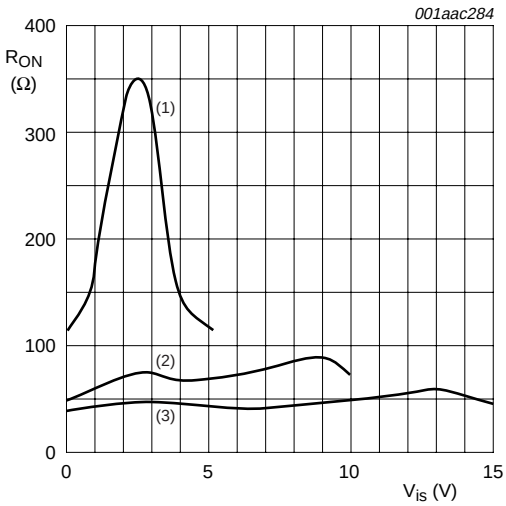

I_{is} = 200 µA; V_{SS} = V_{EE} = 0 V.

(1) V_{DD} = 5 V.

(2) V_{DD} = 10 V.

(3) V_{DD} = 15 V.

Fig 9. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8: Dynamic characteristics

V_{EE} = V_{SS} = 0 V; R_L = 10 kΩ; C_L = 50 pF; T_{amb} = 25 °C; input transition times ≤ 20 ns; test circuit see Figure 13.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay Z to Yn or Yn to Z	$\overline{E}$ = V_{SS}; V_{is} = V_{DD} (square-wave); see Figure 10	[1]				
		V_{DD} = 5 V		-	15	30	ns
		V_{DD} = 10 V		-	5	10	ns
		V_{DD} = 15 V		-	5	10	ns
t_{PHL}	HIGH to LOW propagation delay An to Z or An to Yn	$\overline{E}$ = V_{SS}; An = V_{DD} (square-wave); V_{is} = V_{EE}; see Figure 11	[1] [2]				
		V_{DD} = 5 V		-	150	300	ns
		V_{DD} = 10 V		-	60	120	ns
		V_{DD} = 15 V		-	45	90	ns
t_{PLH}	LOW to HIGH propagation delay An to Z or An to Yn	$\overline{E}$ = V_{SS}; An = V_{DD} (square-wave); V_{is} = V_{DD}; see Figure 11	[1] [2]				
		V_{DD} = 5 V		-	150	300	ns
		V_{DD} = 10 V		-	65	130	ns
		V_{DD} = 15 V		-	45	90	ns

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Table 8: Dynamic characteristics *…continued*

V_{EE} = V_{SS} = 0 V; R_L = 10 kΩ; C_L = 50 pF; T_{amb} = 25 °C; input transition times ≤ 20 ns; test circuit see Figure 13.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHZ}	output disable time HIGH to OFF for $\overline{E}$ to Z or $\overline{E}$ to Yn	$\overline{E}$ = V_{DD} (square wave); V_{is} = V_{DD}; see Figure 12	[1]				
		V_{DD} = 5 V		-	120	240	ns
		V_{DD} = 10 V		-	90	180	ns
		V_{DD} = 15 V		-	85	170	ns
t_{PLZ}	output disable time LOW to OFF for $\overline{E}$ to Z or $\overline{E}$ to Yn	$\overline{E}$ = V_{DD} (square wave); V_{is} = V_{EE}; see Figure 12	[1]				
		V_{DD} = 5 V		-	145	290	ns
		V_{DD} = 10 V		-	120	240	ns
		V_{DD} = 15 V		-	115	230	ns
t_{PZH}	output enable times OFF to HIGH or LOW for $\overline{E}$ to Z or $\overline{E}$ to Yn	$\overline{E}$ = V_{DD} (square wave); V_{is} = V_{DD}; see Figure 12	[1]				
		V_{DD} = 5 V		-	140	280	ns
		V_{DD} = 10 V		-	55	110	ns
		V_{DD} = 15 V		-	40	80	ns
t_{PZL}	output enable times OFF to HIGH or LOW for $\overline{E}$ to Z or $\overline{E}$ to Yn	$\overline{E}$ = V_{DD} (square wave); V_{is} = V_{EE}; see Figure 12	[1]				
		V_{DD} = 5 V		-	140	280	ns
		V_{DD} = 10 V		-	55	110	ns
		V_{DD} = 15 V		-	40	80	ns
P_D	dynamic power dissipation		[3]	-	-	-	-

[1] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as input. V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as output.

[2] The temperature coefficient for propagation delays is 0.35 %/°C.

[3] Dynamic power dissipation P_D can be calculated with the following formulae (P_D in µW):

for V_{DD} = 5 V, $P_D = 1000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$;

for V_{DD} = 10 V, $P_D = 5500 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$;

for V_{DD} = 15 V, $P_D = 15000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$, where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{DD} = supply voltage in V;

$\Sigma(C_L \times f_o)$ = sum of the outputs.

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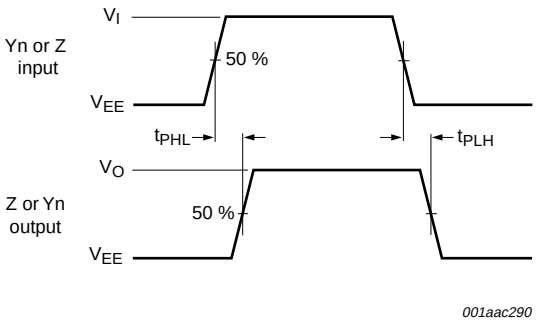
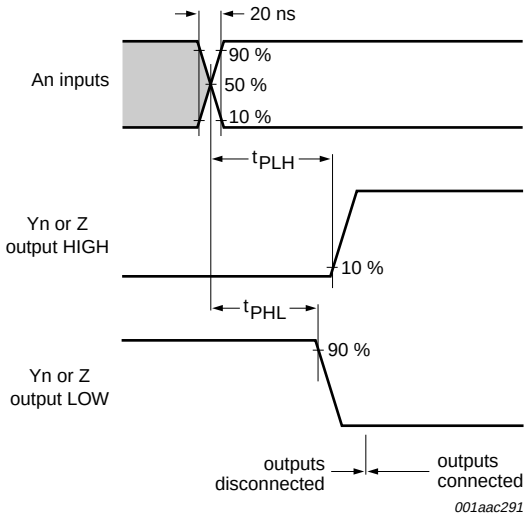
11. Waveforms



$t_r = t_f = 20$ ns

Fig 10. Input to output (Z to Yn or Yn to Z) propagation delays and output transition times



$t_r = t_f = 20$ ns

Fig 11. Input to output (Z to Yn or Yn to Z) propagation delays when other Y selected

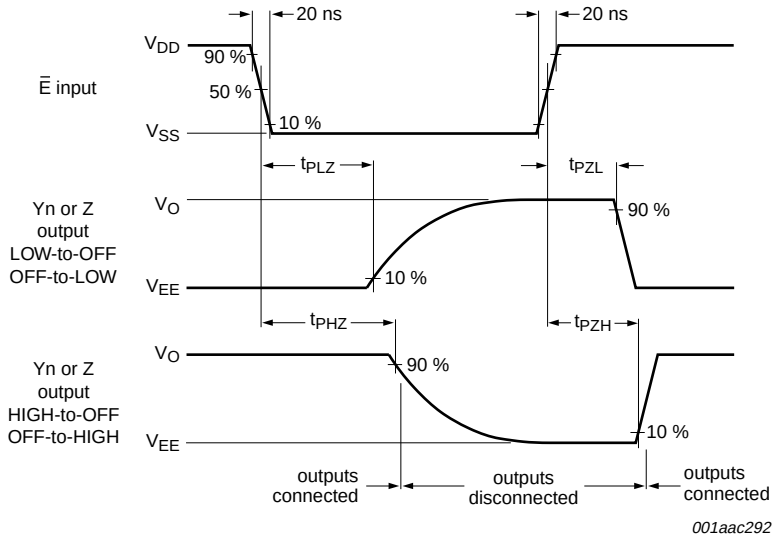


Fig 12. Enable and disable times of 3-state outputs

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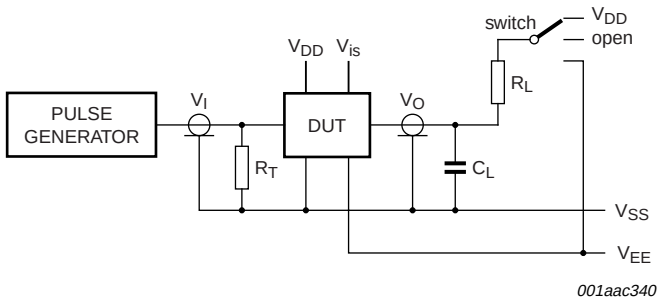

Test data is given in Table 9.

Definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 13. Load circuitry for switching times

Table 9: Test data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20 ns	50 pF	10 kΩ	V_{DD}
t_{PLH}	V_{DD}	20 ns	50 pF	10 kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20 ns	50 pF	10 kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20 ns	50 pF	10 kΩ	V_{DD}
other	pulse	20 ns	50 pF	10 kΩ	open

12. Additional dynamic characteristics

Table 10: Additional dynamic characteristics

V_{is} = 0.5V_{DD}(p-p) sine-wave and symmetrical.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
d_{sin}	distortion, sine-wave response	channel ON; R_L = 10 kΩ; C_L = 15 pF; f_{is} = 1 kHz; see Figure 14					
		V_{DD} = 5 V		-	0.25	-	%
		V_{DD} = 10 V		-	0.04	-	%
		V_{DD} = 15 V		-	0.04	-	%
f_{ct}	crosstalk between any two channels	V_{DD} = 10 V	[1]	-	1	-	MHz
V_{ct}	crosstalk $\overline{E}$ or An to Yn or Z	R_L = 10 kΩ; C_L = 15 pF; $\overline{E}$ or An = V_{DD} (square-wave); crosstalk is $\lvert V_{OS} \rvert$ (peak value); V_{DD} = 10 V; see Figure 15		-	50	-	mV
f_{OFF}	OFF-state feed-through	V_{DD} = 10 V	[2]	-	1	-	MHz

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Table 10: Additional dynamic characteristics *...continued*

V_{is} = 0.5V_{DD}(p-p) sine-wave and symmetrical.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{ON}	ON-state frequency response	V_{DD} = 5 V	[3]	-	13	-	MHz
		V_{DD} = 10 V	[3]	-	40	-	MHz
		V_{DD} = 15 V	[3]	-	70	-	MHz

[1] R_L = 1 kΩ; $20log\frac{V_{os}}{V_{is}} = -50$ dB; see Figure 16.

[2] R_L = 1 kΩ; C_L = 5 pF; channel OFF; $20log\frac{V_{os}}{V_{is}} = -50$ dB; see Figure 14.

[3] R_L = 1 kΩ; C_L = 5 pF; channel ON; $20log\frac{V_{os}}{V_{is}} = -3$ dB; see Figure 14.

13. Test circuits additional dynamic characteristics

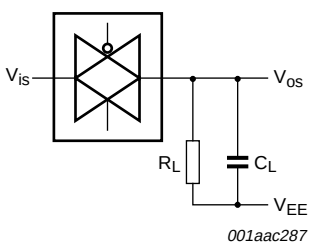


Fig 14. Load circuitry for sine wave distortion, OFF state frequency and ON state frequency measurement

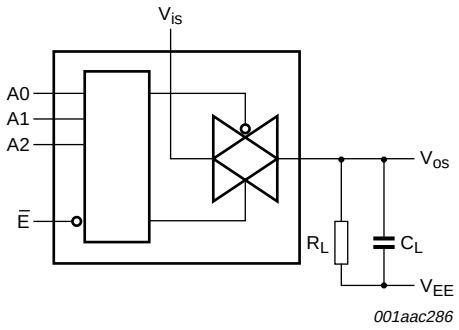
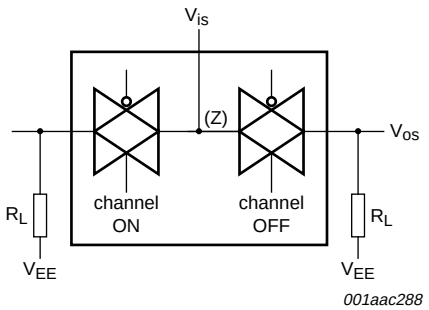
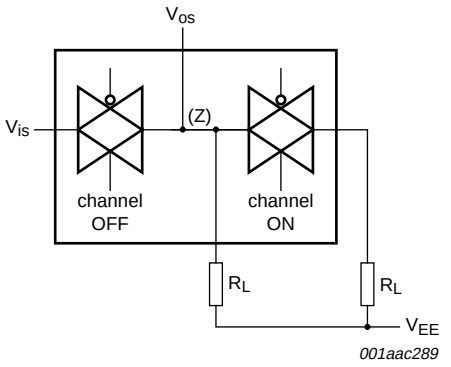


Fig 15. Load circuitry for crosstalk measurement of logic inputs to output



a. Channel ON condition



b. Channel OFF condition

Fig 16. Load circuitry for crosstalk measurement between channels

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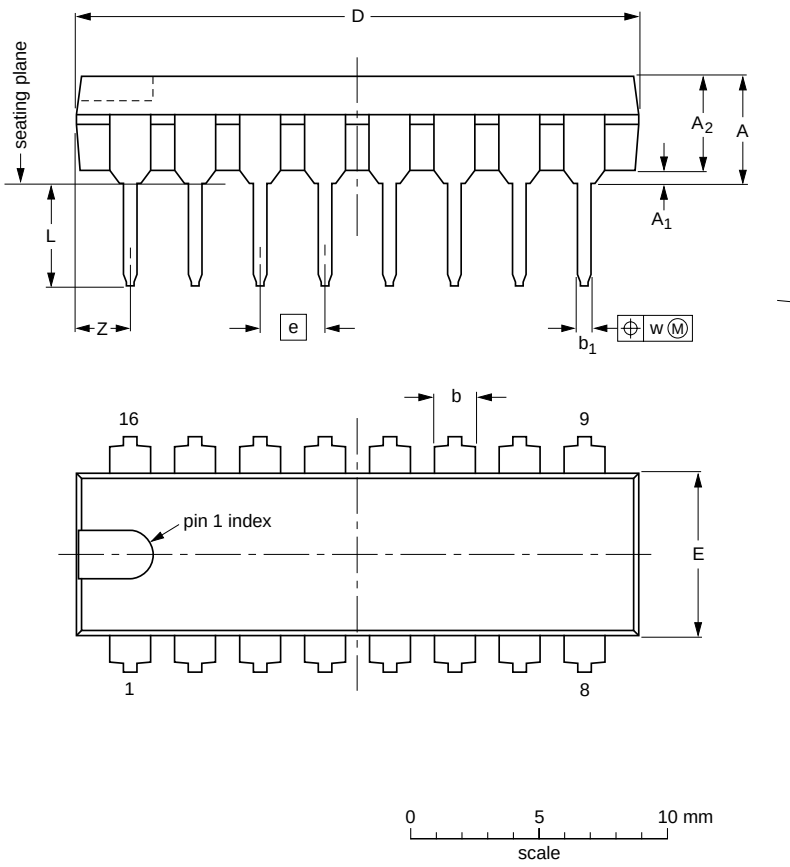
14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 17. Package outline SOT38-1 (DIP16)

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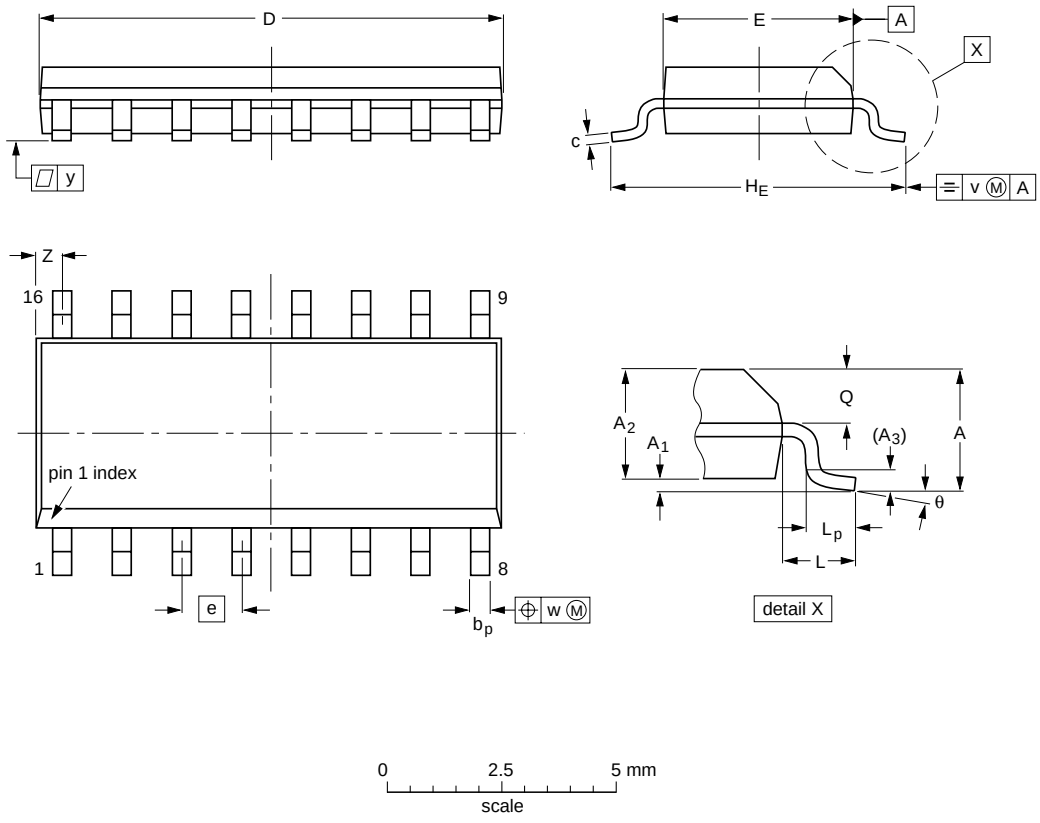
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT109-1 (SO16)

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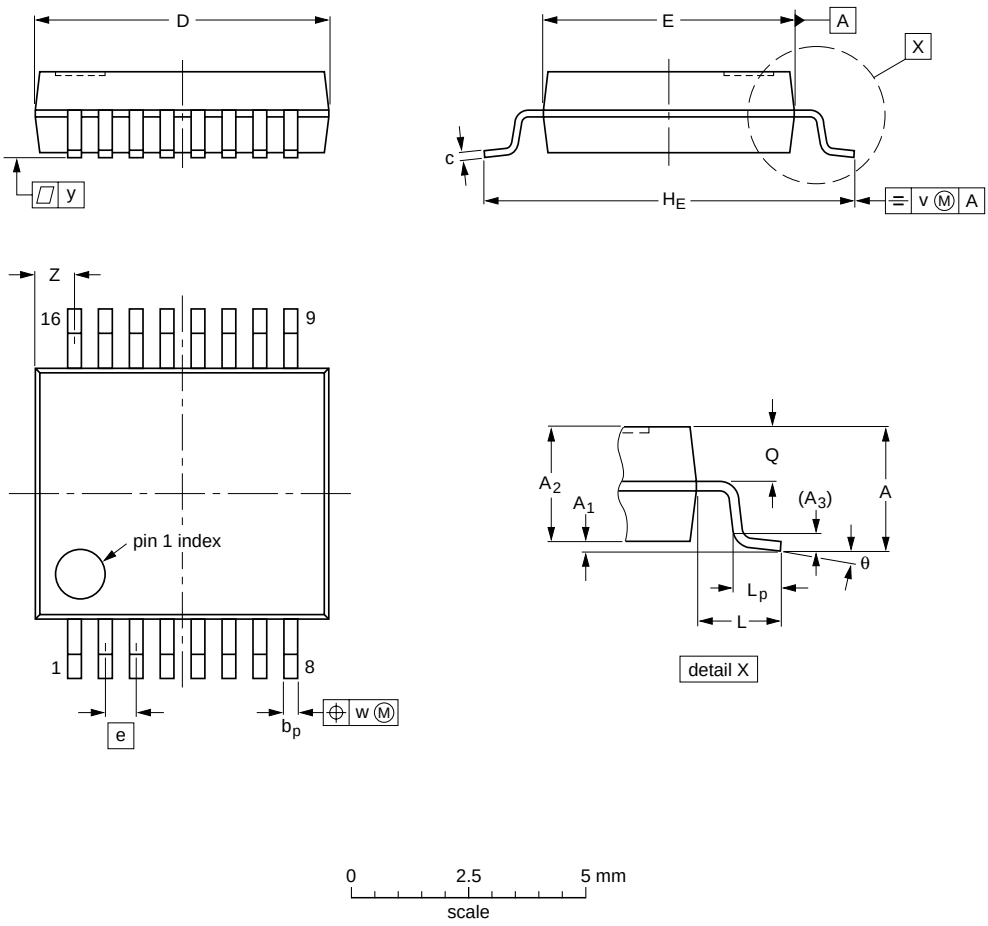
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT338-1 (SSOP16)

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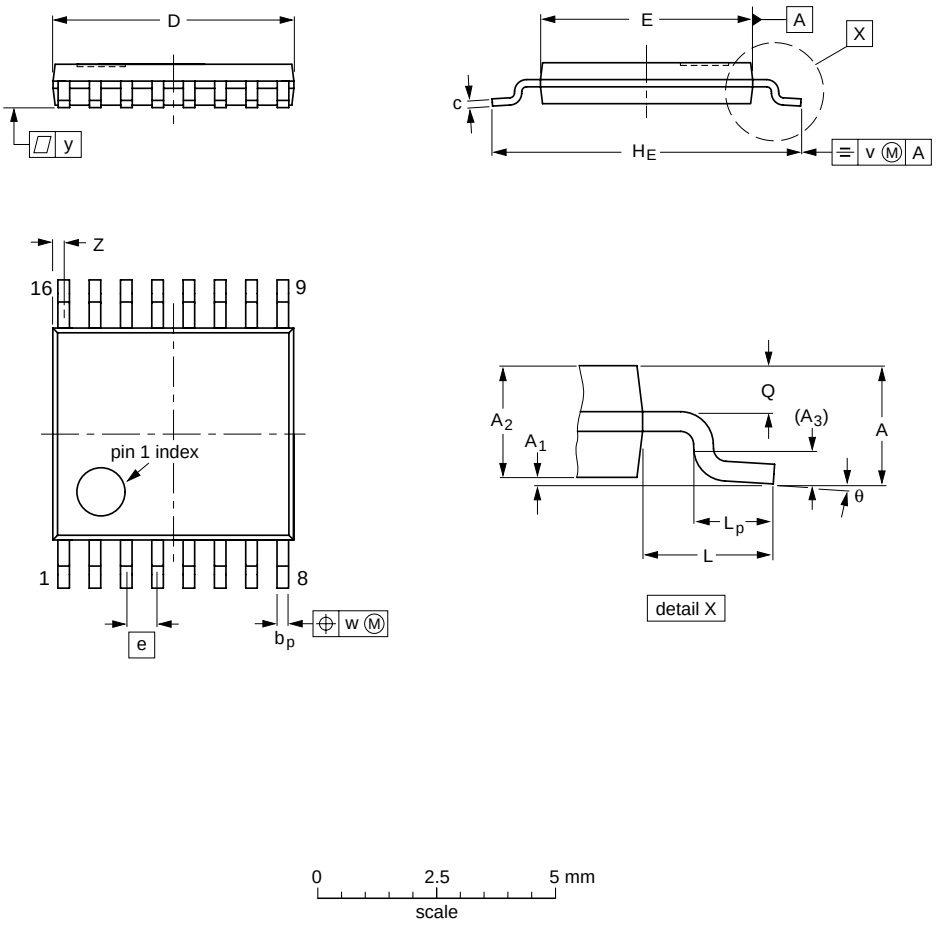
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 20. Package outline SOT403-1 (TSSOP16)

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15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
HEF4051B_4	20050112	Product data sheet	-	9397 750 14377	HEF4051B_CNV_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 4 “Ordering information”, and Section 14 “Package outline”: Modified to include the SOT338-1 (SSOP16) and SOT403-1 (TSSOP16) packages and to remove the SOT74 (CDIP16) package				
HEF4051B_CNV_3	19950101	Product specification	-	-	-

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16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

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