SGS-THOMSON MICROELECTRONICS

T74LS155
T74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

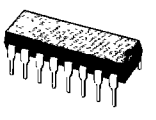
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- COMMON ADDRESS INPUTS
- TRUE OR COMPLEMENT DATA DEMULTIPLEXING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

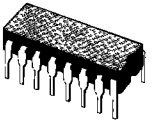
The TTL/MSI T74LS155 and T74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs.

Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs.If the Enable functions are satisfied, one input of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all TTL families.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

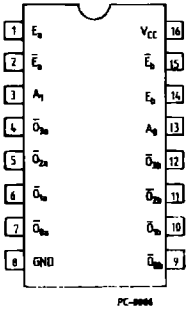
T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

PIN NAMES

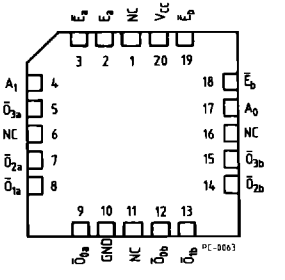
$\overline{A}_0 - \overline{A}_1$	ADDRESS INPUTS
$\overline{E}_a - \overline{E}_b$	ENABLE (active LOW) INPUTS
E_a	ENABLE (active HIGH) INPUT
$\overline{O}_0 - \overline{O}_3$	ACTIVE LOW OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

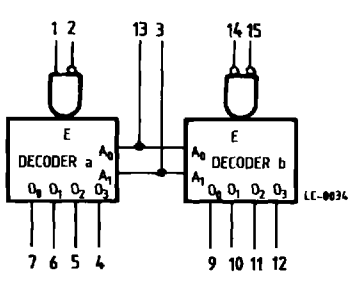


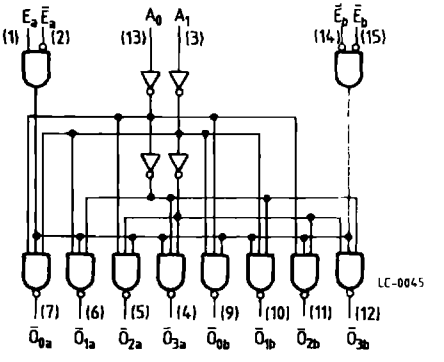
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

ABSOLUTE MAXIMUM RATING

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	LS155	- 0.5 to 15	V
		LS156	- 1.5 to 5.5	V
V_O	Output Voltage, Applied to Output		- 0.5 to 10	V
I_I	Input Current, into Inputs		- 30 to 5	mA
I_O	Output Current, into Outputs		50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS155/156XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/demultiplexer with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs (O_0-O_3). If the Enable requirements of each decoder are not met, all ouputs of that decoder are HIGH.

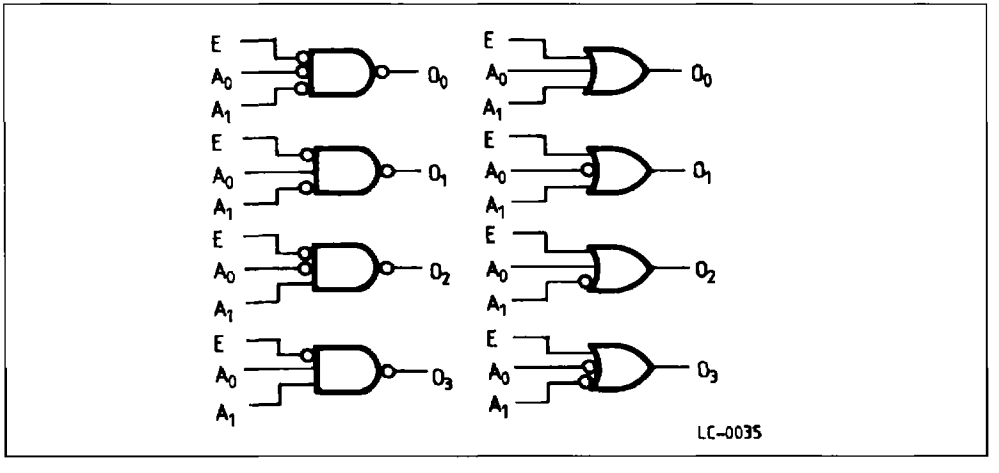
Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($\overline{E}_a \bullet \overline{E}_a$). In demultiplexing applications, Decoder "a" can accepts either true or complemented data by using the $\overline{E}_a$ or $\overline{E}_a$ inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \bullet \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying $\overline{E}_a$ to $\overline{E}_b$ and relabeling the common connection as (A2). The other $\overline{E}_b$ to $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are used in some applications replacing multiple gate functions as shown in Fig. 1. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \bullet (E + \overline{A_0} + A_1) \bullet (E + A_0 + \overline{A_1}) \bullet (E + \overline{A_0} + \overline{A_1})$$

where $E = E_a + \overline{E_a}$; $E = E_b + \overline{E_b}$

Figure 1.



TRUTH TABLE

Address		Enable "a"		Output "a"				Enable "b"		Output "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Treshold Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Treshold Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage for LS155 Only	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
I_{OH}	Output HIGH Current for LS156 Only			100	V_{CC} = MIN, V_{OH} = - 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		6.0	10	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits				Test Conditions		Unit
		LS155		LS156				
		Typ.	Max.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	17 19	26 30	31 34	46 51	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 kΩ (only LS156)	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	10 19	15 30	25 34	40 51	Fig. 3		ns
t_{PLH} t_{PHL}	Propagation Delay, E_a to Output	18 18	27 27	32 32	48 48	Fig. 2		ns

AC WAVEFORMS

Figure 2 .

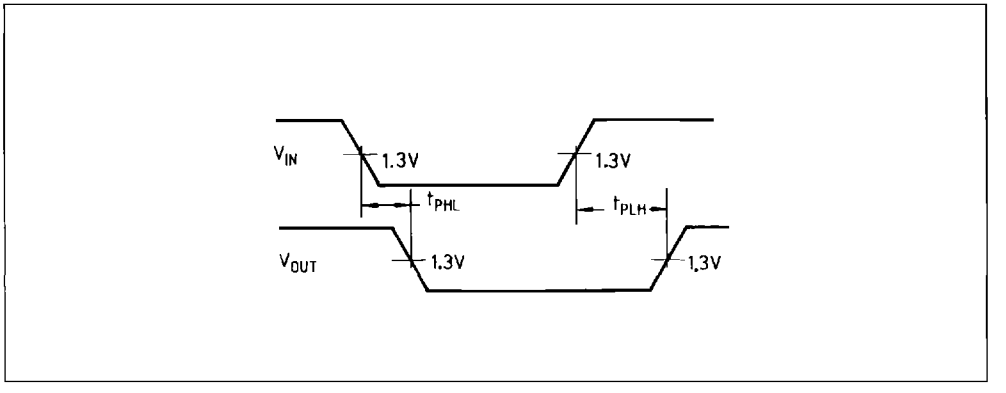
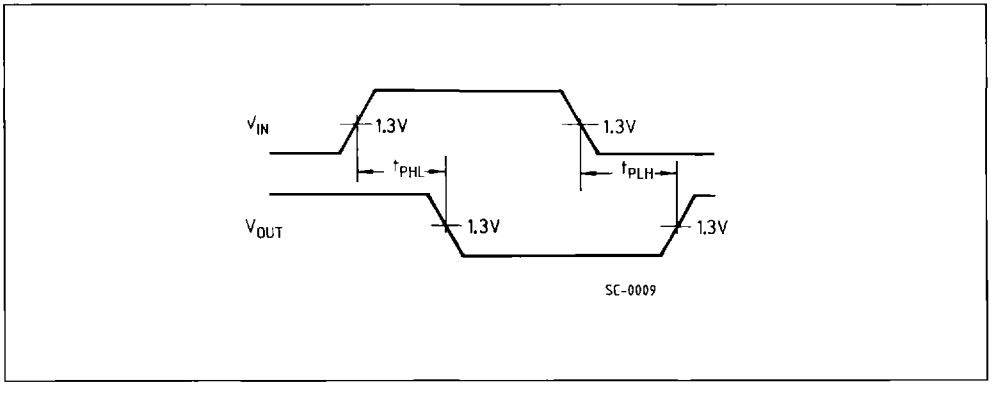


Figure 3.



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