MCP1726

1A, Low-Voltage, Low Quiescent Current LDO Regulator

Features

- 1A Output Current Capability
- Input Operating Voltage Range: 2.3V to 6.0V
- Adjustable Output Voltage Range: 0.8V to 5.0V
- Standard Fixed Output Voltages:
  - 0.8V, 1.2V, 1.8V, 2.5V, 3.0V, 3.3V, 5.0V
- Low Dropout Voltage: 220 mV typical at 1A
- Typical Output Voltage Tolerance: ±0.5%
- Stable with 1.0 µF Ceramic Output Capacitor
- Fast Response to Load Transients
- Low Supply Current: 140 µA (typical)
- Low Shutdown Supply Current: 0.1 µA (typical)
- Adjustable Delay on Power Good Output
- Short-Circuit Current Limiting and Overtemperature Protection
- 3x3 DFN-8 and SOIC-8 Package Options
- Passes Automotive AEC-Q100 Reliability Testing

Applications

- High-Speed Driver Chipset Power
- Networking Backplane Cards
- Notebook Computers
- Network Interface Cards
- Palmtop Computers
- 2.5V to 1.XV Regulators

Description

The MCP1726 is a 1A Low Dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. The MCP1726 comes in fixed or adjustable output voltage versions, with an output voltage range of 0.8V to 5.0V. The 1A output current capability and low output voltage capability make the MCP1726 a good choice for new sub-1.8V output voltage LDO applications that have high current demands.

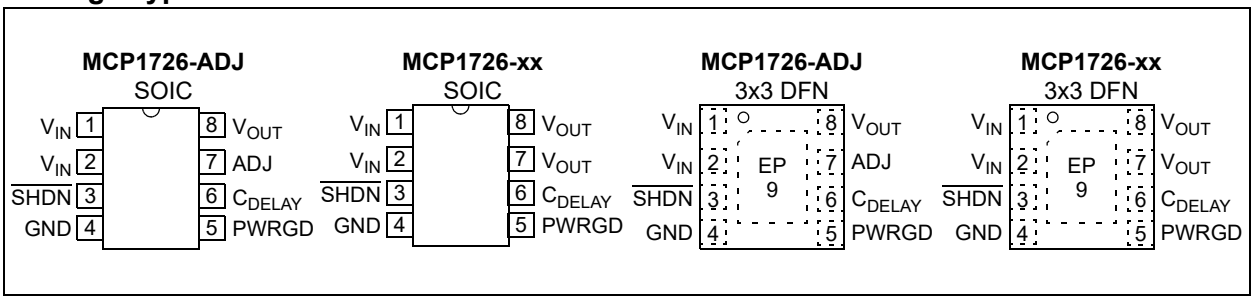
The MCP1726 is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 µF of output capacitance is needed to stabilize the LDO.

Using CMOS construction, the quiescent current consumed by the MCP1726 is typically less than 140 µA over the entire input voltage range, making it attractive for portable computing applications that demand high output current. When the MCP1726 is shut down, the quiescent current is reduced to less than 0.1 µA.

The scaled-down output voltage is internally monitored and a Power Good (PWRGD) output is provided when the output is within 92% of regulation (typical). An external capacitor can be used on the C_{DELAY} pin to adjust the delay from 1 ms to 300 ms.

The overtemperature and short-circuit current limiting provide additional protection for the LDO during system fault conditions.

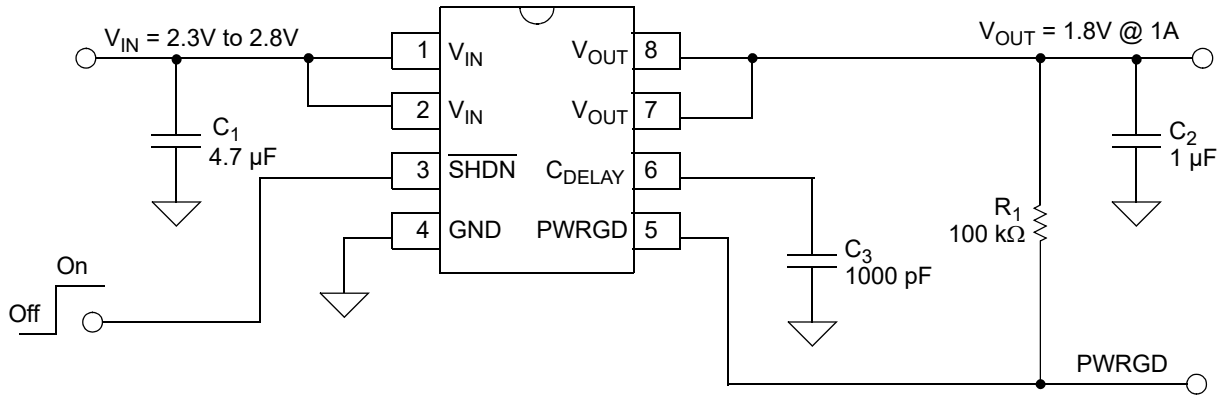
Package Types



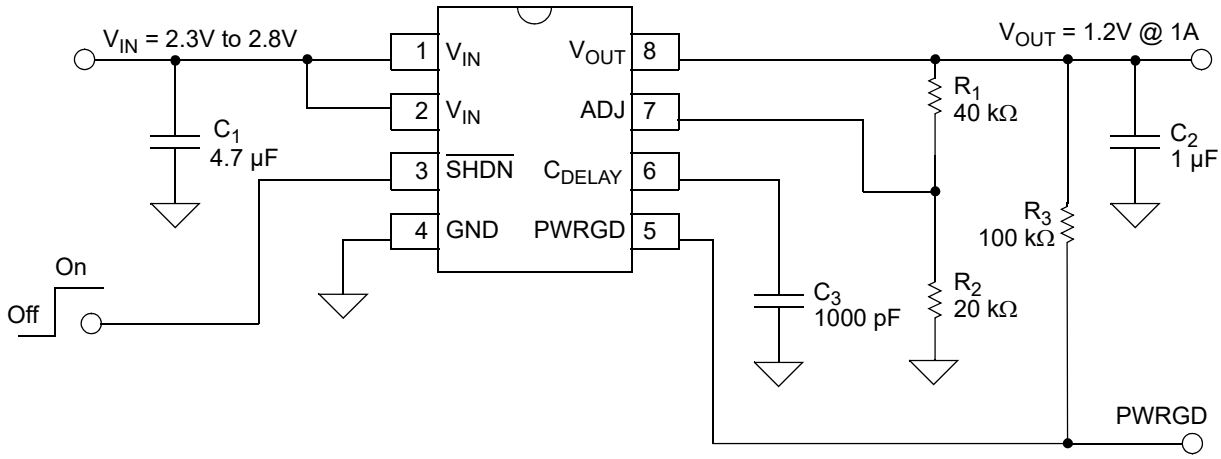
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Typical Application

MCP1726 Fixed Output Voltage

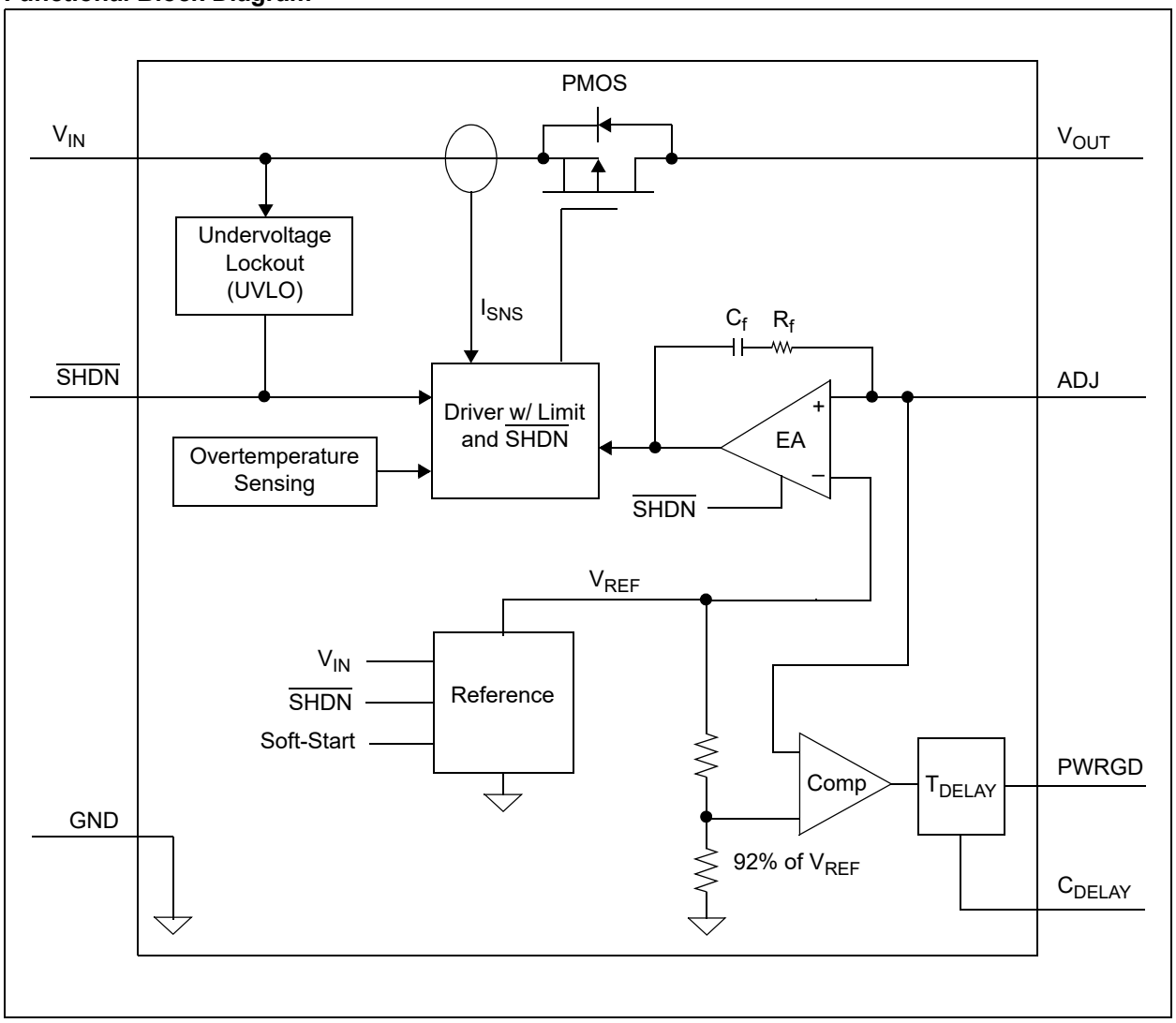


MCP1726 Adjustable Output Voltage



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Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} 6.5V

Maximum Voltage on Any Pin ..(GND – 0.3V) to (V_{DD} + 0.3)V

Maximum Junction Temperature, T_J ..... +150°C

Maximum Power Dissipation..... Internally-Limited (**Note 6**)

Storage Temperature .....-65°C to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{IN} = (V_R + 0.5V) or 2.3V, whichever is greater, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 4.7 µF (X7R Ceramic), T_A = +25°C. **Boldface** type applies for junction temperatures, T_J (**Note 7**), of **-40°C to +125°C**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Operating Voltage	V_{IN}	**2.3**		**6.0**	V	**Note 1**
Input Quiescent Current	I_q	—	140	**220**	µA	I_L = 0 mA, V_{IN} = V_R + 0.5V, V_{OUT} = 0.8V to 5.0V
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	0.1	**3**	µA	$\overline{SHDN}$ = GND
Maximum Output Current	I_{OUT}	**1**	—	—	A	V_{IN} = 2.3V to 6.0V (**Note 1**)
Line Regulation	ΔV_{OUT}/(V_{OUT} x ΔV_{IN})	—	0.05	**0.3**	%/V	(V_R + 0.5)V ≤ V_{IN} ≤ 6V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-1.5**	±0.5	**1.5**	%	I_{OUT} = 1 mA to 1A, V_{IN} = (V_R + 0.6)V (**Note 4**)
Output Short-Circuit Current	I_{OUT_SC}	—	1.7	—	A	V_{IN} = (V_R + 0.5)V, R_{LOAD} < 0.1Ω, Peak Current
Adjust Pin Characteristics						
Adjust Pin Reference Voltage	V_{ADJ}	**0.402**	0.410	**0.418**	V	V_{IN} = 2.3V to V_{IN} = 6.0V, I_{OUT} = 1 mA
Adjust Pin Leakage Current	I_{ADJ}	-10	±0.01	+10	nA	V_{IN} = 6.0V, V_{ADJ} = 0V to 6V
Adjust Temperature Coefficient	TCV_{OUT}	—	40	—	ppm/°C	**Note 3**
Fixed-Output Characteristics						
Voltage Regulation	V_{OUT}	**V_R – 2.5%**	V_R ± 0.5%	**V_R + 2.5%**	V	**Note 2**
Dropout Characteristics						
Dropout Voltage	$V_{IN} - V_{OUT}$	—	220	**500**	mV	I_{OUT} = 1A, $V_{IN(MIN)}$ = 2.3V (**Note 5**)

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} \times ((R_1/R_2) + 1)$. See Figure 4-1.

3: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) \times 10^6/(V_R \times \Delta\text{Temperature})$. $V_{OUT\text{-}HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ is the lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of V_{IN} = V_R + 0.5V.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 125°C can impact device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

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DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{IN} = (V_R + 0.5V) or 2.3V, whichever is greater, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 4.7 µF (X7R Ceramic), T_A = +25°C. **Boldface** type applies for junction temperatures, T_J (**Note 7**), of **-40°C to +125°C**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Good Characteristics						
Input Voltage Operating Range for Valid PWRGD	V_{PWRGD_VIN}	1.0	—	6.0	V	T_A = +25°C
		1.2	—	**6.0**		T_A = -40°C to +125°C
						I_{SINK} = 100 µA
PWRGD Threshold Voltage (Referenced to V_{OUT})	PWRGD_THF	**88**	92	**96**	%	V_{OUT} < 2.5V, Falling Edge
		89	92	**95**	%	V_{OUT} > 2.5V, Falling Edge
	PWRGD_THR	**89**	94	**98**	%	V_{OUT} < 2.5V, Rising Edge
		90	93	**96**	%	V_{OUT} > 2.5V, Rising Edge
PWRGD Output Voltage Low	V_{PWRGD_L}	—	0.2	**0.4**	V	$I_{PWRGD\ SINK}$ = 1.2 mA
PWRGD Leakage	P_{WRGD_LK}	—	0.1	—	µA	V_{PWRGD} = V_{IN} = 6.0V
PWRGD Time Delay	T_{PG}	—	200	—	µs	C_{DELAY} = OPEN
		10	30	**55**	ms	C_{DELAY} = 0.01 µF
		—	300	—	ms	C_{DELAY} = 0.1 µF
Detect Threshold to PWRGD Active Time Delay	$T_{VDET-PWRGD}$	—	170	—	µs	
Shutdown Input						
Logic-High Input	$V_{SHDN-HIGH}$	**45**	—	—	%V_{IN}	V_{IN} = 2.3V to 6.0V
Logic-Low Input	$V_{SHDN-LOW}$	—	—	**15**	%V_{IN}	V_{IN} = 2.3V to 6.0V
$\overline{SHDN}$ Input Leakage Current	$\overline{SHDN}_{ILK}$	**-0.1**	±0.001	**+0.1**	µA	V_{IN} = 6V, $\overline{SHDN}$ = V_{IN}, $\overline{SHDN}$ = GND
AC Performance						
Output Delay from $\overline{SHDN}$	T_{OR}		100		µs	$\overline{SHDN}$ = GND to V_{IN} V_{OUT} = GND to 95% V_R
Output Noise	e_N	—	2.0	—	µV/√Hz	I_{OUT} = 200 mA, f = 1 kHz, C_{OUT} = 1 µF (X7R Ceramic), V_{OUT} = 2.5V
Power Supply Ripple Rejection Ratio	PSRR	—	54	—	dB	f = 100 Hz, C_{OUT} = 10 µF, I_{OUT} = 100 mA, V_{INAC} = 30 mV pk-pk, C_{IN} = 0 µF
Thermal Shutdown Temperature	T_{SD}	—	150	—	°C	I_{OUT} = 100 µA, V_{OUT} = 1.8V, V_{IN} = 2.8V
Thermal Shutdown Hysteresis	ΔT_{SD}	—	10	—	°C	I_{OUT} = 100 µA, V_{OUT} = 1.8V, V_{IN} = 2.8V

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.3V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} \times ((R_1/R_2) + 1)$. See Figure 4-1.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \times 10^6/(V_R \times \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 0.5V$.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 125°C can impact device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{IN} = 2.3V to 6.0V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady State
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L 3x3 DFN	θ_{JA}	—	64	—	°C/W	4-Layer JC51-5 Standard Board with Vias
	θ_{JC}	—	12	—		
Thermal Resistance, 8L SOIC	θ_{JA}	—	163	—	°C/W	4-Layer JC51-7 Standard Board
	θ_{JC}	—	42	—		

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1$ mA and $T_A = +25°C$.

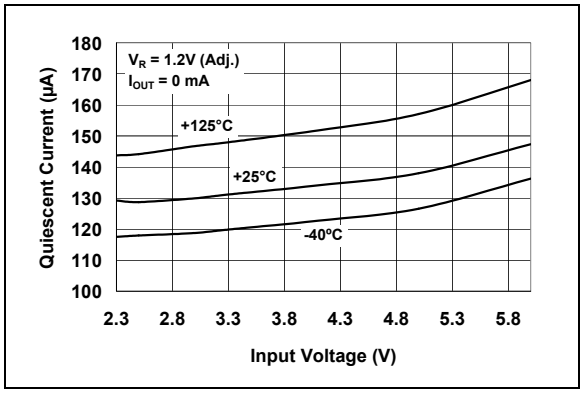


FIGURE 2-1: *Quiescent Current vs. Input Voltage (1.2V Adjustable).*

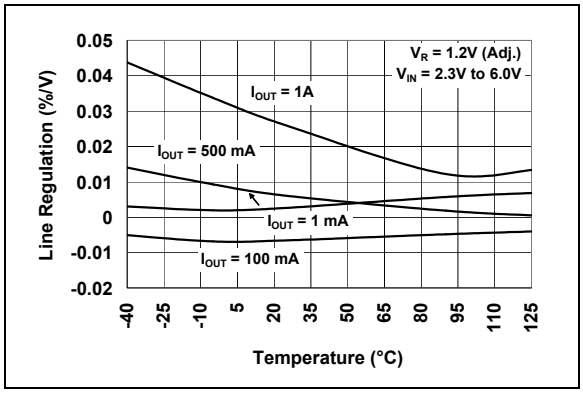


FIGURE 2-4: *Line Regulation vs. Temperature (1.2V Adjustable).*

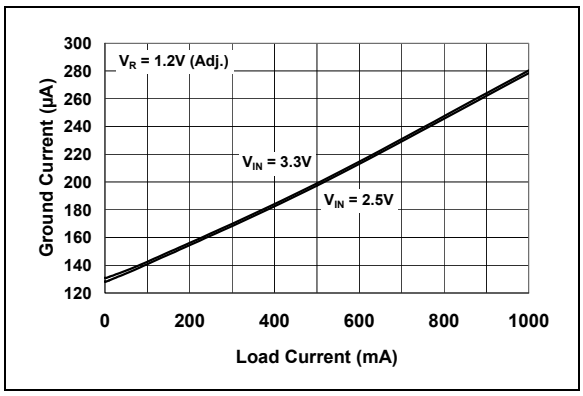


FIGURE 2-2: *Ground Current vs. Load Current (1.2V Adjustable).*

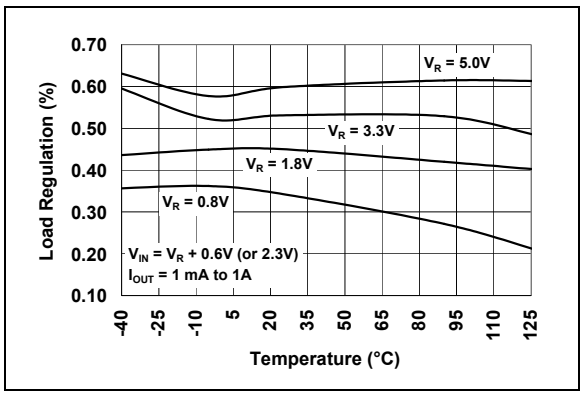


FIGURE 2-5: *Load Regulation vs. Temperature.*

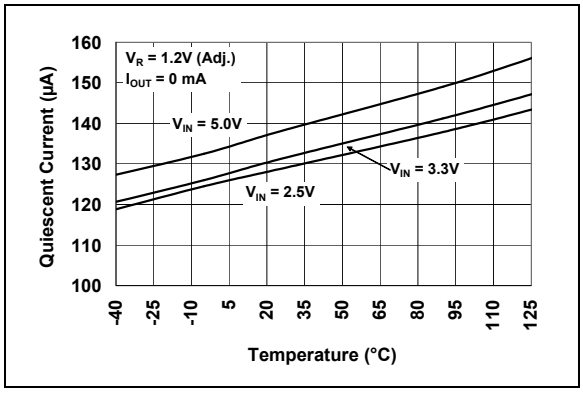


FIGURE 2-3: *Quiescent Current vs. Junction Temperature (1.2V Adjustable).*

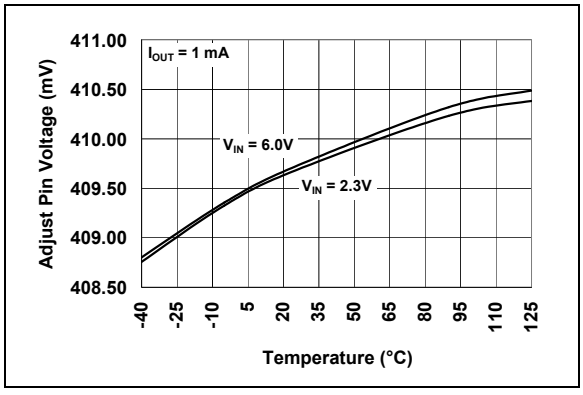


FIGURE 2-6: *Adjust Pin Voltage vs. Temperature.*

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1$ mA and $T_A = +25°C$.

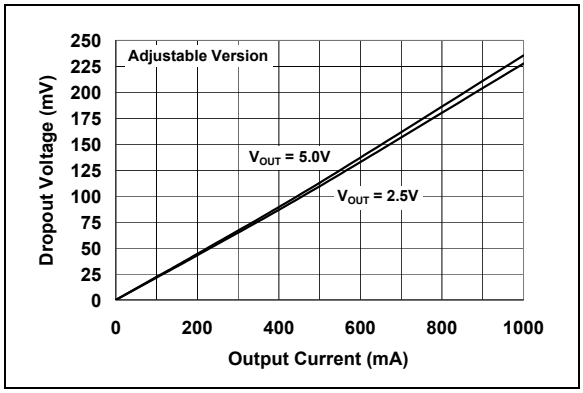


FIGURE 2-7: *Dropout Voltage vs. Output Current (Adjustable Version).*

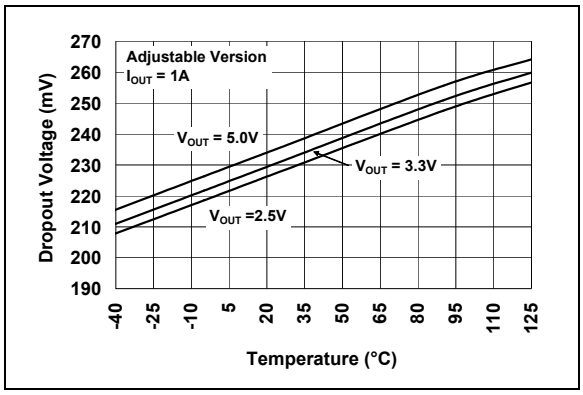


FIGURE 2-8: *Dropout Voltage vs. Temperature (Adjustable Version).*

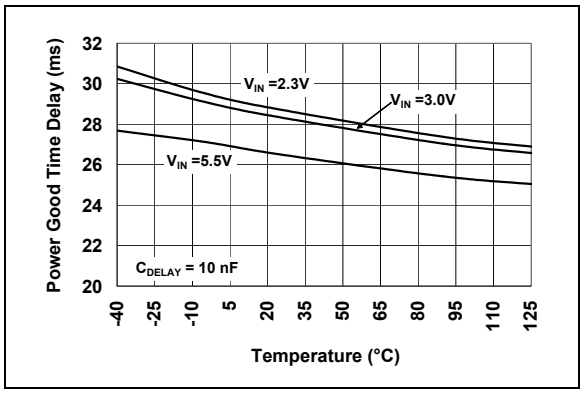


FIGURE 2-9: *Power Good (PWRGD) Time Delay vs. Temperature.*

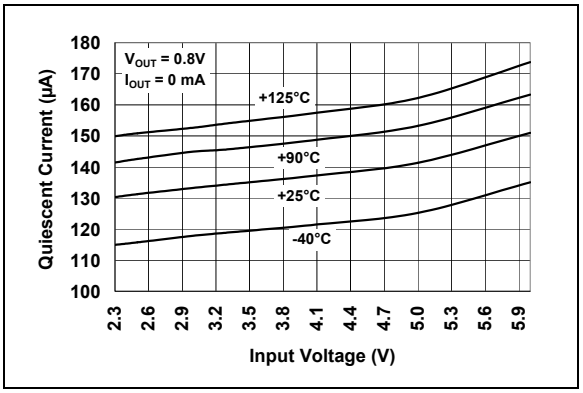


FIGURE 2-10: *Quiescent Current vs. Input Voltage (0.8V Fixed).*

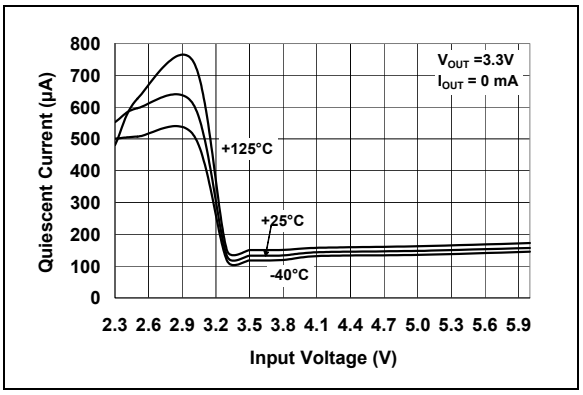


FIGURE 2-11: *Quiescent Current vs. Input Voltage (3.3V Fixed).*

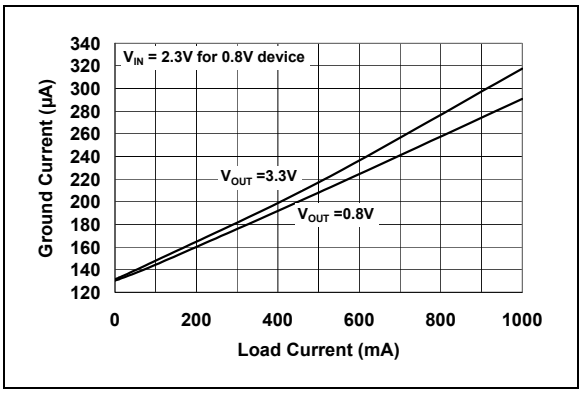


FIGURE 2-12: *Ground Current vs. Load Current.*

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Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, I_{OUT} = 1 mA and T_A = +25°C.

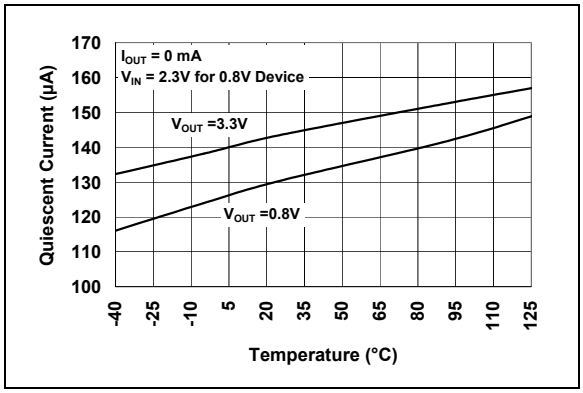


FIGURE 2-13: *Quiescent Current vs. Temperature.*

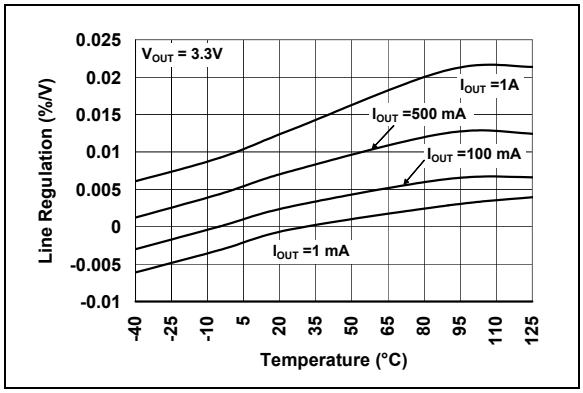


FIGURE 2-16: *Line Regulation vs. Temperature (3.3V Fixed).*

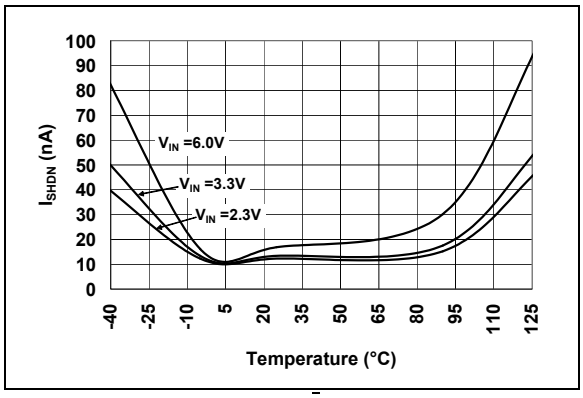


FIGURE 2-14: *$I_{\overline{SHDN}}$ vs. Temperature.*

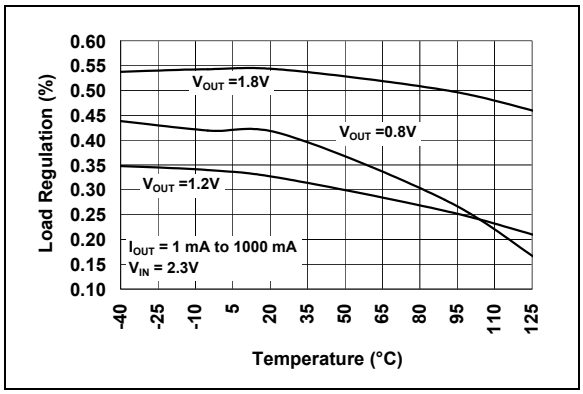


FIGURE 2-17: *Load Regulation vs. Temperature (V_{OUT} < 2.5V Fixed).*

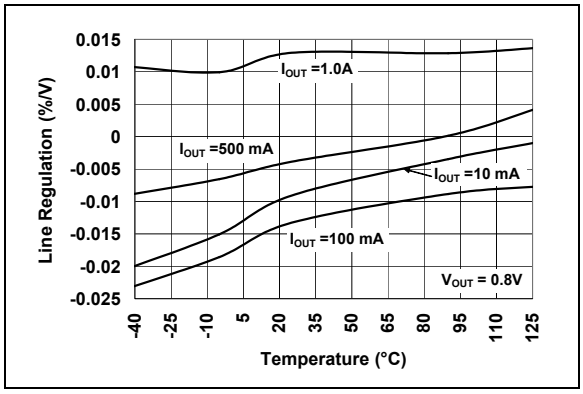


FIGURE 2-15: *Line Regulation vs. Temperature (0.8V Fixed).*

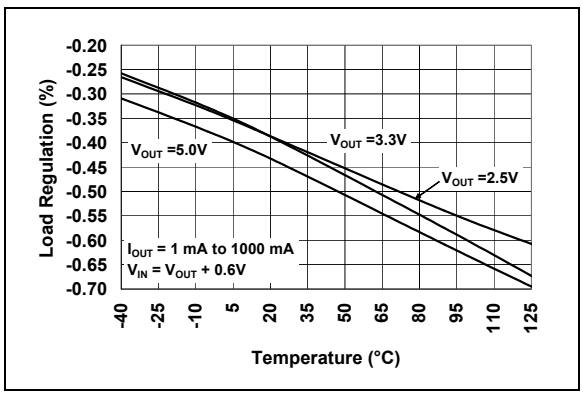


FIGURE 2-18: *Load Regulation vs. Temperature ($V_{OUT} \geq$ 2.5V Fixed).*

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1$ mA and $T_A = +25°C$.

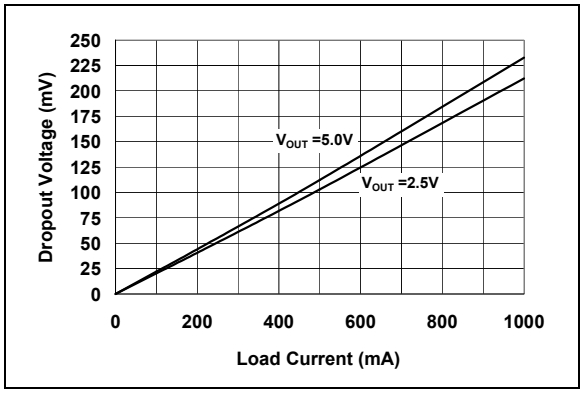


FIGURE 2-19: *Dropout Voltage vs. Load Current.*

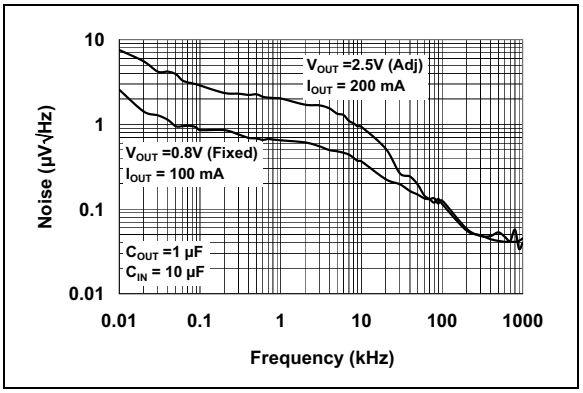


FIGURE 2-22: *Output Noise Voltage Density vs. Frequency.*

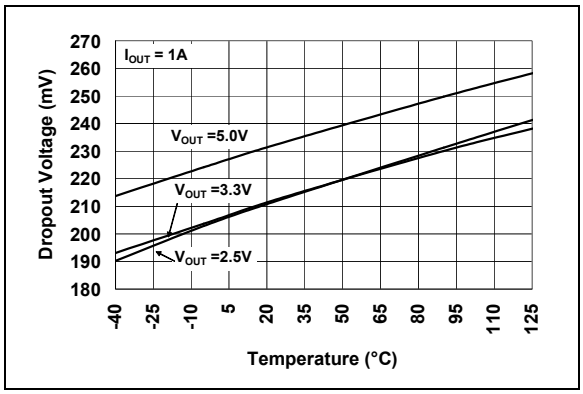


FIGURE 2-20: *Dropout Voltage vs. Temperature.*

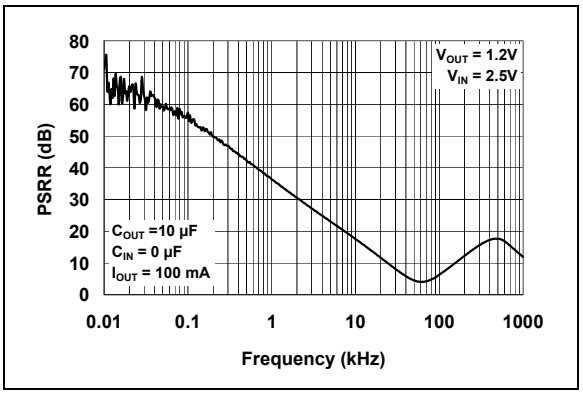


FIGURE 2-23: *Power Supply Ripple Rejection (PSRR) vs. Frequency (V_{OUT} = 1.2V Adjustable).*

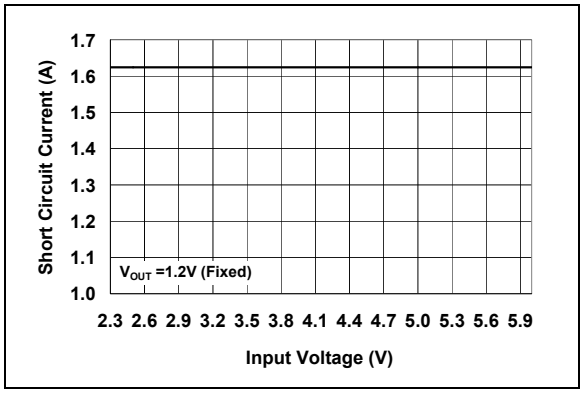


FIGURE 2-21: *Short-Circuit Current vs. Input Voltage.*

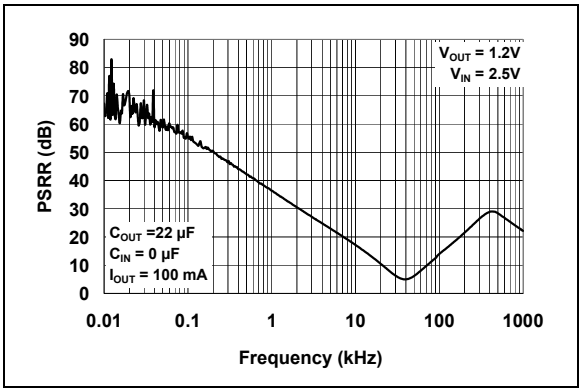


FIGURE 2-24: *Power Supply Ripple Rejection (PSRR) vs. Frequency (V_{OUT} = 1.2V Adjustable).*

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Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, I_{OUT} = 1 mA and T_A = +25°C.

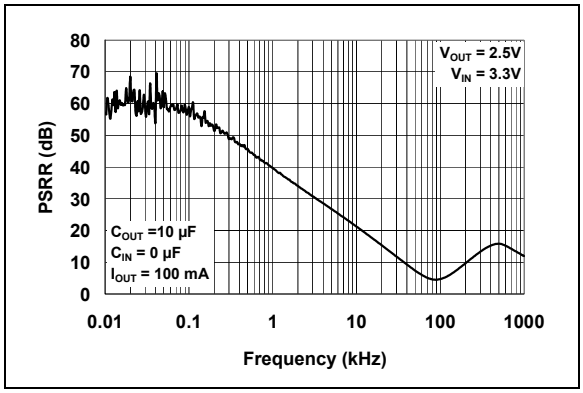


FIGURE 2-25: *Power Supply Ripple Rejection (PSRR) vs. Frequency (V_{OUT} = 2.5V Fixed).*

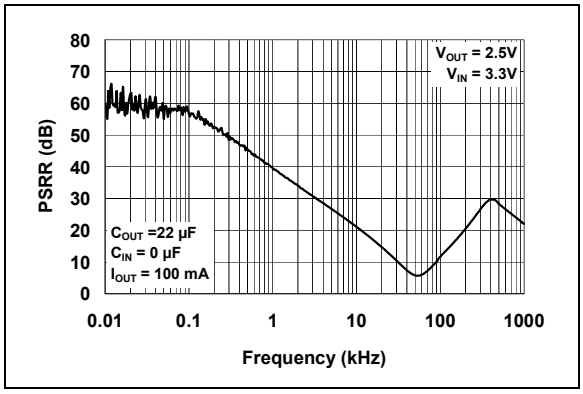


FIGURE 2-26: *Power Supply Ripple Rejection (PSRR) vs. Frequency (V_{OUT} = 2.5V Fixed).*

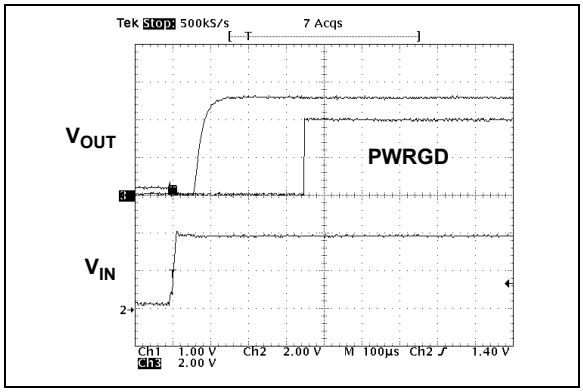


FIGURE 2-27: *2.5V (Adjustable) Start-Up from V_{IN}.*

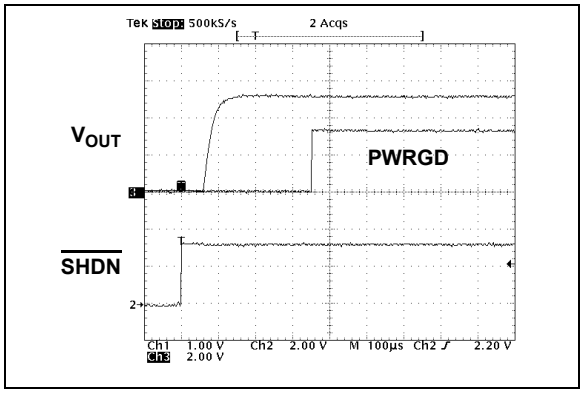


FIGURE 2-28: *2.5V (Adjustable) Start-Up from Shutdown.*

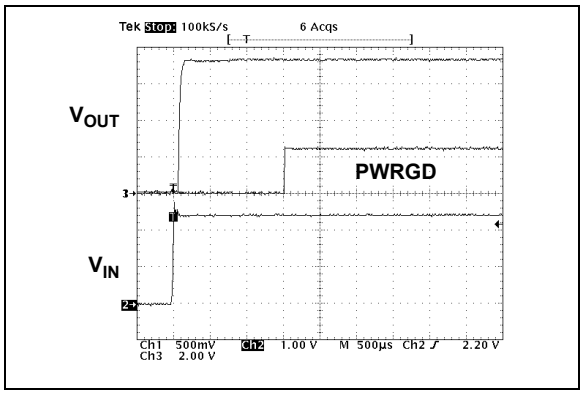


FIGURE 2-29: *Power Good (PWRGD) Timing with C_{BYPASS} of 1000 pF.*

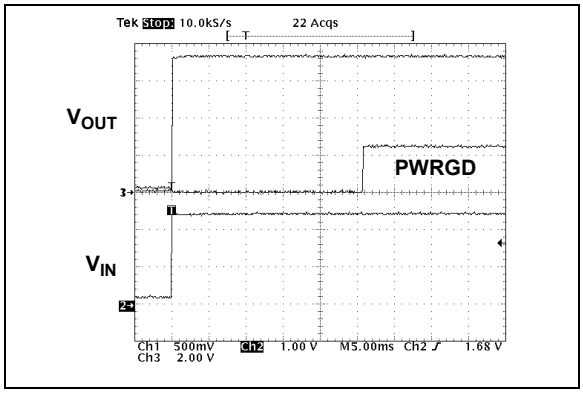


FIGURE 2-30: *Power Good (PWRGD) Timing with C_{BYPASS} of 0.01 µF.*

Note: Unless otherwise indicated, $V_{IN} = V_{OUT} + 0.5V$, I_{OUT} = 1 mA and T_A = +25°C.

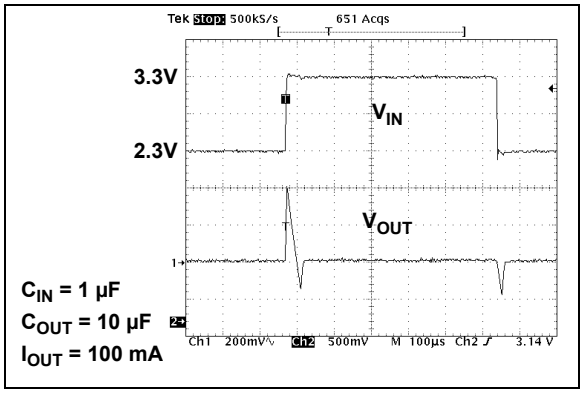


FIGURE 2-31: *Dynamic Line Response (1.2V Fixed).*

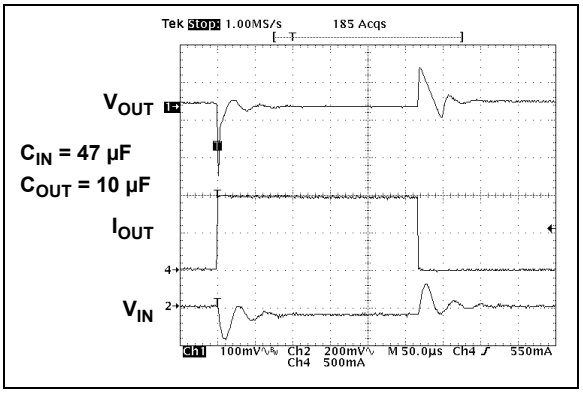


FIGURE 2-33: *Dynamic Load Response (2.5V Fixed, 10 mA to 1000 mA).*

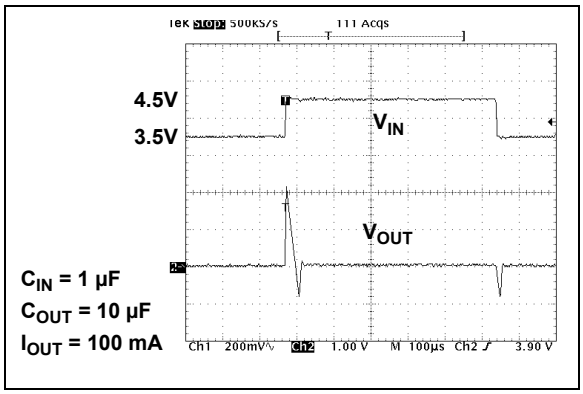


FIGURE 2-32: *Dynamic Line Response (2.5V Fixed).*

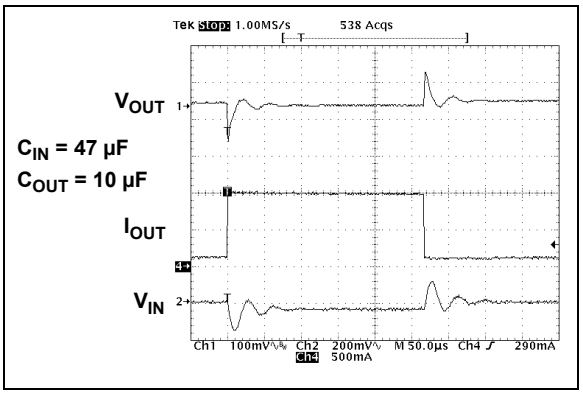


FIGURE 2-34: *Dynamic Load Response (2.5V Fixed, 100 mA to 1000 mA).*

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3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Fixed Output		Adjustable Output		Name	Description
3x3 DFN	SOIC	3x3 DFN	SOIC		
1	1	1	1	V_{IN}	Input Voltage Supply
2	2	2	2	V_{IN}	Input Voltage Supply
3	3	3	3	$\overline{SHDN}$	Shutdown Control Input (active-low)
4	4	4	4	GND	Ground
5	5	5	5	PWRGD	Power Good Output
6	6	6	6	C_{DELAY}	Power Good Delay Set-Point Input
—	—	7	7	ADJ	Output Voltage Sense Input (adjustable version)
7	7	—	—	V_{OUT}	Regulated Output Voltage
8	8	8	8	V_{OUT}	Regulated Output Voltage
9	—	9	—	EP	Exposed Pad

3.1 Input Voltage Supply (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications.

3.2 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.1 µA.

3.3 Ground (GND)

Connect the GND pin of the LDO to a quiet circuit ground. This will help the LDO power supply rejection ratio and noise performance. The ground pin of the LDO only conducts the quiescent current of the LDO (typically 140 µA), so a heavy trace is not required.

3.4 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD output has a typical hysteresis value of 2% for the adjustable voltage version and for voltage outputs less than 2.5V. For fixed output voltage versions greater than 2.5V, the hysteresis is 0.7%. The PWRGD output is delayed on power-up by 200 µs (typical, no capacitance on the C_{DELAY} pin). This delay time is controlled by the C_{DELAY} pin.

3.5 Power Good Delay Set-Point Input (C_{DELAY})

The C_{DELAY} input sets the power-up delay time for the PWRGD output. By connecting an external capacitor from the C_{DELAY} pin to ground, the delay times for the PWRGD output can be adjusted from 200 µs (no capacitance) to 300 ms (0.1 µF capacitor). This allows for the optimal setting of the system reset time.

3.6 Output Voltage Sense Input (ADJ)

The output voltage adjust pin (ADJ) for the adjustable output voltage version of the MCP1726 allows the user to set the output voltage of the LDO by using two external resistors. The adjust pin voltage is 0.41V (typical).

3.7 Regulated Output Voltage (V_{OUT})

The V_{OUT} pin(s) is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 µF is required for LDO stability. The MCP1726 is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See **Section 4.3 "Output Capacitor"** for output capacitor selection guidance.

3.8 Exposed Pad (EP)

The 3x3 DFN package has an exposed pad on the bottom of the package. This pad should be soldered to the Printed Circuit Board (PCB) to aid in the removal of heat from the package during operation. The exposed pad is at the ground potential of the LDO.

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4.0 DEVICE OVERVIEW

The MCP1726 is a high output current, Low Dropout (LDO) voltage regulator with an adjustable delay power-good output and shutdown control input. The low dropout voltage of 220 mV at 1A of current makes it ideal for battery-powered applications. Unlike other high output current LDOs, the MCP1726 only draws 220 µA of quiescent current at full load.

4.1 LDO Output Voltage

The MCP1726 LDO is available with either a fixed output voltage or an adjustable output voltage. The allowable output voltage range is 0.8V to 5.5V for both versions.

4.1.1 ADJUSTABLE INPUT

The adjustable version of the MCP1726 uses the ADJ pin (pin 7) to get the output voltage feedback for output voltage regulation. This allows the user to set the output voltage of the device with two external resistors. The nominal voltage for ADJ is 0.41V.

Figure 4-1 shows the adjustable version of the MCP1726. Resistors R_1 and R_2 form the resistor divider network necessary to set the output voltage. With this configuration, the equation for setting V_{OUT} is:

EQUATION 4-1:

$$V_{OUT} = V_{ADJ}\left(\frac{R_1 + R_2}{R_2}\right)$$

V_{OUT} = LDO Output Voltage
V_{ADJ} = ADJ Pin Voltage (typically 0.41V)

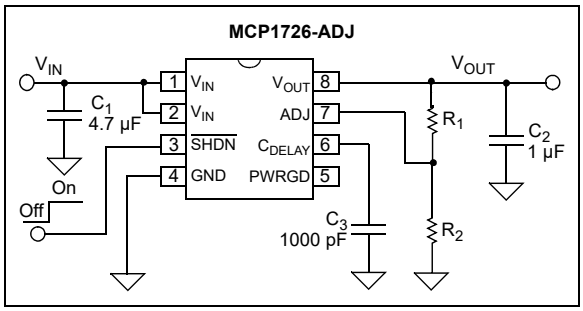


FIGURE 4-1: *Typical Adjustable Output Voltage Application Circuit.*

The range of allowable resistance values for resistor R_2 is 10 kΩ to 200 kΩ. Solving the equation for R_1 yields the following equation:

EQUATION 4-2:

$$R_1 = R_2\left(\frac{V_{OUT} - V_{ADJ}}{V_{ADJ}}\right)$$

V_{OUT} = LDO Output Voltage
V_{ADJ} = ADJ Pin Voltage (typically 0.41V)

4.2 Output Current and Current Limiting

The MCP1726 LDO is tested and ensured to supply a minimum of 1A of output current. The MCP1726 has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1726 also incorporates an output current limit. If the output voltage falls below 0.7V due to an overload condition (usually represents a shorted load condition), the output current is limited to 1.7A (typical). If the overload condition is a soft overload, the MCP1726 will supply higher load currents of up to 3A. The MCP1726 should not be operated in this condition continuously as it may result in failure of the device. However, this does allow for device usage in applications that have higher pulsed load currents having an average output current value of 1A or less.

Output overload conditions may also result in an overtemperature shutdown of the device. If the junction temperature rises above 150°C, the LDO will shut down the output voltage. See **Section 4.9 "Overtemperature Protection"** for more information on overtemperature shutdown.

4.3 Output Capacitor

The MCP1726 requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor must be no greater than 2Ω. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 mΩ.

Larger LDO output capacitors can be used with the MCP1726 to improve dynamic performance and power supply ripple rejection performance. A maximum of 22 µF is recommended. Aluminum-electrolytic capacitors are not recommended for low-temperature applications of < -25°C.

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4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent (or higher) value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.5 Power Good Output (PWRGD)

The PWRGD output is used to indicate when the output voltage of the LDO is within 92% (typical value, see the DC Characteristics table for Min/Max specs) of its nominal regulation value.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as T_{PG} in the DC Characteristics table). The power good time delay is adjustable via the C_{DELAY} pin of the LDO (see **Section 4.6 "C_{DELAY} Input"**). By placing a capacitor from the C_{DELAY} pin to ground, the power good time delay can be adjusted from 200 µs (no capacitance) to 300 ms (0.1 µF capacitor). After the time delay period, the PWRGD output will go high, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 170 µs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-2 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{SHDN}$ input, the power good output is pulled low immediately, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-3.

The power good output is an open-drain output that can be pulled up to any voltage that is equal to or less than the LDO input voltage. This output is capable of sinking 1.2 mA (V_{PWRGD} < 0.4V maximum).

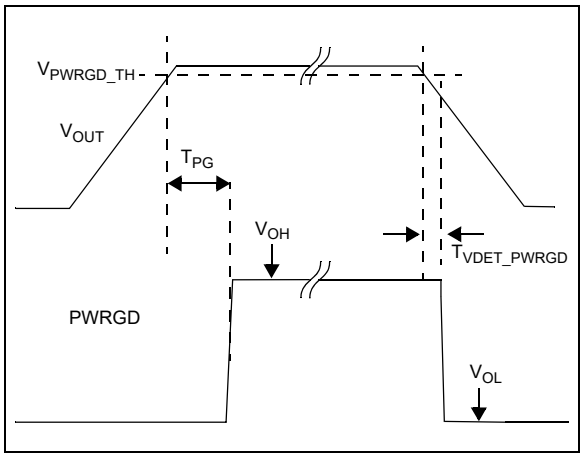


FIGURE 4-2: *Power Good Timing.*

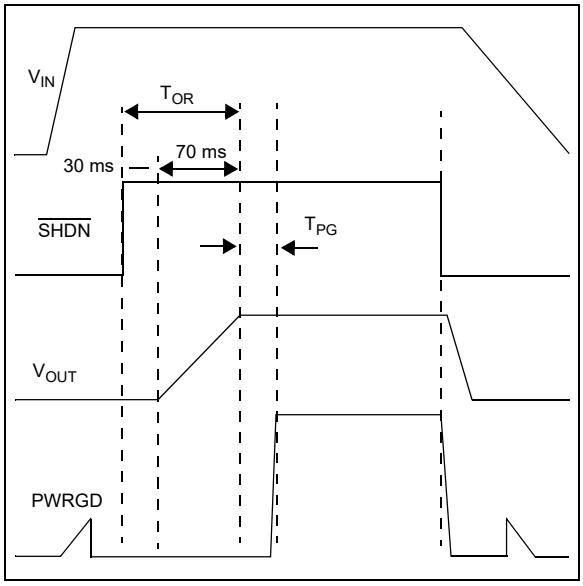


FIGURE 4-3: *Power Good Timing from Shutdown.*

4.6 C_{DELAY} Input

The C_{DELAY} input is used to provide the power-up delay timing for the power good output, as discussed in the previous section. By adding a capacitor from the C_{DELAY} pin to ground, the PWRGD power-up time delay can be adjusted from 200 µs (no capacitance on C_{DELAY}) to 300 ms (0.1 µF of capacitance on C_{DELAY}). See the DC Characteristics table for C_{DELAY} timing tolerances.

Once the power good threshold (rising) has been reached, the C_{DELAY} pin charges the external capacitor to 1.5V (typical; this level can vary between 1.4V and 1.75V across the input voltage range of the part). The PWRGD output will transition high when the C_{DELAY} pin voltage has charged to 0.42V. If the output falls below the power good threshold limit during the charging time between 0.0V and 0.42V on the C_{DELAY} pin, the C_{DELAY} pin voltage will be pulled to ground, thus resetting the timer. The C_{DELAY} pin will be held low until the output voltage of the LDO has once again risen above the power good rising threshold. A timing diagram showing C_{DELAY}, PWRGD and V_{OUT} is shown in Figure 4-4.

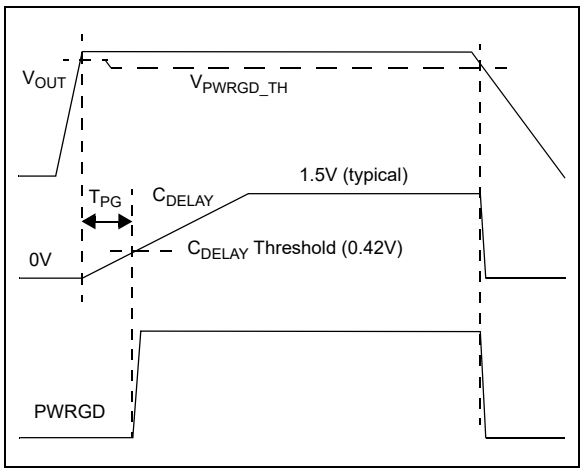


FIGURE 4-4: *C_{DELAY} and PWRGD Timing Diagram.*

4.7 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The typical value of this shutdown threshold is 30% of V_{IN}, with minimum and maximum limits over the entire operating temperature range of 45% and 15%, respectively.

The $\overline{SHDN}$ input will ignore low-going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO will enter Shutdown mode. This small bit of filtering helps reject any system noise spikes on the shutdown input signal.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 30 µs delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the 30 µs delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 30 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the LDO output being in regulation is typically 100 µs. See Figure 4-5 for a timing diagram of the $\overline{SHDN}$ input.

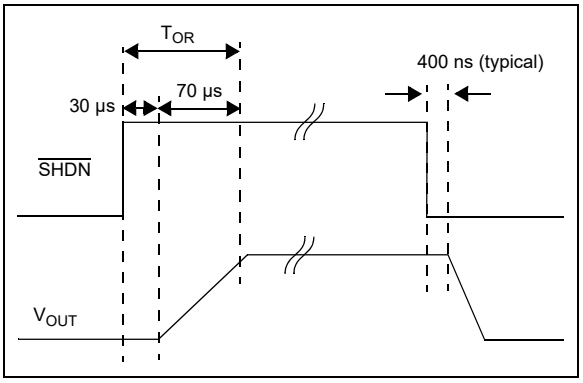


FIGURE 4-5: *Shutdown Input Timing Diagram.*

4.8 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 0.5V differential applied. The MCP1726 LDO has a very low dropout voltage specification of 220 mV (typical) at 1A of output current. See the DC Characteristics table for maximum dropout voltage specifications.

The MCP1726 LDO operates across an input voltage range of 2.3V to 6.0V and incorporates input Undervoltage Lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 2.18V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output will remain on until the input voltage level reaches 2.04V (typical).

Since the MCP1726 LDO Undervoltage Lockout activates at 2.04V as the input voltage is falling, the dropout voltage specification does not apply for output voltages that are less than 1.9V.

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 2.3V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

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4.9 Overtemperature Protection

The MCP1726 LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately 150°C. If the LDO junction temperature does reach 150°C, the LDO output will be turned off until the junction temperature cools to approximately 140°C, at which point the LDO output will automatically resume normal operation. If the internal power dissipation continues to be excessive, the device will shut off again. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See **Section 5.0 "Application Circuits/Issues"** for more information on LDO power dissipation and junction temperature.

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5.0 APPLICATION CIRCUITS/ ISSUES

5.1 Typical Application

The MCP1726 is used for applications that require high LDO output current and a power good output.

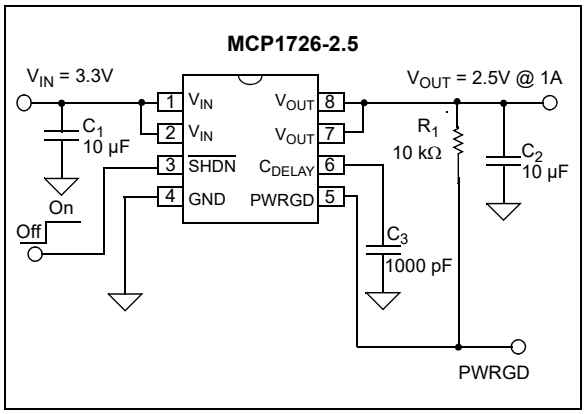


FIGURE 5-1: *Typical Application Circuit.*

5.1.1 APPLICATION CONDITIONS

Package Type	=	8-Lead 3x3 DFN
Input Voltage Range	=	3.3V ± 10%
V_{IN} maximum	=	3.63V
V_{IN} minimum	=	2.97V
V_{OUT} typical	=	2.5V
I_{OUT}	=	1.0A maximum

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1726 is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

P_{LDO}	=	LDO Pass device internal power dissipation
$V_{IN(MAX)}$	=	Maximum input voltage
$V_{OUT(MIN)}$	=	LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1726 as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

$P_{I(GND)}$	=	Power dissipation due to the quiescent current of the LDO
$V_{IN(MAX)}$	=	Maximum input voltage
I_{VIN}	=	Current flowing in the V_{IN} pin with no LDO output current (LDO quiescent current)

The total power dissipated within the MCP1726 is the sum of the power dissipated in the LDO pass device and the $P_{I(GND)}$ term. Because of the CMOS construction, the typical I_{GND} for the MCP1726 is 140 µA. Operating at a maximum of 3.63V results in a power dissipation of 0.51 mW. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1726 is +125°C. To estimate the internal junction temperature of the MCP1726, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction to ambient for the 3x3 DFN package is estimated at 64°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction-to-ambient
$T_{A(MAX)}$	=	Maximum ambient temperature

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The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$ = Maximum device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
T_A = Ambient temperature

5.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 3x3 DFN

Input Voltage

V_{IN} = 3.3V ± 10%

LDO Output Voltage and Current

V_{OUT} = 2.5V

I_{OUT} = 1.0A

Maximum Ambient Temperature

$T_{A(MAX)}$ = 70°C

Internal Power Dissipation

$P_{LDO(MAX)} = [V_{IN(MAX)} - V_{OUT(MIN)}] \times I_{OUT(MAX)}$

$P_{LDO} = [(3.3V \times 1.1) - (0.975 \times 2.5V)] \times 1.0A$

P_{LDO} = 1.192W

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7 “High Effective Thermal Conductivity Test Board for Leaded Surface-Mount Packages”. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *“A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”* (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$

$T_{J(RISE)}$ = 1.192W x 64.0°C/W

$T_{J(RISE)}$ = 76.3°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$T_J = T_{JRISE} + T_{A(MAX)}$
$T_J = 76.3°C + 70.0°C$
$T_J = 146.3°C$

As can be seen from the result, this application will be operating above the maximum operating junction temperature of 125°C. The PCB layout for this application is very important, as it has a significant impact on the junction-to-ambient thermal resistance ($R\theta_{JA}$) of the 3x3 DFN package, which is very important in this application.

Maximum Package Power Dissipation at 70°C Ambient Temperature

3x3 DFN (64°C/W $R\theta_{JA}$)
$P_{D(MAX)} = (125°C – 70°C)/64°C/W$
$P_{D(MAX)} = 0.86W$
8LD SOIC (163°C/W $R\theta_{JA}$)
$P_{D(MAX)} = (125°C – 70°C)/163°C/W$
$P_{D(MAX)} = 0.337W$

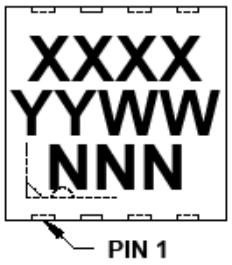
From this table you can see the difference in maximum allowable power dissipation between the 3x3 DFN package and the 8-pin SOIC package. This difference is due to the exposed metal tab on the bottom of the DFN package. The exposed tab of the DFN package provides a very good thermal path from the die of the LDO to the PCB. The PCB then acts like a heat sink, providing more area to distribute the heat generated by the LDO. When the PCB heat sink area is used, the $R\theta_{JA}$ should be replaced by $R\theta_{JC}$ plus $R\theta_{HS}$, where $R\theta_{HS}$ is the PCB copper area heat sink thermal resistance. This will allow for higher maximum power dissipation compared to the free-air power dissipation calculated using $R\theta_{JA}$.

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6.0 PACKAGING INFORMATION

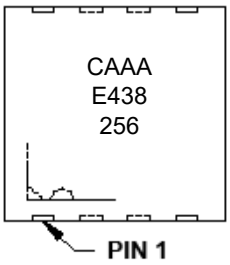
6.1 Package Marking Information

8-Lead DFN (3x3x0.9 mm)

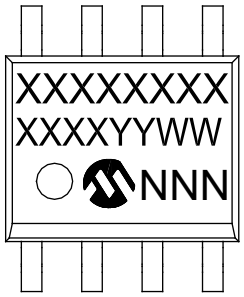


Voltage Option	Code
0.8V	CAAA
1.2V	CAAB
1.8V	CAAC
2.5V	CAAD
3.0V	CAAE
3.3V	CAAF
5.0V	CAAG
Adj	AADJ

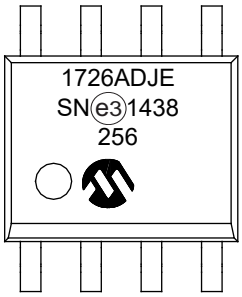
Example



8-Lead SOIC (3.90 mm)



Example

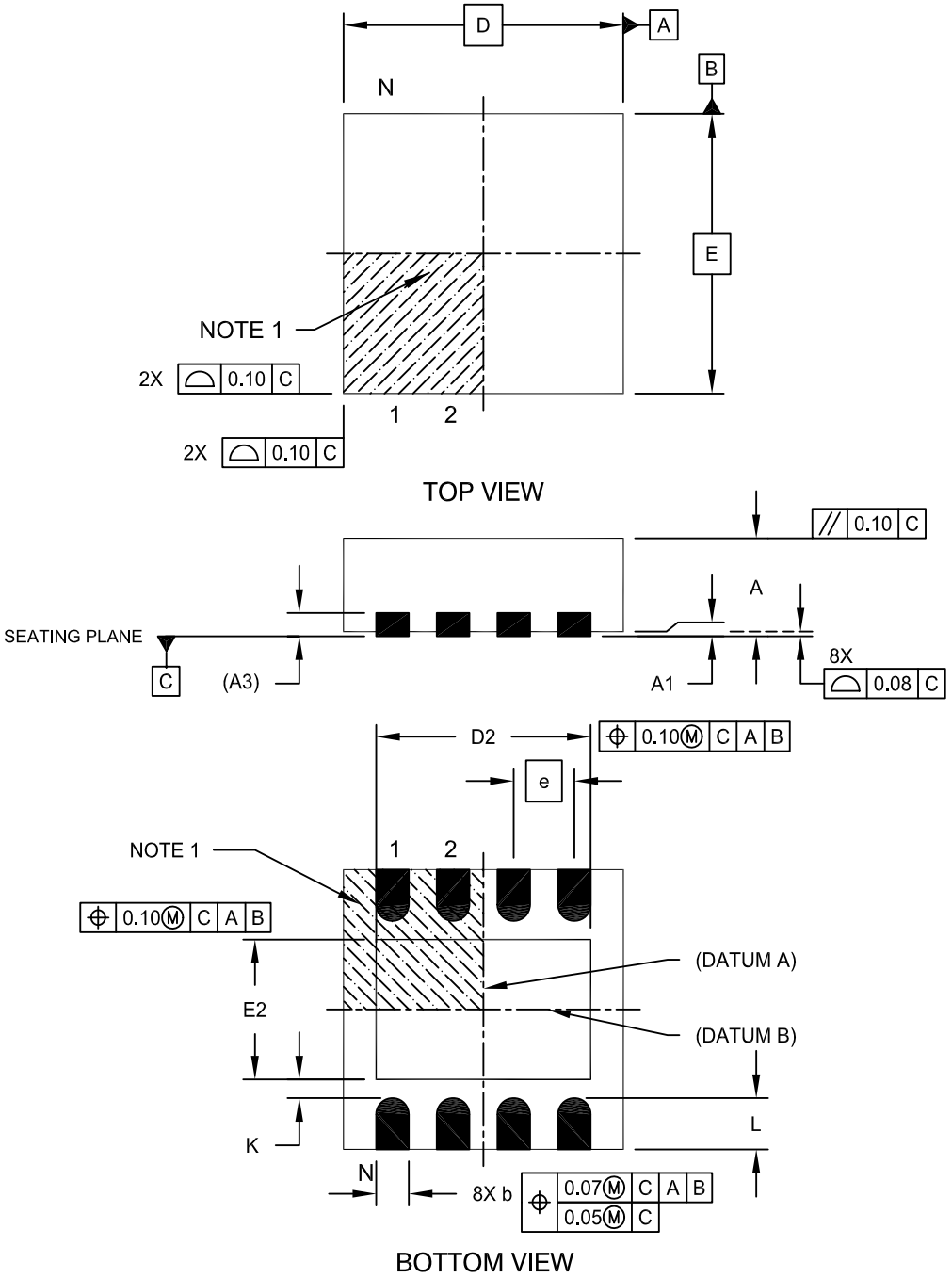


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

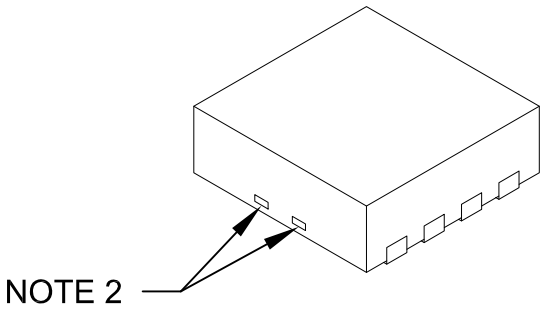


Microchip Technology Drawing No. C04-062C Sheet 1 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

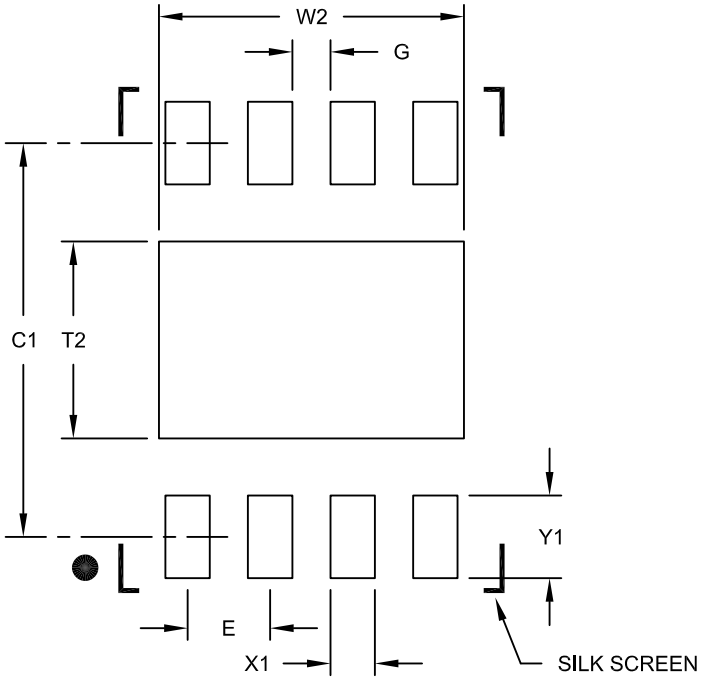
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

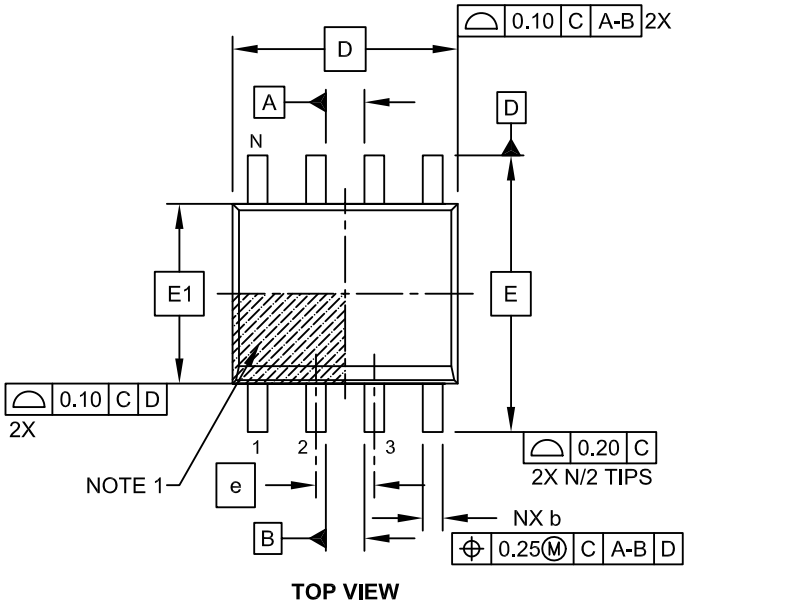
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

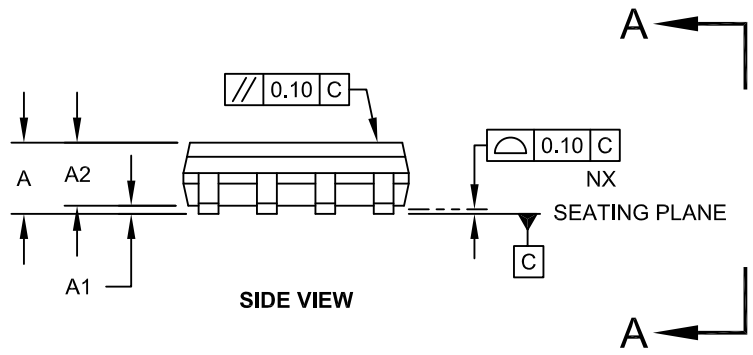
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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

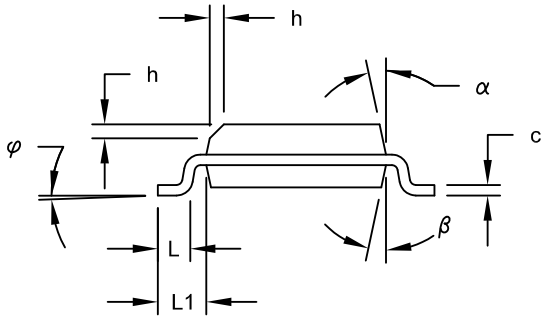
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

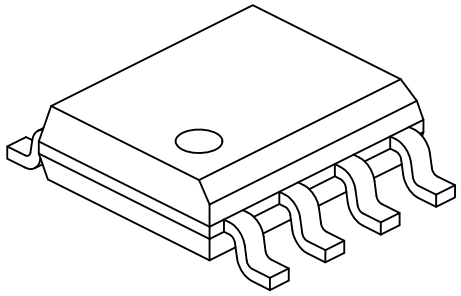


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

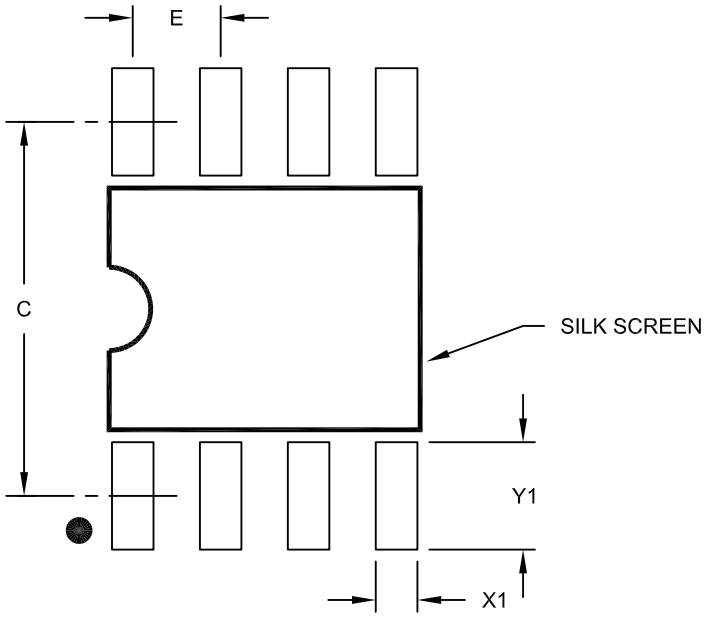
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision E (January 2021)

The following is the list of modifications:

1. Added Automotive Qualification-related information in the **Features** and **Product Identification System** sections.

Revision D (September 2014)

The following is the list of modifications:

1. Corrected the typical output voltage tolerance in the **Features** section to match the stated value in the DC Characteristics table.
2. Corrected illustrations of package markings in **Section 6.0, Packaging Information**.
3. Minor typographical changes.

Revision C (August 2007)

The following is the list of modifications:

1. Added 3.0V option to **Section 6.1, Package Marking Information**.
2. Updated package outline drawings.
3. Added 3.0V option to Product Identification System (PIS) section.

Revision B (March 2005)

The following is the list of modifications:

1. Replaced 3x3 DFN package diagram.
2. Emphasized (bolded) a few specifications of **Section 1.0, Electrical Characteristics** in the DC Characteristics table.

Revision A (February 2005)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-XXX	X	X	XX	XXX
Device	Tape & Reel	Voltage Output	Tolerance	Temperature Range	Package	Qualification

Device:	MCP1726: 1A, Low Quiescent Current LDO Regulator
Tape & Reel Option:	T = Tape and Reel Blank = Tube
Standard Output Voltage*:	080 = 0.80V 120 = 1.20V 180 = 1.80V 250 = 2.50V 300 = 3.00V 330 = 3.30V 500 = 5.00V ADJ = Adjustable Voltage Version * Custom output voltages available upon request. Contact your local Microchip sales office for more information.
Tolerance:	2 = 2.0%
Temperature Range:	E = -40° to +125°C
Package*:	SN = Plastic Small Outline – Narrow, 3.90 mm Body, 8-Lead (SOIC) MF = Plastic Dual Flat, No Lead Package – 3x3x0.9 mm Body, 8-Lead (DFN) (Blank) = Standard Qualification VAO = AEC-Q100 Automotive Qualification *All packages are Lead Free

Examples:

a) MCP1726-0802E/MF: 0.80V, 1A LDO, 8LD DFN Package

b) MCP1726T-1202E/MF: Tape and Reel, 1.20V, 1A LDO, 8LD DFN Package

c) MCP1726-3002E/MF: 3.00V, 1A LDO, 8LD DFN Package

d) MCP1726T-3302E/MF: Tape and Reel, 3.30V, 1A LDO, 8LD DFN Package

e) MCP1726-1802E/SN: 1.80V, 1A LDO, 8LD SOIC Package

f) MCP1726T-2502E/SN: Tape and Reel, 2.50V, 1A LDO, 8LD SOIC Package

g) MCP1726-5002E/SN: 5.00V, 1A LDO, 8LD SOIC Package

h) MCP1726T-ADJE/SN: Tape and Reel, Adjustable, 1A LDO, 8LD SOIC Package

i) MCP1726-ADJE/MFVAO: Adjustable, 1A LDO, 8LD DFN Package, Automotive Qualified

j) MCP1726-1202E/SNVAO: 1.2V, 1A LDO, 8LD SOIC Package, Automotive Qualified

k) MCP1726-3302E/SNVAO: 3.3V, 1A LDO, 8LD SOIC Package, Automotive Qualified

l) MCP1726T-1202E/SNVAO: Tape and Reel, 1.2V, 1A LDO, 8LD SOIC Package, Automotive Qualified

m) MCP1726T-3302E/SNVAO: Tape and Reel, 3.3V, 1A LDO, 8LD SOIC Package, Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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