DN2450

N-Channel, Depletion-Mode, Vertical DMOS FET

Features

- High-input impedance
- Low-input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakages

Applications

- Normally-on switches
- Battery operated systems
- Voltage to current converters
- Constant current sources
- Current and voltage limiters

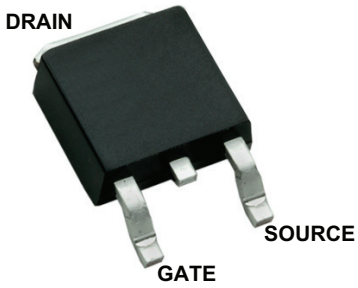
Description

This low threshold, depletion-mode, normally-on, transistor utilizes an advanced vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors, plus the high-input impedance and positive-temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

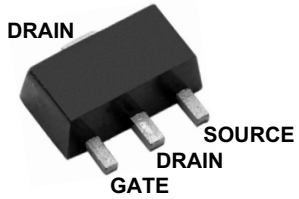
Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where a very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

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Package Type



TO-252 (D-PAK)



TO-243AA (SOT-89)

See Table 2-1 for pin information

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1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Drain-to-source voltage ..... BV_{DSX}
Drain-to-gate voltage ..... BV_{DGX}
Gate-to-source voltage ..... ±20V
Operating and storage temperature ..... -55°C to +150°C
Maximum junction temperature ..... 150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: DC AND AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC Parameters (**Note 1**, unless otherwise stated)						
BV_{DSX}	Drain-to-source breakdown voltage	500	–	–	V	V_{GS}= -5.0V, I_D= 100µA
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	–	-3.5	V	V_{DS}= 25V, I_D= 10µA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	–	–	-4.5	mV/°C	V_{DS}= 25V, I_D= 10µA (**Note 2**)
I_{GSS}	Gate body leakage	–	–	100	nA	V_{GS}= ±20V, V_{DS}= 0V
$I_{D(OFF)}$	Drain-to-source leakage current	–	–	1.0	µA	V_{DS}= BV_{DSX}, V_{GS}= -10V
		–	–	1.0	mA	V_{DS}= 0.8 BV_{DSX}, V_{GS}= -10V, T_A= 125°C (**Note 2**)
I_{DSS}	Saturated drain-to-source current	700	–	–	mA	V_{GS}= 0V, V_{DS}= 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	–	7.0	10	Ω	V_{GS}= 0V, I_D= 300mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	–	–	1.1	%/°C	V_{GS}= 0V, I_D= 300mA (**Note 2**)
AC Parameters (**Note 2**)						
G_{FS}	Forward transconductance	500	–	–	mmho	V_{DS}= 10V, I_D= 300mA
C_{ISS}	Input capacitance	–	150	200	pF	V_{GS}= -10V, V_{DS}= 25V, f = 1MHz
C_{OSS}	Common source output capacitance	–	40	55		
C_{RSS}	Reverse transfer capacitance	–	15	25		
$t_{d(ON)}$	Turn-on delay time	–	–	15	ns	V_{DD}= 25V, I_D= 300mA, R_{GEN}= 25Ω,
t_r	Rise time	–	–	20		
$t_{d(OFF)}$	Turn-off delay time	–	–	15		
t_f	Fall time	–	–	15		
Diode Parameters						
V_{SD}	Diode forward voltage drop	–	–	1.8	V	V_{GS}= -5.0V, I_{SD}= 300mA (**Note 1**)
t_{rr}	Reverse recovery time	–	800	–	ns	V_{GS}= -5.0V, I_{SD}= 300mA (**Note 2**)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

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TABLE 1-2: TYPICAL THERMAL RESISTANCE

Package	θ_{ja}
TO-252 (D-PAK)	81°C/W
TO-243AA (SOT-89)	133°C/W

TABLE 1-3: THERMAL CHARACTERISTICS

Package	I_D[1] continuous (mA)	I_D pulsed (mA)	Power Dissipation @T_A = 25°C (W)	I_{DR}[1] (mA)	I_{DRM} (mA)
TO-252 (D-PAK)	350	1000	2.5[2]	350	1000
TO-243AA (SOT-89)	230	900	1.6[2]	230	900

1. I_D continuous is limited by max rated T_j
2. Mounted on FR4 board, 25mm x 25mm x 1.57 mm

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION

Pin # TO-252	Pin # TO-243AA	Function
1	1	GATE
3	3	SOURCE
2,4	2,4	DRAIN

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3.0 APPLICATION INFORMATION

Figure shows the switching waveform and test circuit for DN2450.

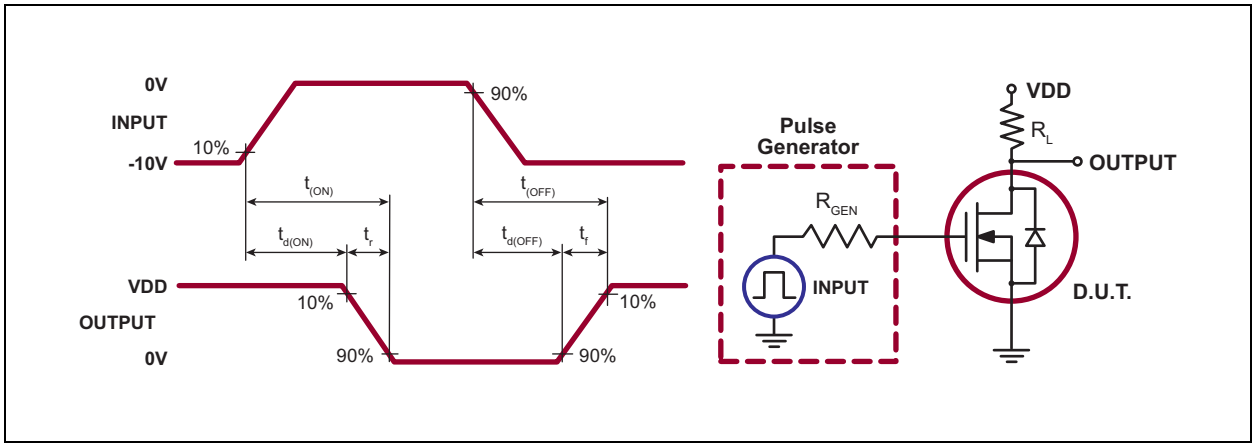


FIGURE 3-1: *Switching Waveforms and Test Circuit*

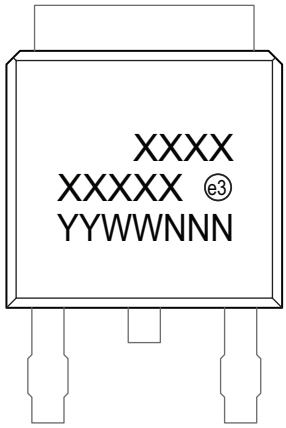
Product Summary

BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (Ω)	I_{DSS} (min) (mA)
500	10	700

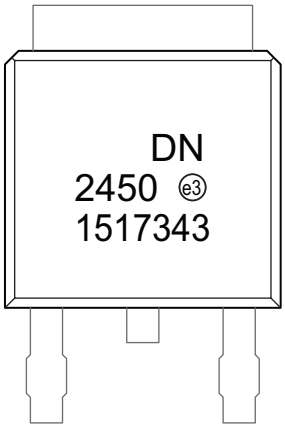
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

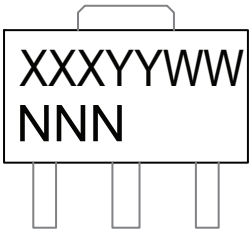
TO-252 (D-PAK)



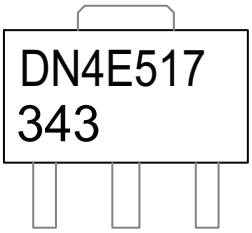
Example



3-lead TO-243AA *
(SOT-89)



Example

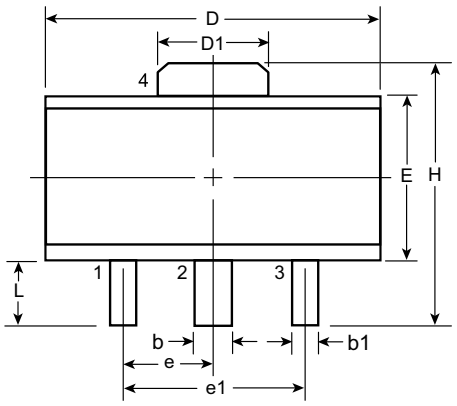


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

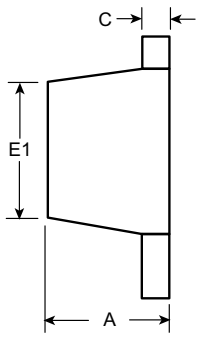
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



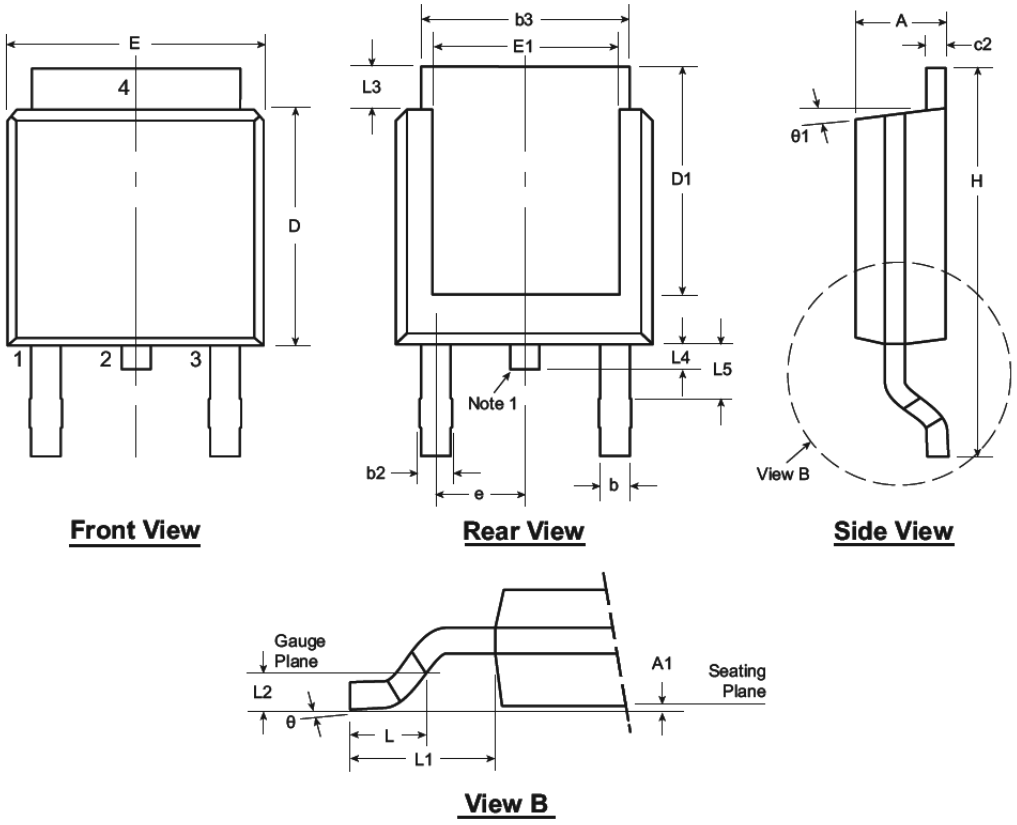
Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
Drawings not to scale.

3-Lead TO-252 (D-PAK) Package Outline (K4)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0°	0°
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (July 2015)

- Update file to new format

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	DN2450 =	N-Channel, Depletion-Mode, vertical DMOS FET
Package:	K4 =	TO-252 (D-PAK)
	N8 =	TO-243AA (SOT-89)
Environmental	G =	Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank) =	2000/Reel

Examples:

a) DN2450K4-G — TO-252 package, 2000/reel

b) DN2450N8-G — TO-243AA package, 2000/reel

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