MCP1810

Ultra-Low Quiescent Current LDO Regulator

Features

- Ultra-Low Quiescent Current: 20 nA (typical)
- Ultra-Low Shutdown Supply Current: 1 nA (typical)
- 150 mA Output Current Capability for $V_R \leq 3.5V$
- 100 mA Output Current Capability for $V_R > 3.5V$
- Input Operating Voltage Range: 2.5V to 5.5V
- Standard Output Voltages (V_R): 1.2V, 1.5V, 1.8V, 2.0V, 2.2V, 2.5V, 2.8V, 3.0V, 3.3V, 3.5V, 4.2V
- Low Dropout Voltage: 380 mV maximum at 150 mA
- Stable with 1.0 µF Ceramic Output Capacitor
- Overcurrent Protection
- Available in the following packages:
  - 2 x 2 mm No Lead VDFN
  - 3 Lead SOT-23 ($V_R < 4.0V$)
  - 5 Lead SOT-23 ($V_R < 4.0V$)

Applications

- Energy Harvesting
- Long-Life, Battery-Powered Applications
- Smart Cards
- Ultra-Low Consumption “Green” Products
- Portable Electronics

Description

The MCP1810 is a 150 mA (for $V_R \leq 3.5V$), 100 mA (for $V_R > 3.5V$) low dropout (LDO) linear regulator that provides high-current and low-output voltages, while maintaining an ultra-low 20 nA of quiescent current during device operation. In addition, the MCP1810 can be shut down for an even lower 1 nA (typical) supply current draw.

The MCP1810 comes in 11 standard fixed output-voltage versions: 1.2V, 1.5V, 1.8V, 2.0V, 2.2V, 2.5V, 2.8V, 3.0V, 3.3V, 3.5V and 4.2V.

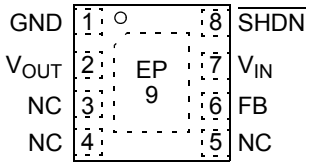
The 150 mA output current capability, combined with the low output-voltage capability, make the MCP1810 a good choice for new ultra-long-life LDO applications that have high-current demands, but require ultra-low power consumption during sleep states.

The MCP1810 is stable with ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 µF (2.2 µF recommended) of output capacitance is needed to stabilize the LDO.

The MCP1810 ultra-low quiescent and shutdown current allows it to be paired with other ultra-low current draw devices, such as Microchip’s nanoWatt eXtreme Low Power (XLP) technology devices, for a complete ultra-low-power solution.

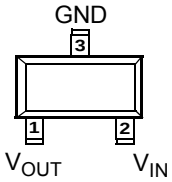
Package Types

MCP1810
2x2 VDFN*

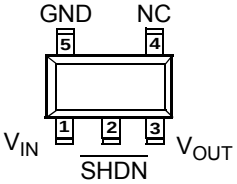


* Includes Exposed Thermal Pad (EP); see Table 3-1.

3 Lead-SOT23



5 Lead-SOT23



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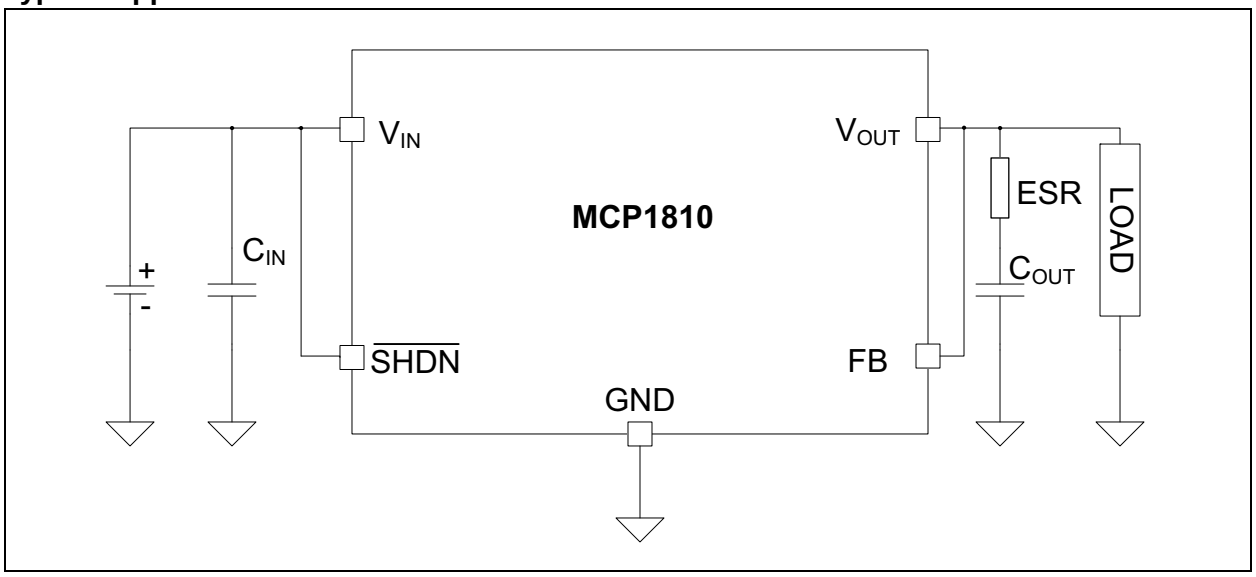
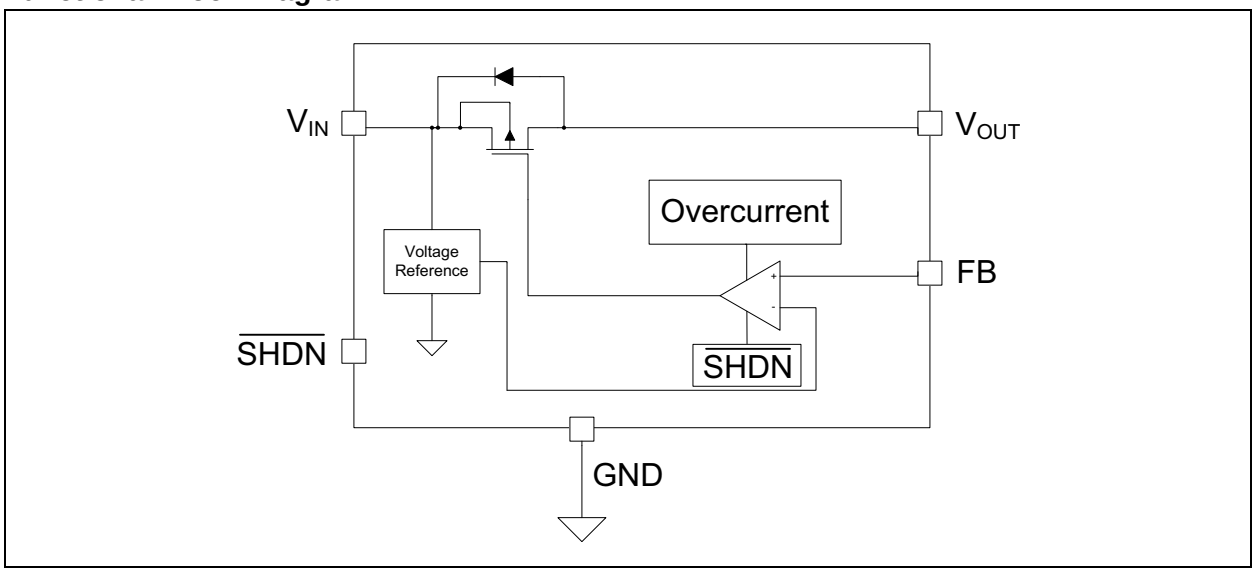
Typical Application



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input voltage, V_{IN} ..... +6.0V
Maximum Voltage on any pin - ..... (GND - 0.3V) to +6.0V
Output Short-Circuit Duration ..... Unlimited
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature, T_J ..... +150°C
Operating Junction Temperature, T_J ..... –40°C to +85°C
ESD protection on all pins (HBM) ..... ≥ 4 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 800$ mV **(Note 1)**, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 2.2$ µF ceramic (X7R), $T_A = +25°C$. **Boldface** type applies for junction temperatures T_J of –40°C to +85°C **(Note 2)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**5.5**	V	
		2.5	—	**5.5**	V	$V_R \le 1.8V$, $I_{OUT} < 50$ mA
Output Voltage Range	V_{OUT}	**1.2**	—	**4.2**	V	
Input Quiescent Current	I_Q	—	20	**50**	nA	$V_{IN} = V_R + 800$ mV or 2.7V (whichever is greater) $I_{OUT} = 0$
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	1	—	nA	$\overline{SHDN}$ = GND
Ground Current	I_{GND}	—	200	**290**	µA	$V_{IN} = V_R + 800$ mV or 2.7V (whichever is greater) $I_{OUT} = 150$ mA, $V_R \le 3.5V$ $I_{OUT} = 100$ mA, $V_R > 3.5V$
Maximum Continuous Output Current	I_{OUT}	—	—	**150**	mA	$V_R \le 3.5V$
		—	—	**100**	mA	$V_R > 3.5V$
Current Limit	I_{OUT}	—	350	—	mA	$V_{OUT} = 0.9 \times V_R$ $V_R \le 3.5V$
		—	250	—	mA	$V_{OUT} = 0.9 \times V_R$ $V_R > 3.5V$
Output Voltage Regulation	V_{OUT}	**V_R - 4%**	—	**V_R + 4%**	V	$V_R < 1.8V$ **(Note 3)**
		V_R - 2%	—	**V_R + 2%**	V	$V_R \ge 1.8V$ **(Note 3)**
Line Regulation	$\Delta V_{OUT} / (V_{OUT} \times \Delta V_{IN})$	**–4**	—	**+4**	%/V	$V_{IN} = V_{IN(min.)}$ to 5.5V $I_{OUT} = 50$ mA **(Note 1)**

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge V_{IN(MIN)}$ and $V_{IN} \ge V_R + V_{DROPOUT(MAX)}$.

2: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is short enough such that the rise in junction temperature over the ambient temperature is not significant.

3: V_R is the nominal regulator output voltage. V_R = 1.2V, 1.5V, 1.8V, 2.0V, 2.2V, 2.5V, 2.8V, 3.0V, 3.3V, 3.5V or 4.2V.

4: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 800$ mV **(Note 1)**, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 2.2$ µF ceramic (X7R), $T_A = +25°C$. **Boldface** type applies for junction temperatures T_J of –40°C to +85°C **(Note 2)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**–3**	1	**+3**	%	$V_{IN} = (V_{IN(MIN)} + V_{IN(MAX)})/2$ I_{OUT} = 0.02 mA to 150 mA **(Note 1)**
Dropout Voltage	$V_{DROPOUT}$	—	—	**380**	mV	I_{OUT} = 150 mA $V_R \leq 3.5V$ **(Note 4)**
		—	—	**280**	mV	I_{OUT} = 100 mA $V_R > 3.5V$ **(Note 4)**
Shutdown Input						
Logic High Input	$V_{SHDN-HIGH}$	**70**	—	—	$\%V_{IN}$	$V_{IN} = V_R + 800$ mV or 2.7V (whichever is greater) I_{OUT} = 1 mA **(Note 3)**
Logic Low Input	$V_{SHDN-LOW}$	—	—	**30**	$\%V_{IN}$	$V_{IN} = V_R + 800$ mV or 2.7V (whichever is greater) I_{OUT} = 1 mA **(Note 3)**
AC Performance						
Output Delay from $\overline{SHDN}$	T_{OR}	—	20	—	ms	$\overline{SHDN}$ = GND to V_{IN} V_{OUT} = GND to 95% V_R
Output Noise	e_N	—	0.48	—	µV/√Hz	V_{IN} = 3.3V $C_{IN} = C_{OUT}$ = 2.2 µF ceramic (X7R) V_R = 2.5V, I_{OUT} = 50 mA f = 1 kHz
		—	48	—	µVrms	V_{IN} = 3.3V $C_{IN} = C_{OUT}$ = 2.2 µF ceramic (X7R) V_R = 2.5V, I_{OUT} = 50 mA f = 100 Hz to 1 MHz
Power Supply Ripple Rejection Ratio	PSRR	—	40	—	dB	f = 100 Hz, I_{OUT} = 10 mA V_{INAC} = 200 mV pk-pk C_{IN} = 0 µF

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq V_{IN(MIN)}$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is short enough such that the rise in junction temperature over the ambient temperature is not significant.

3: V_R is the nominal regulator output voltage. V_R = 1.2V, 1.5V, 1.8V, 2.0V, 2.2V, 2.5V, 2.8V, 3.0V, 3.3V, 3.5V or 4.2V.

4: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+85	°C	Steady State
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 2 x 2 mm VDFN-8LD	θ_{JA}	—	73.1	—	°C/W	JEDEC® standard FR4 board with 1 oz. copper and thermal vias
	θ_{JC}	—	10.7	—	°C/W	
Thermal Resistance, SOT23-3LD	θ_{JA}	—	256	—	°C/W	
	θ_{JC}	—	81	—	°C/W	
Thermal Resistance, SOT23-5LD	θ_{JA}	—	256	—	°C/W	
	θ_{JC}	—	81	—	°C/W	

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, $V_{IN} = V_R + 0.8V$, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

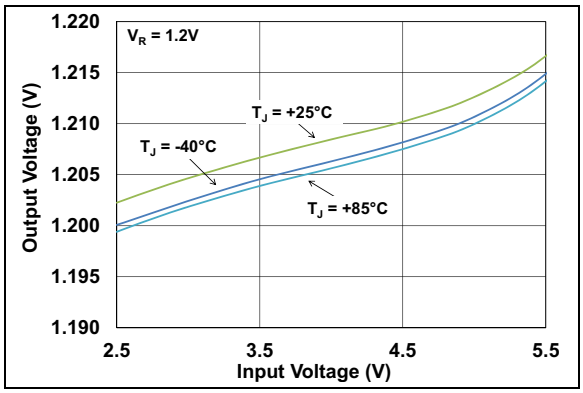

FIGURE 2-1: *Output Voltage vs. Input Voltage (V_R = 1.2V).*

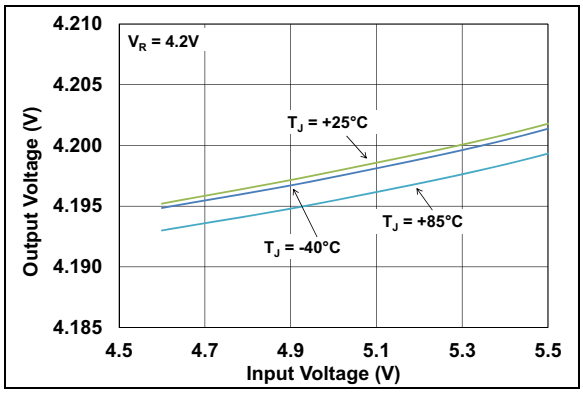

FIGURE 2-4: *Output Voltage vs. Input Voltage (V_R = 4.2V).*

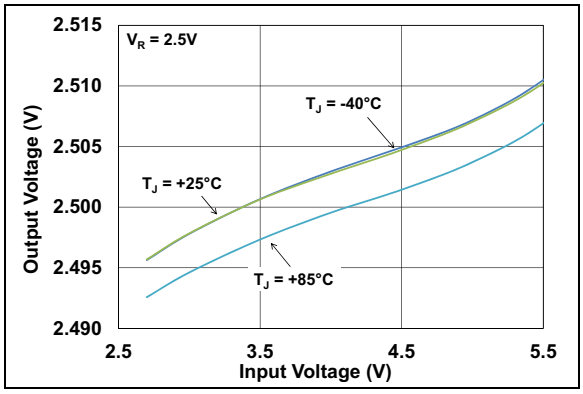

FIGURE 2-2: *Output Voltage vs. Input Voltage (V_R = 2.5V).*

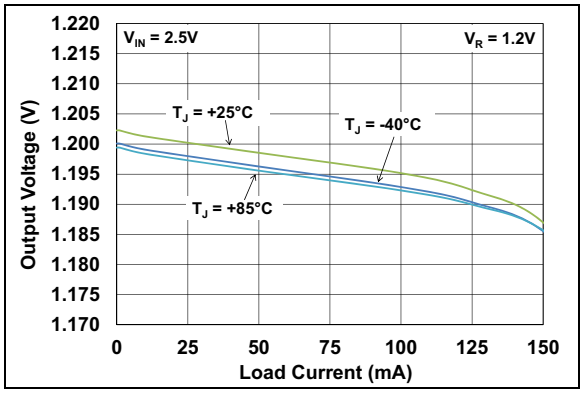

FIGURE 2-5: *Output Voltage vs. Load Current (V_R = 1.2V).*

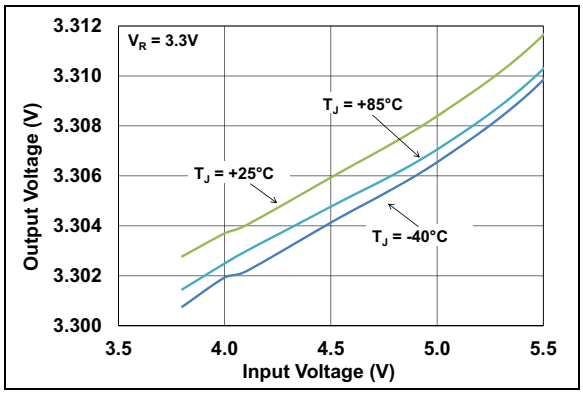

FIGURE 2-3: *Output Voltage vs. Input Voltage (V_R = 3.3V).*

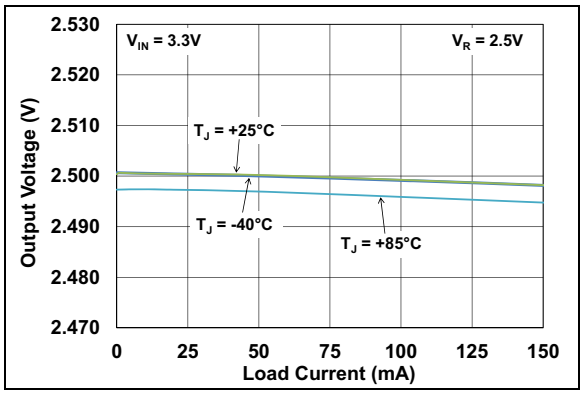

FIGURE 2-6: *Output Voltage vs. Load Current (V_R = 2.5V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

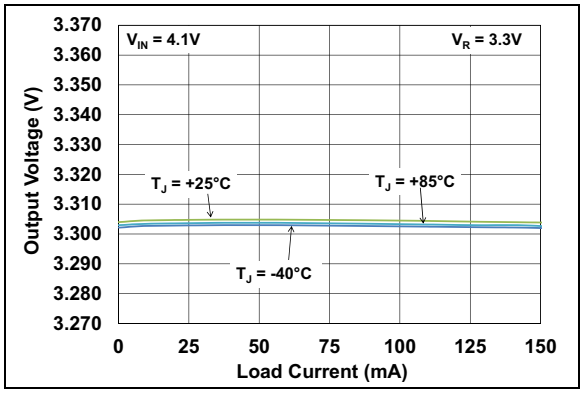

FIGURE 2-7: *Output Voltage vs. Load Current (V_R = 3.3V).*

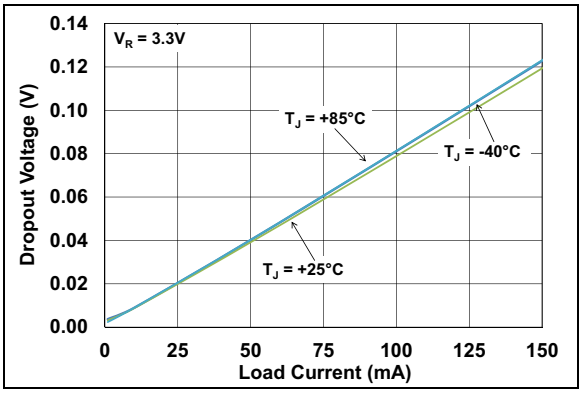

FIGURE 2-10: *Dropout Voltage vs. Load Current (V_R = 3.3V).*

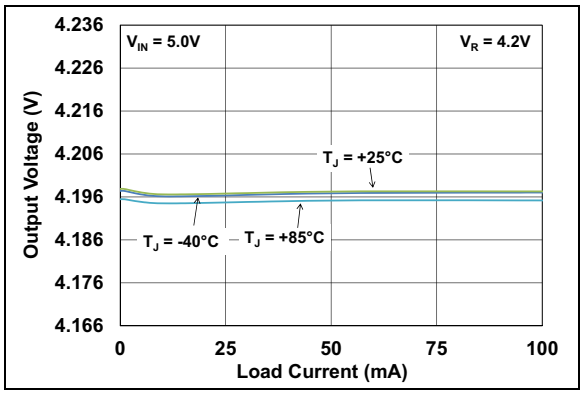

FIGURE 2-8: *Output Voltage vs. Load Current (V_R = 4.2V).*

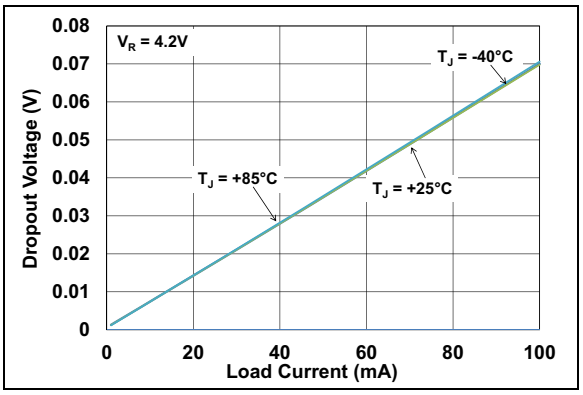

FIGURE 2-11: *Dropout Voltage vs. Load Current (V_R = 4.2V).*

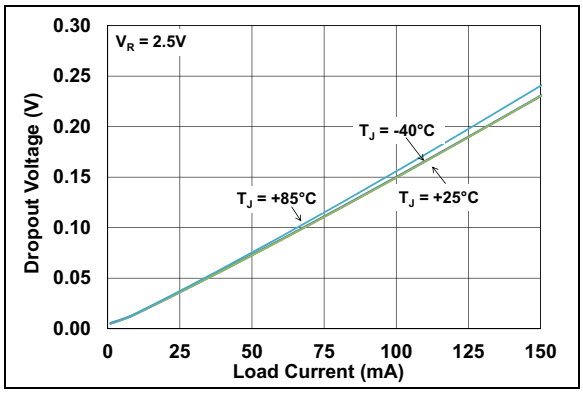

FIGURE 2-9: *Dropout Voltage vs. Load Current (V_R = 2.5V)*

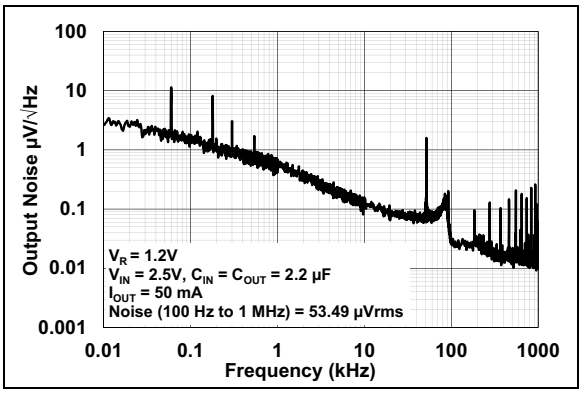

FIGURE 2-12: *Noise vs. Frequency (V_R = 1.2V).*

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Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, $V_{IN} = V_R + 0.8V$, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

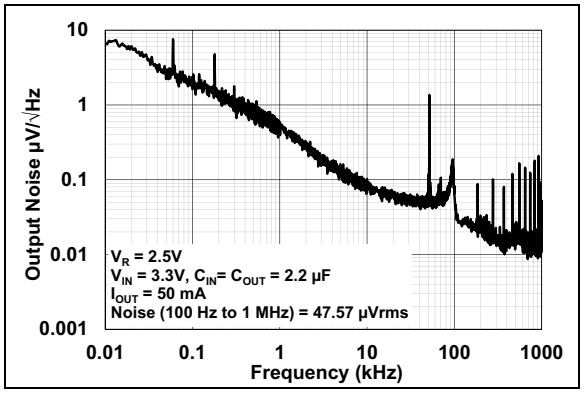

FIGURE 2-13: *Noise vs. Frequency (V_R = 2.5V).*

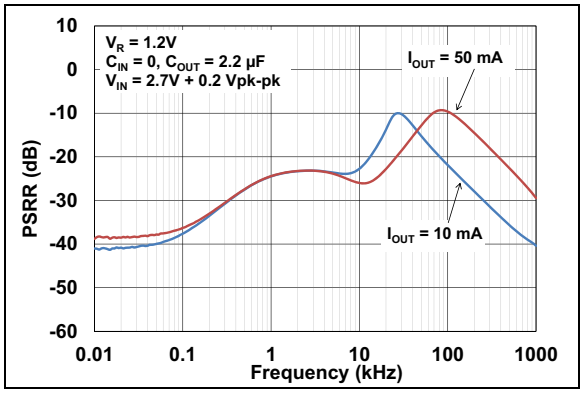

FIGURE 2-16: *Power Supply Ripple Rejection vs. Frequency (V_R = 1.2V).*

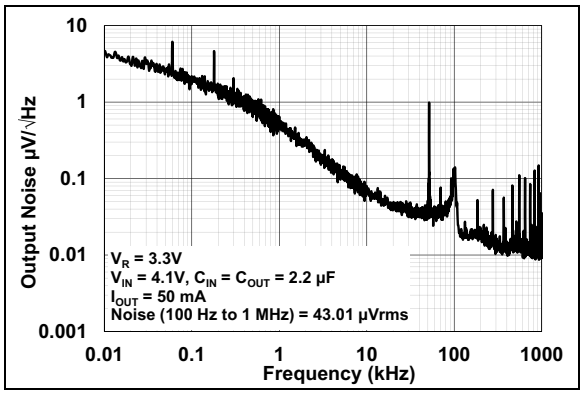

FIGURE 2-14: *Noise vs. Frequency (V_R = 3.3V).*

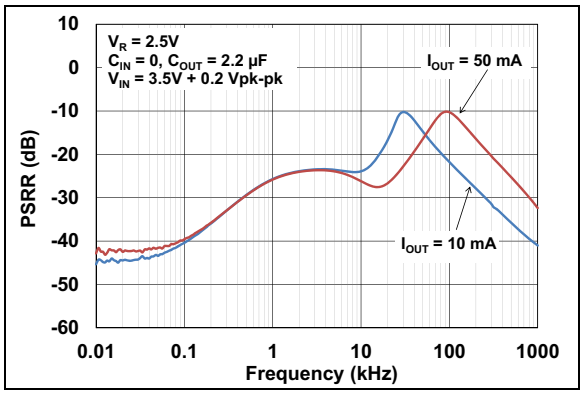

FIGURE 2-17: *Power Supply Ripple Rejection vs. Frequency (V_R = 2.5V).*

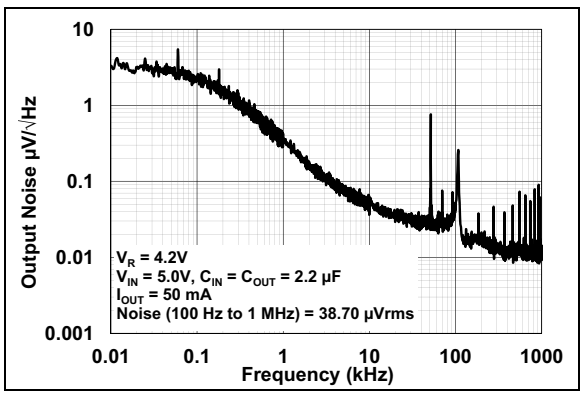

FIGURE 2-15: *Noise vs. Frequency (V_R = 4.2V).*

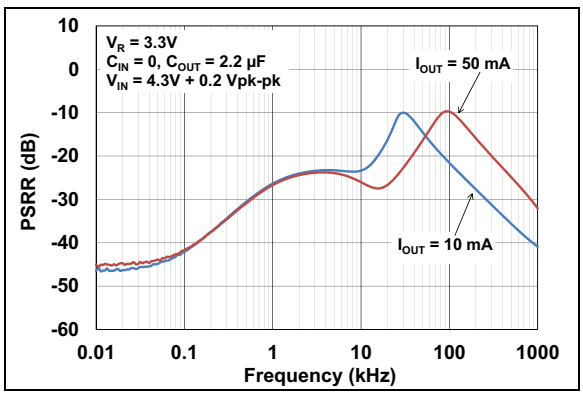

FIGURE 2-18: *Power Supply Ripple Rejection vs. Frequency (V_R = 3.3V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

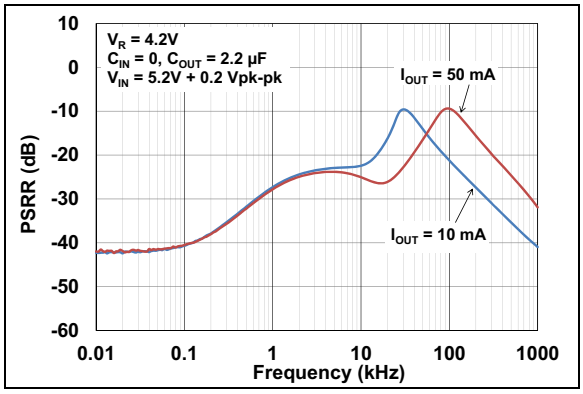

FIGURE 2-19: *Power Supply Ripple Rejection vs. Frequency (V_R = 4.2V).*

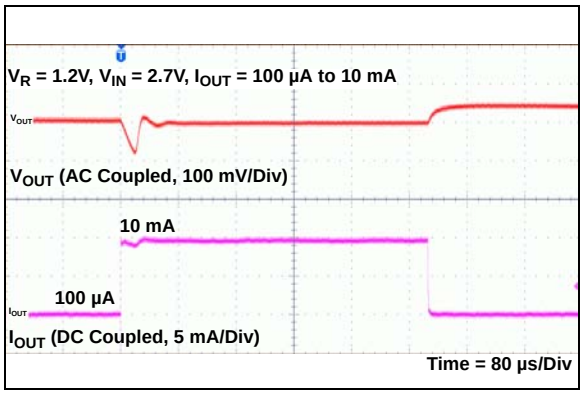

FIGURE 2-20: *Dynamic Load Step (V_R = 1.2V).*

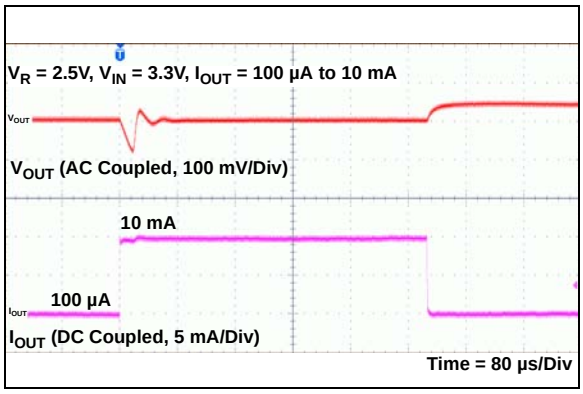

FIGURE 2-21: *Dynamic Load Step (V_R = 2.5V).*

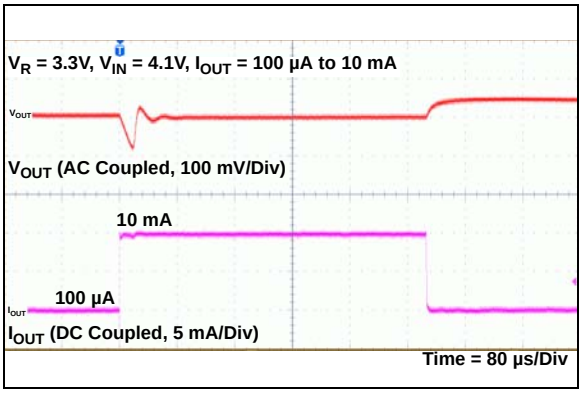

FIGURE 2-22: *Dynamic Load Step (V_R = 3.3V).*

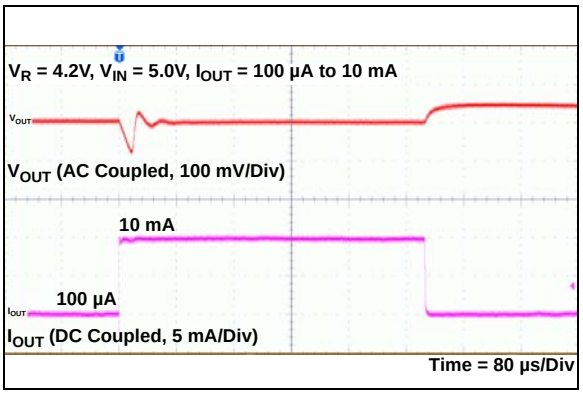

FIGURE 2-23: *Dynamic Load Step (V_R = 4.2V).*

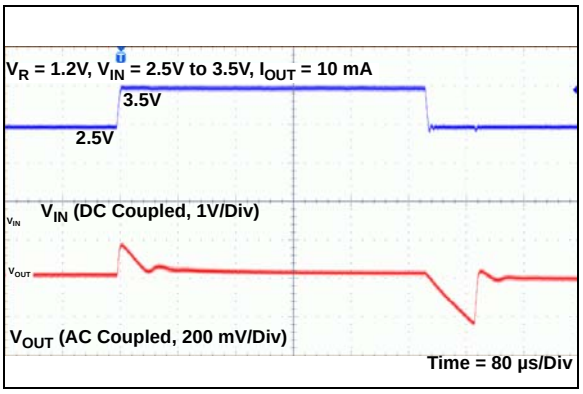

FIGURE 2-24: *Dynamic Line Step (V_R = 1.2V).*

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Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, $V_{IN} = V_R + 0.8V$, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

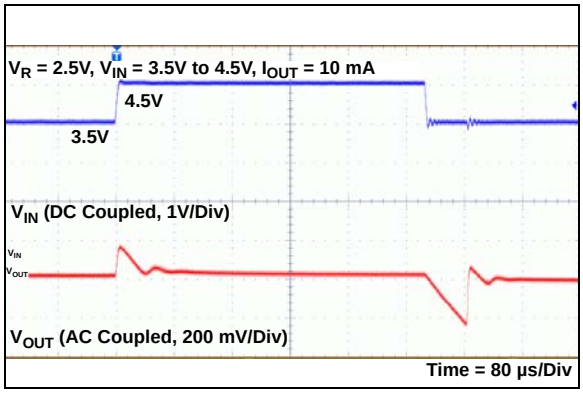

FIGURE 2-25: *Dynamic Line Step (V_R = 2.5V).*

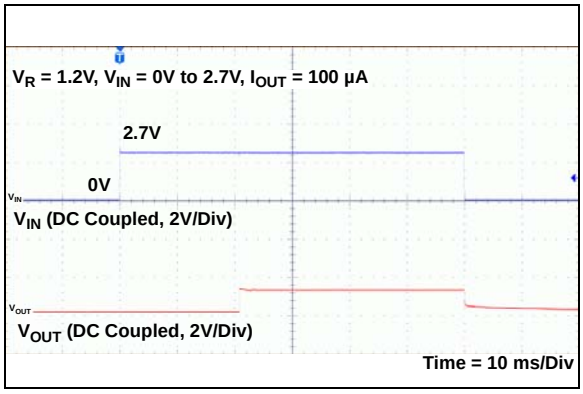

FIGURE 2-28: *Start-up from V_{IN} (V_R = 1.2V).*

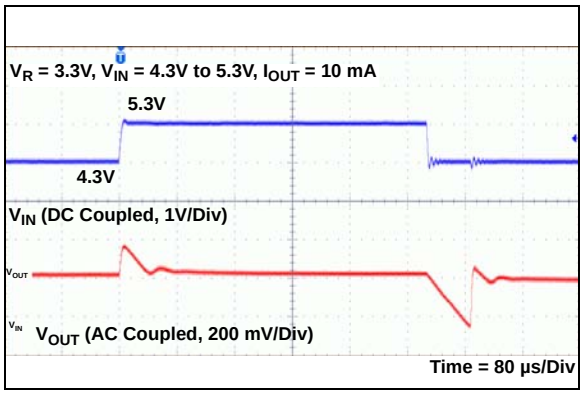

FIGURE 2-26: *Dynamic Line Step (V_R = 3.3V).*

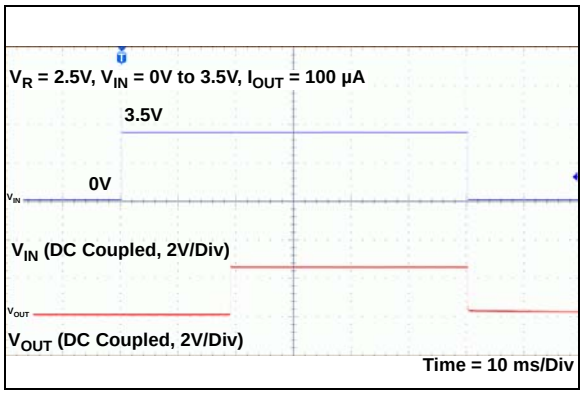

FIGURE 2-29: *Start-up from V_{IN} (V_R = 2.5V).*

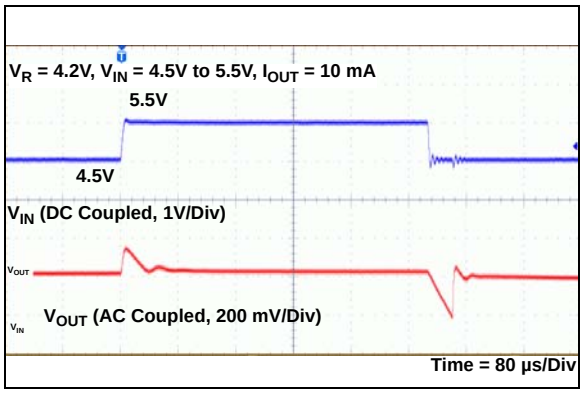

FIGURE 2-27: *Dynamic Line Step (V_R = 4.2V).*

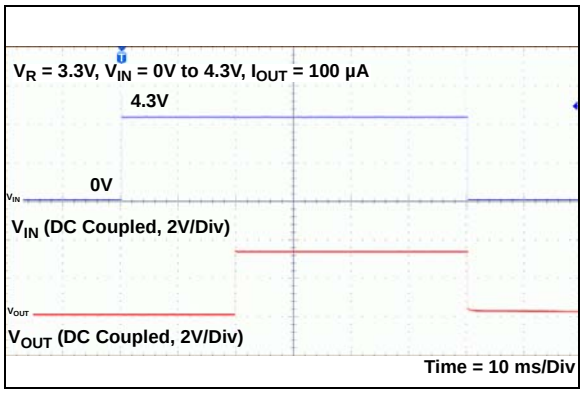

FIGURE 2-30: *Start-up from V_{IN} (V_R = 3.3V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

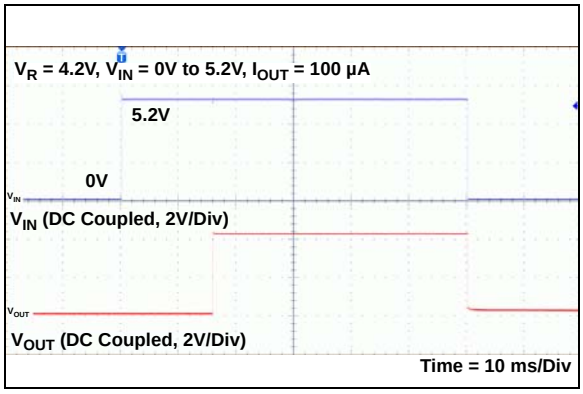

FIGURE 2-31: *Start-up from V_{IN} (V_R = 4.2V).*

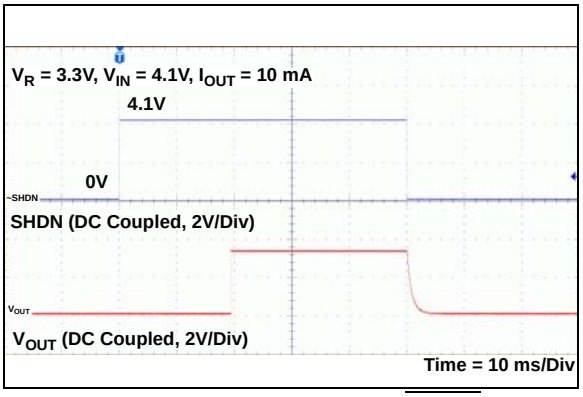

FIGURE 2-34: *Start-up from $\overline{SHDN}$ (V_R = 3.3V).*

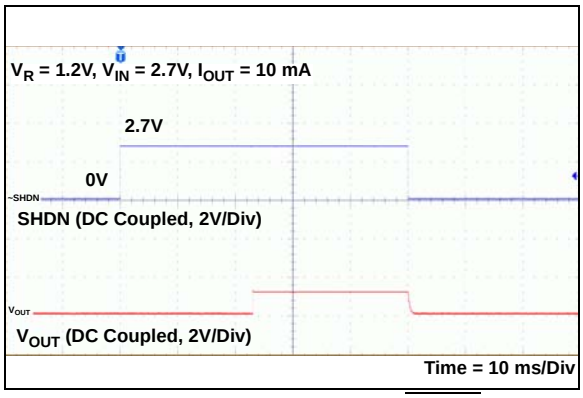

FIGURE 2-32: *Start-up from $\overline{SHDN}$ (V_R = 1.2V).*

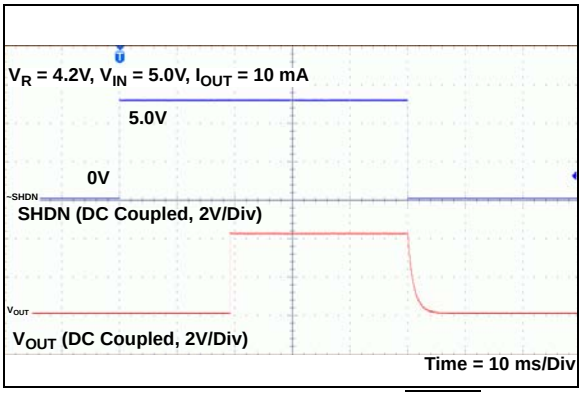

FIGURE 2-35: *Start-up from $\overline{SHDN}$ (V_R = 4.2V).*

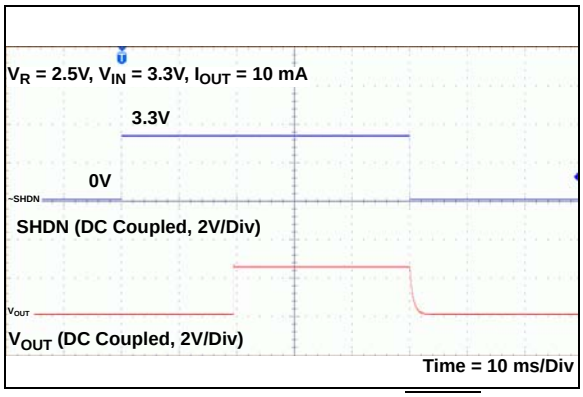

FIGURE 2-33: *Start-up from $\overline{SHDN}$ (V_R = 2.5V).*

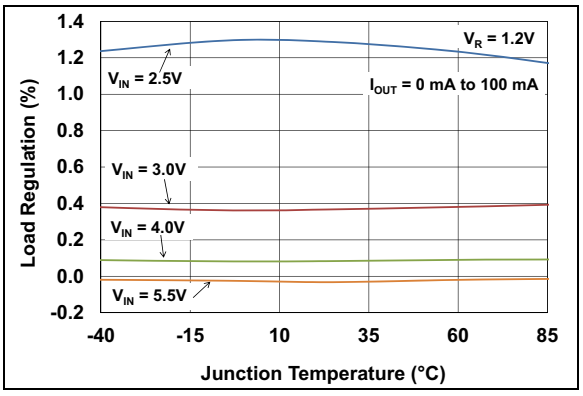

FIGURE 2-36: *Load Regulation vs. Junction Temperature (V_R = 1.2V).*

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Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

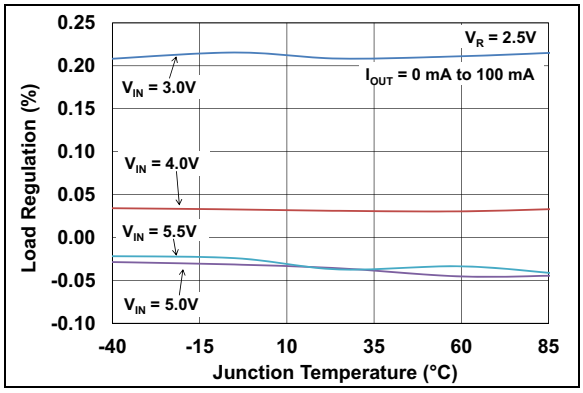

FIGURE 2-37: *Load Regulation vs. Junction Temperature (V_R = 2.5V).*

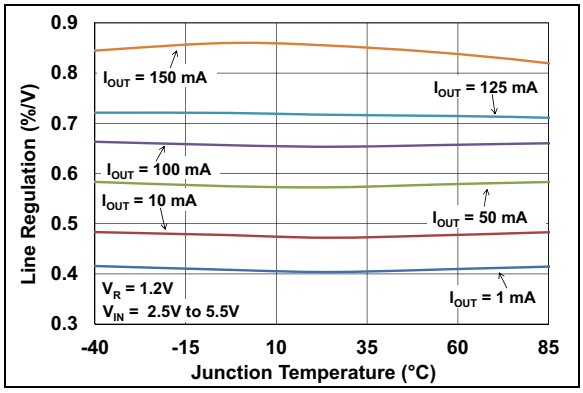

FIGURE 2-40: *Line Regulation vs. Junction Temperature (V_R = 1.2V).*

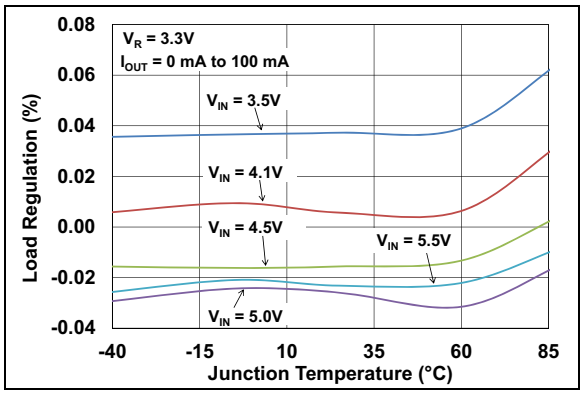

FIGURE 2-38: *Load Regulation vs. Junction Temperature (V_R = 3.3V).*

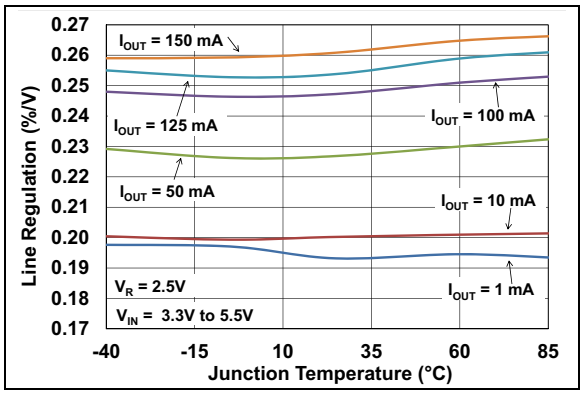

FIGURE 2-41: *Line Regulation vs. Junction Temperature (V_R = 2.5V).*

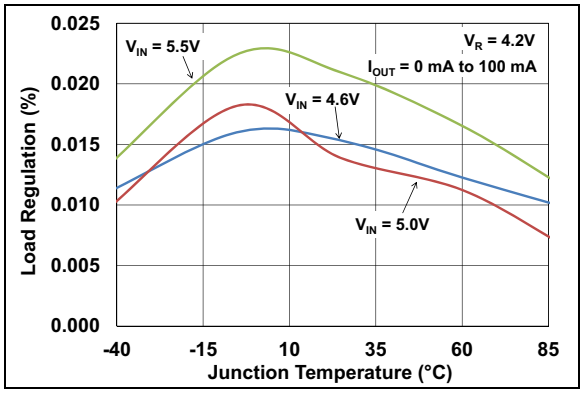

FIGURE 2-39: *Load Regulation vs. Junction Temperature (V_R = 4.2V).*

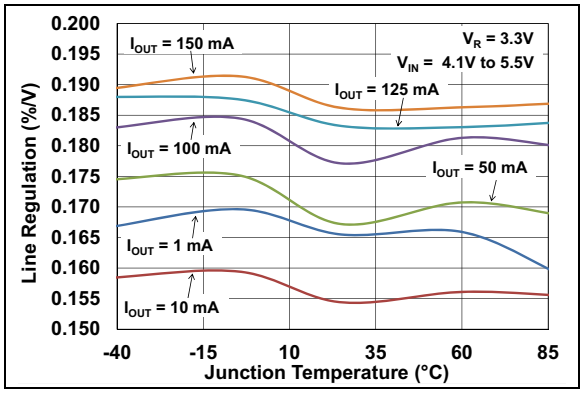

FIGURE 2-42: *Line Regulation vs. Junction Temperature (V_R = 3.3V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

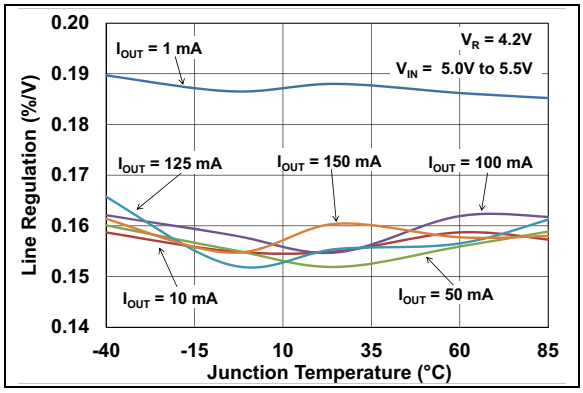

FIGURE 2-43: *Line Regulation vs. Junction Temperature (V_R = 4.2V).*

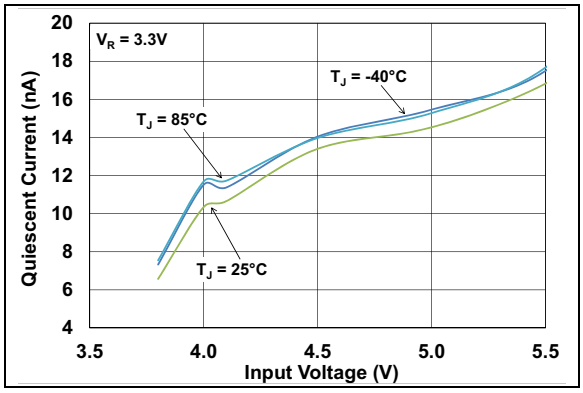

FIGURE 2-46: *Quiescent Current vs. Input Voltage (V_R = 3.3V).*

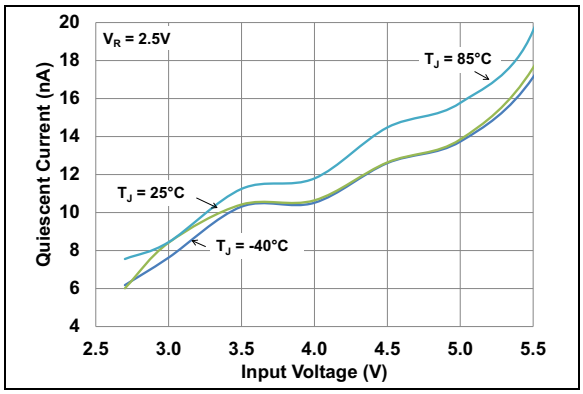

FIGURE 2-44: *Quiescent Current vs. Input Voltage (V_R = 1.2V).*

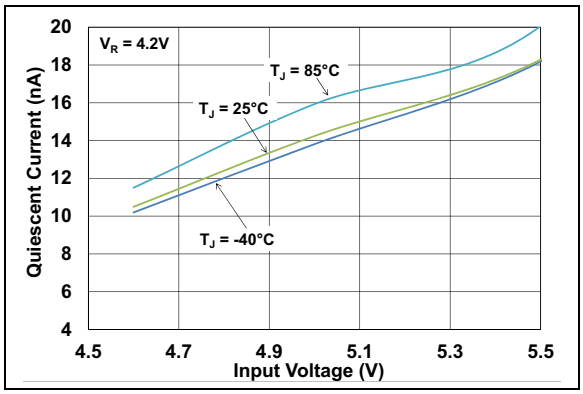

FIGURE 2-47: *Quiescent Current vs. Input Voltage (V_R = 4.2V).*

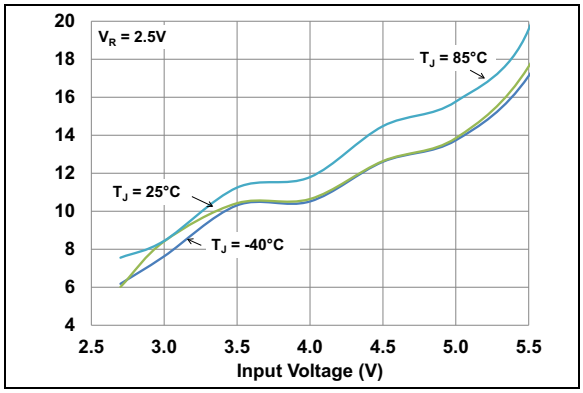

FIGURE 2-45: *Quiescent Current vs. Input Voltage (V_R = 2.5V).*

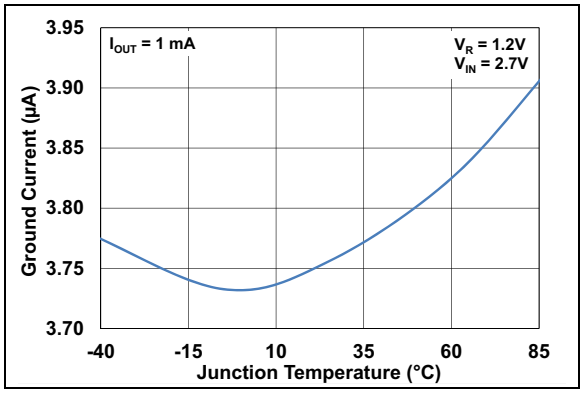

FIGURE 2-48: *Ground Current vs. Junction Temperature (V_R = 1.2V).*

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Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

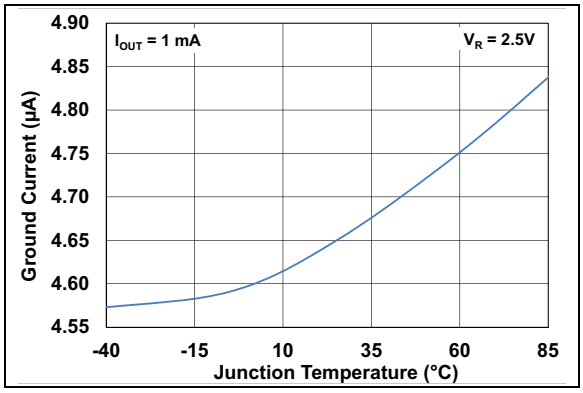

FIGURE 2-49: *Ground Current vs. Junction Temperature (V_R = 2.5V).*

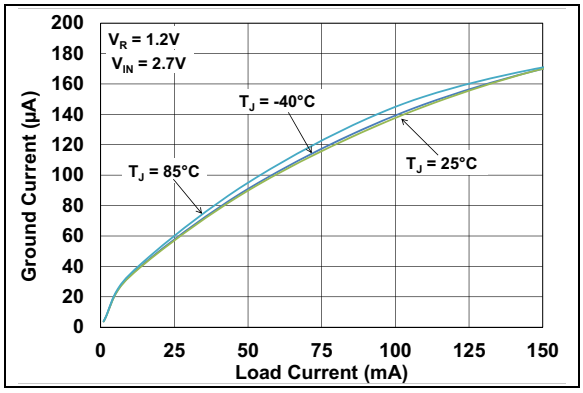

FIGURE 2-52: *Ground Current vs. Load Current (V_R = 1.2V).*

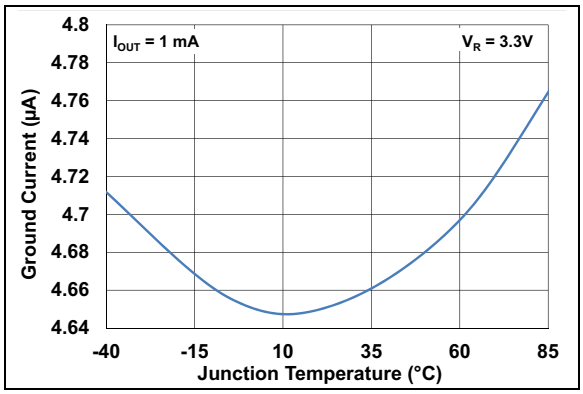

FIGURE 2-50: *Ground Current vs. Junction Temperature (V_R = 3.3V).*

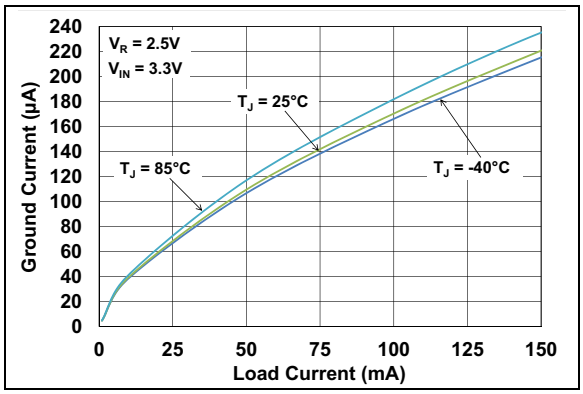

FIGURE 2-53: *Ground Current vs. Load Current (V_R = 2.5V).*

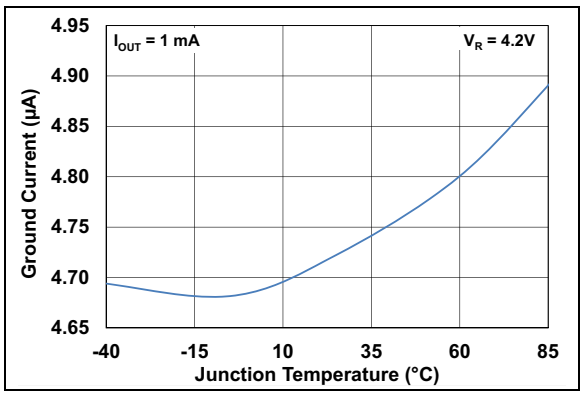

FIGURE 2-51: *Ground Current vs. Junction Temperature (V_R = 4.2V).*

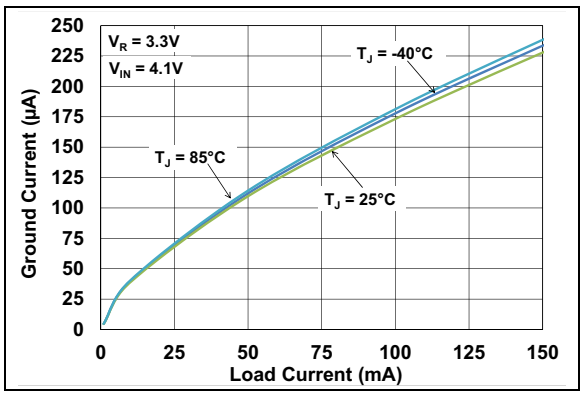

FIGURE 2-54: *Ground Current vs. Load Current (V_R = 3.3V).*

Note: Unless otherwise indicated, C_{OUT} = 2.2 µF ceramic (X7R), C_{IN} = 2.2 µF ceramic (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 0.8V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

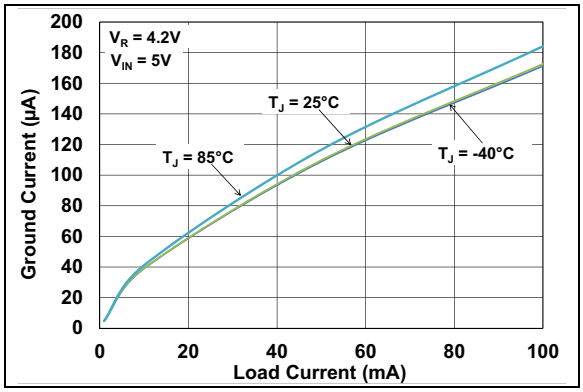

FIGURE 2-55: *Ground Current vs. Load Current (V_R = 4.2V).*

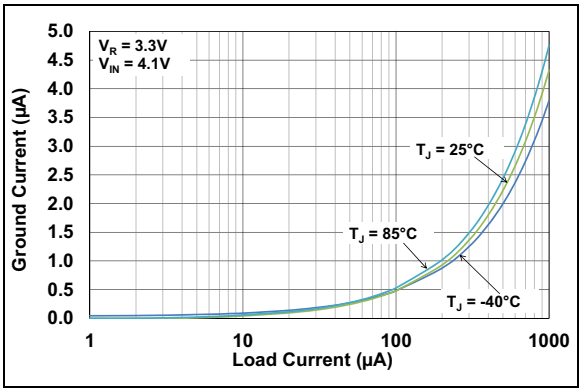

FIGURE 2-58: *Ground Current vs. Very Low Load Current (V_R = 3.3V).*

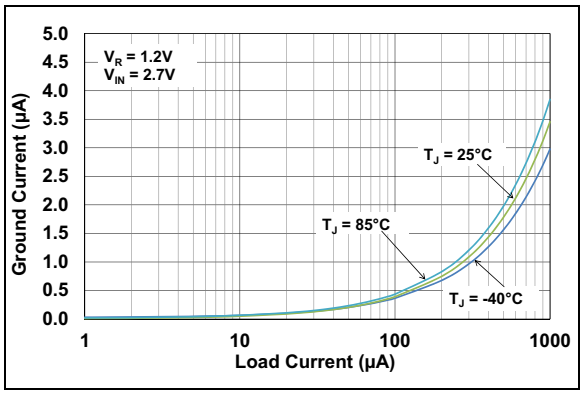

FIGURE 2-56: *Ground Current vs. Very Low Load Current (V_R = 1.2V).*

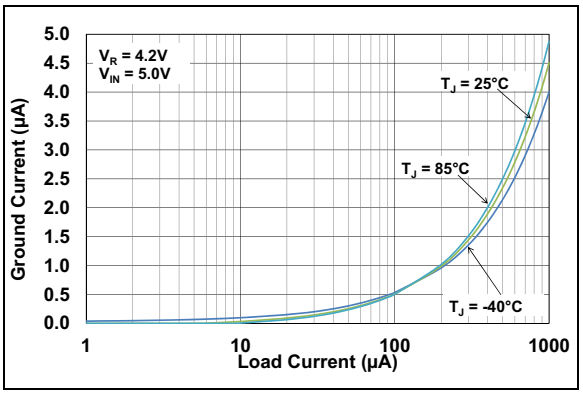

FIGURE 2-59: *Ground Current vs. Very Low Load Current (V_R = 4.2V).*

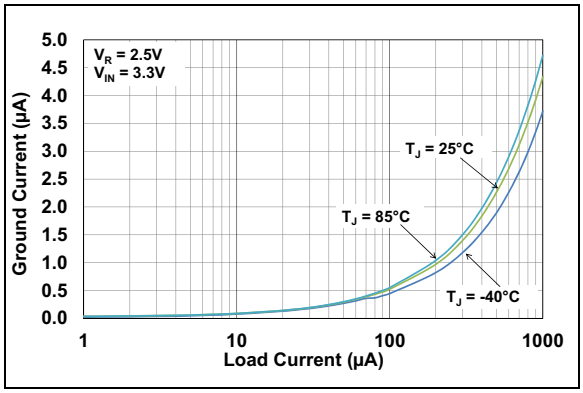

FIGURE 2-57: *Ground Current vs. Very Low Load Current (V_R = 2.5V).*

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3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1810 2 x 2 VDFN	MCP1810 3Ld-SOT23	MCP1810 5Ld-SOT23	Symbol	Description
1	3	5	GND	Ground
2	1	3	V_{OUT}	Regulated Output Voltage
3, 4, 5	–	4	NC	Not connected pins (should either be left floated or connected to ground)
6	–	–	FB	Output Voltage Feedback Input
7	2	1	V_{IN}	Input Voltage Supply
8	–	2	$\overline{SHDN}$	Shutdown Control Input (active-low)
9	–	–	EP	Exposed Thermal Pad, connected to GND

3.1 Ground Pin (GND)

For optimal noise and power supply rejection ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically quiet circuit ground. This will help the LDO power supply rejection ratio and noise performance. The GND pin of the LDO conducts only ground current, so a heavy trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and voltage spikes caused by fast transient load currents.

3.2 Regulated Output Voltage Pin (V_{OUT})

The V_{OUT} pin is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 µF is required for LDO stability. The MCP1810 is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See **Section 4.2 "Output Capacitor"** for output capacitor selection guidance.

3.3 Feedback Pin (FB)

The output voltage is connected to the FB input. This sets the output voltage regulation value.

3.4 Input Voltage Supply Pin (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications (2.2 µF, typical). The type of capacitor used can be ceramic, tantalum, or aluminum-electrolytic. However, the low ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

3.5 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the LDO enters a low-quiescent current shutdown state, where the typical quiescent current is 1 nA.

3.6 Exposed Thermal Pad (EP)

The 2 x 2 VDFN 8-Lead package has an exposed thermal pad on the bottom of the package. The exposed thermal pad gives the device better thermal characteristics by providing a good thermal path to either the printed circuit board (PCB) or heat sink, to remove heat from the device. The exposed pad of the package is at ground potential.

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NOTES:

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4.0 DEVICE OVERVIEW

The MCP1810 is a 150 mA/100 mA output current, low dropout (LDO) voltage regulator. The low dropout voltage of 380 mV maximum at 150 mA of current makes it ideal for battery-powered applications. The input voltage ranges from 2.5V to 5.5V. The MCP1810 adds a shutdown-control input pin and is available in eleven standard fixed-output voltage options: 1.2V, 1.5V, 1.8V, 2.0V, 2.2V, 2.5V, 2.8V, 3.0V, 3.3V, 3.5V and 4.2V. It uses a proprietary voltage reference and sensing scheme to maintain the ultra-low 20 nA quiescent current.

4.1 Output Current and Current Limiting

The MCP1810 LDO is tested and ensured to supply a minimum of 150 mA of output current for the 1.2V-to-3.5V output range, and 100 mA of output current for the 3.5V-to-4.2V output range. The device has no minimum output load, so the output load current can go to 0 mA and the LDO will continue regulating the output voltage within the specified tolerance.

The MCP1810 also incorporates an output current limit. The current limit is set to 350 mA typical for the $1.2V \leq V_R \leq 3.5V$ range, and to 250 mA typical for the $3.5V < V_R \leq 5.5V$ range.

4.2 Output Capacitor

The MCP1810 requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and robust environmental qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 mΩ.

For extreme output currents — below 100 µA or close to 150 mA/100 mA — an output capacitor with higher ESR (tantalum, aluminum-electrolytic) is recommended. Ceramic output capacitor may be used if a 0.5Ω to 1Ω resistor is placed in series with the capacitor.

4.3 Input Capacitor

Low input-source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF of capacitance is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides a low-impedance source of current for the LDO to use for dynamic load changes. This allows the LDO to respond quickly to the output load step. For good step-response performance, the input capacitor should be equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO, as well as the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.4 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The maximum input-low logic level is 30% of V_{IN} and the minimum high logic level is 70% of V_{IN}.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 20 ms (typical) delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signal or noise on the $\overline{SHDN}$ input signal. After the 20 ms delay, the LDO output enters its current-limited soft-start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 20 ms delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the LDO output being in regulation is typically 20 ms. Figure 4-1 shows a timing diagram of the $\overline{SHDN}$ input.

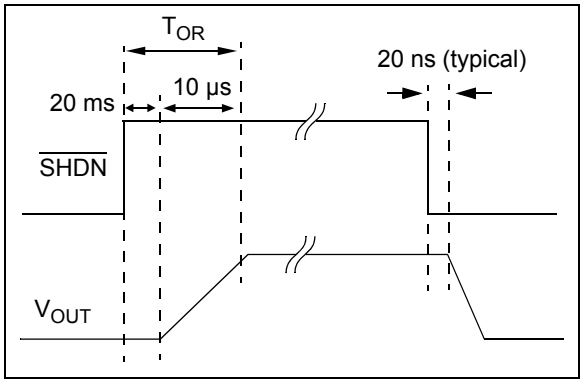

FIGURE 4-1: *Shutdown Input Timing Diagram.*

4.5 Dropout Voltage

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 3% below the nominal value that was measured with a V_R + 0.8V differential applied. The MCP1810 LDO has a low-dropout voltage specification of 230 mV (typical) for V_R = 2.5V, 120 mV for V_R = 3.3V at 150 mA out, and 70 mV (typical) for V_R = 4.2V at 100 mA out. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

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5.0 APPLICATION CIRCUITS AND ISSUES

5.1 Typical Application

The MCP1810 is used for applications that require ultra-low quiescent current draw.

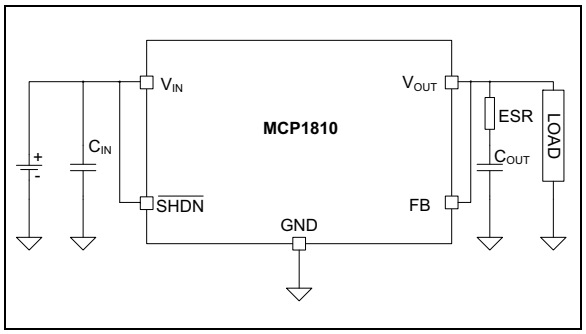

FIGURE 5-1: *Typical Application Circuit.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1810 is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO pass device
$V_{IN(MAX)}$ = Maximum input voltage
$V_{OUT(MIN)}$ = LDO minimum output voltage
$I_{OUT(MAX)}$ = Maximum output current

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1810 as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated by applying Equation 5-2:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{I(GND)}$ = Power dissipation due to the quiescent current of the LDO
$V_{IN(MAX)}$ = Maximum input voltage
I_{GND} = Current flowing into the GND pin

The total power dissipated within the MCP1810 is the sum of the power dissipated in the LDO pass device and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the MCP1810 is maximum 290 µA at full load. Operating at a maximum V_{IN} of 5.5V results in a power dissipation of 1.6 mW. For most applications, this is small compared to the LDO pass device power dissipation, and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1810 is +85°C. To estimate the internal junction temperature of the MCP1810, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction to ambient for the 2x2 VDFN 8-Lead package is estimated at 73.1°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature
P_{TOTAL} = Total power dissipation of the device
$R\theta_{JA}$ = Thermal resistance from junction to ambient
$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

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EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

$P_{D(MAX)}$ = Maximum power dissipation of the device

$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

T_A = Ambient temperature

5.3 Typical Application Examples

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

EXAMPLE 5-1:

Package

Package Type = 2 x 2 VDFN 8-Lead

Input Voltage

V_{IN} = 3.3V ± 5%

LDO Output Voltage and Current

V_{OUT} = 2.5V

I_{OUT} = 150 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +60°C

Internal Power Dissipation

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

P_{LDO} = ((3.3V x 1.05) – (2.5V x 0.975)) x 150 mA

P_{LDO} = 0.154 Watts

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to Application Note AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$

$T_{J(RISE)}$ = 0.154W x 73.1°C/W

$T_{J(RISE)}$ = 11.3°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

EXAMPLE 5-3:

$T_J = T_{J(RISE)} + T_{A(MAX)}$

T_J = 11.3°C + 60.0°C

T_J = 71.3°C

5.3.1.3 Maximum Package Power Dissipation at +60°C Ambient Temperature

EXAMPLE 5-4:

2x2 VDFN 8-Lead (73.1°C/W $R\theta_{JA}$):

$P_{D(MAX)}$ = (85°C – 60°C)/73.1°C/W

$P_{D(MAX)}$ = 0.342W

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6.0 PACKAGING INFORMATION

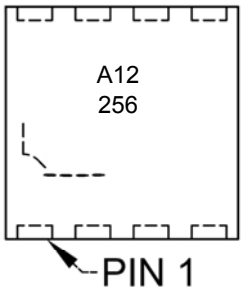
6.1 Package Marking Information

8-Lead VDFN (2 x 2 mm)

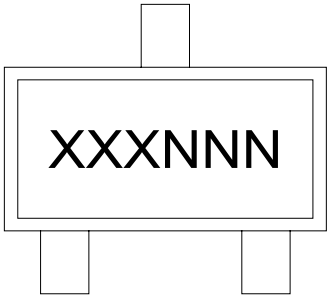


Part Number	Code
MCP1810T-12I/J8A	A12
MCP1810T-18I/J8A	A18
MCP1810T-25I/J8A	A25
MCP1810T-30I/J8A	A30
MCP1810T-33I/J8A	A33
MCP1810T-42I/J8A	A42

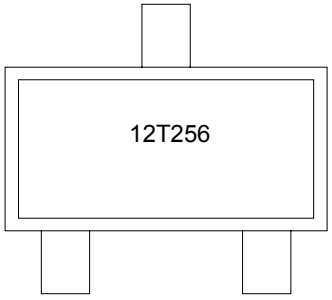
Example



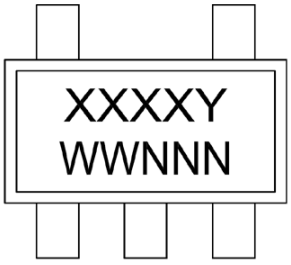
3-Lead SOT23



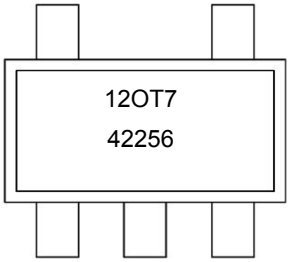
Example



5-Lead SOT23



Example

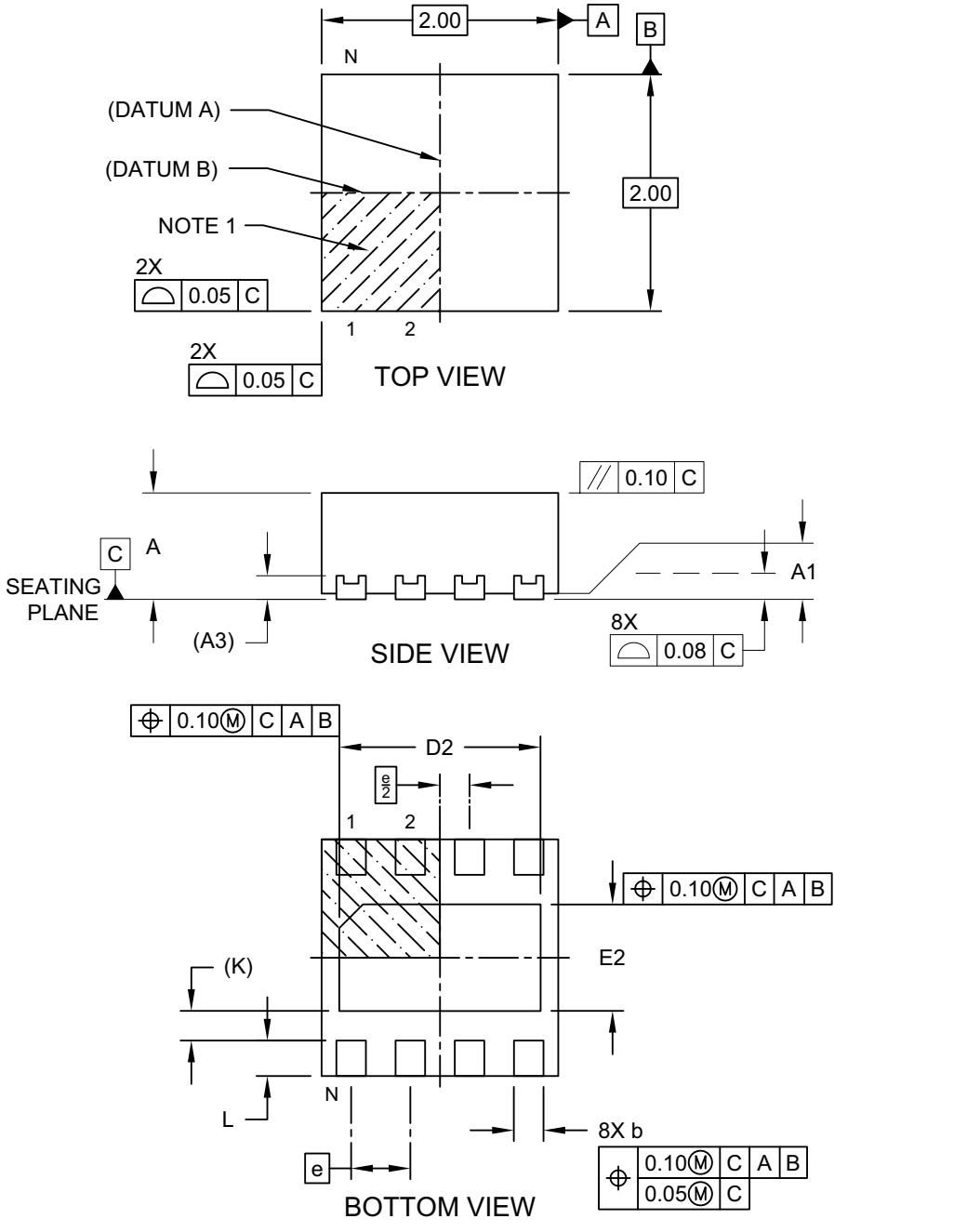


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead Package (J8A) - 2x2 mm Body [VDFN] With 1.7x0.9 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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8-Lead Very Thin Plastic Dual Flat, No Lead Package (J8A) - 2x2 mm Body [VDFN] With 1.7x0.9 mm Exposed Pad

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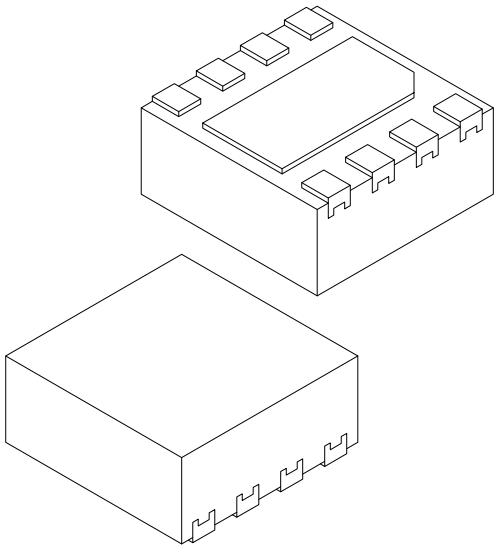

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.65	1.70	1.75
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.85	0.90	0.95
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1207A Sheet 2 of 2

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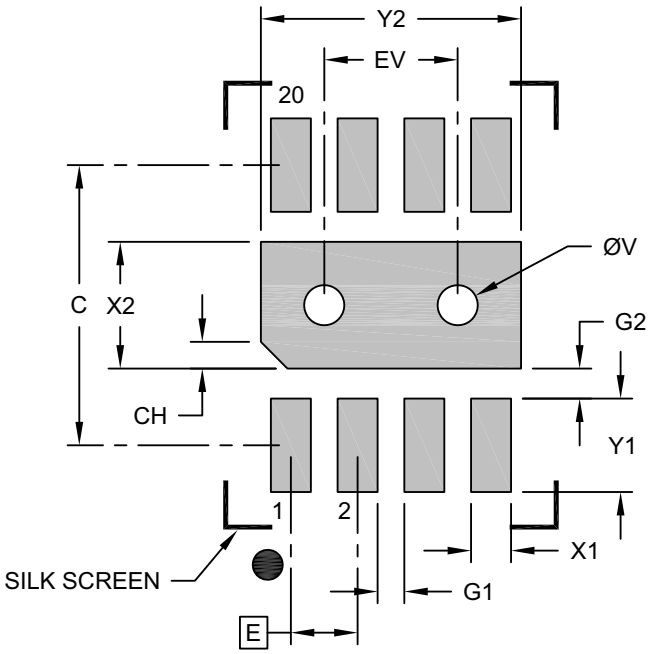
8-Lead Very Thin Plastic Dual Flat, No Lead Package (J8A) - 2x2 mm Body [VDFN] With 1.7x0.9 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			0.95
Optional Center Pad Length	Y2			1.95
Contact Pad Spacing	C		2.10	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.70
Contact Pad to Pad (X6)	G1	0.20		
Contact Pad to Center Pad (X8)	G2	0.23		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3207A

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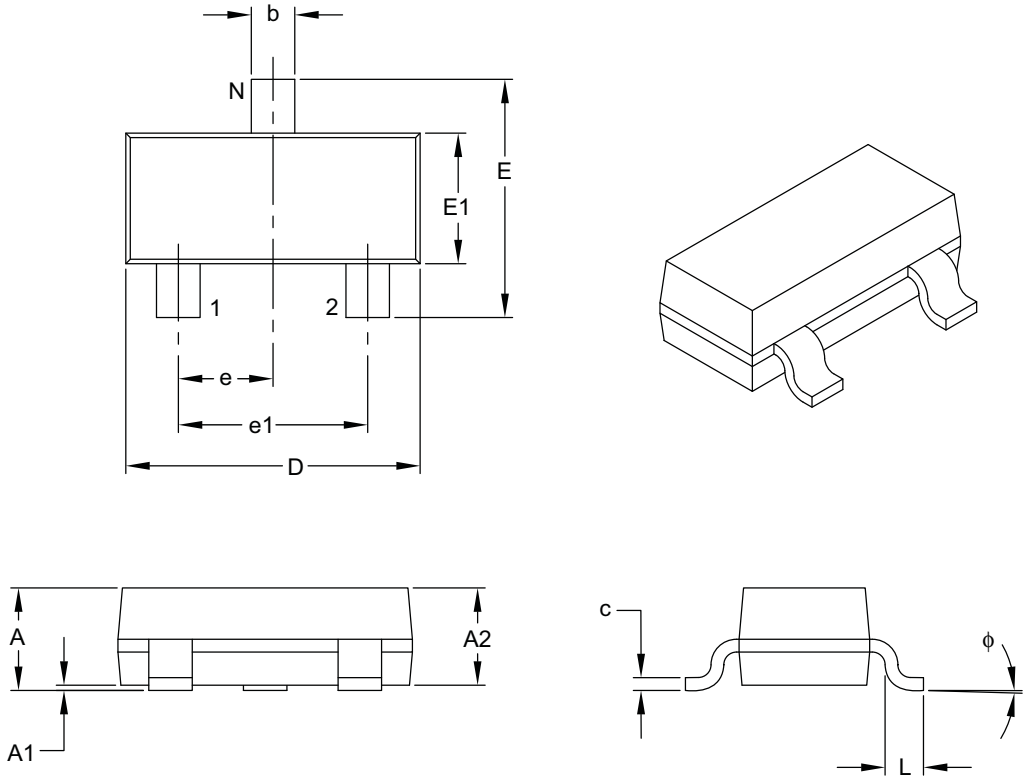
3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

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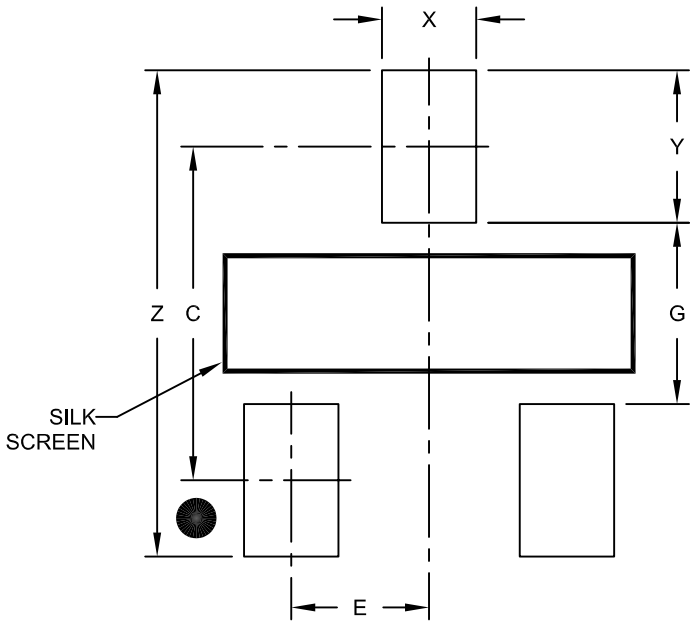

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X			0.65
Contact Pad Length (X3)	Y			1.05
Distance Between Pads	G	1.25		
Overall Width	Z			3.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2104A

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5-Lead Plastic Small Outline Transistor (OT) [SOT23]

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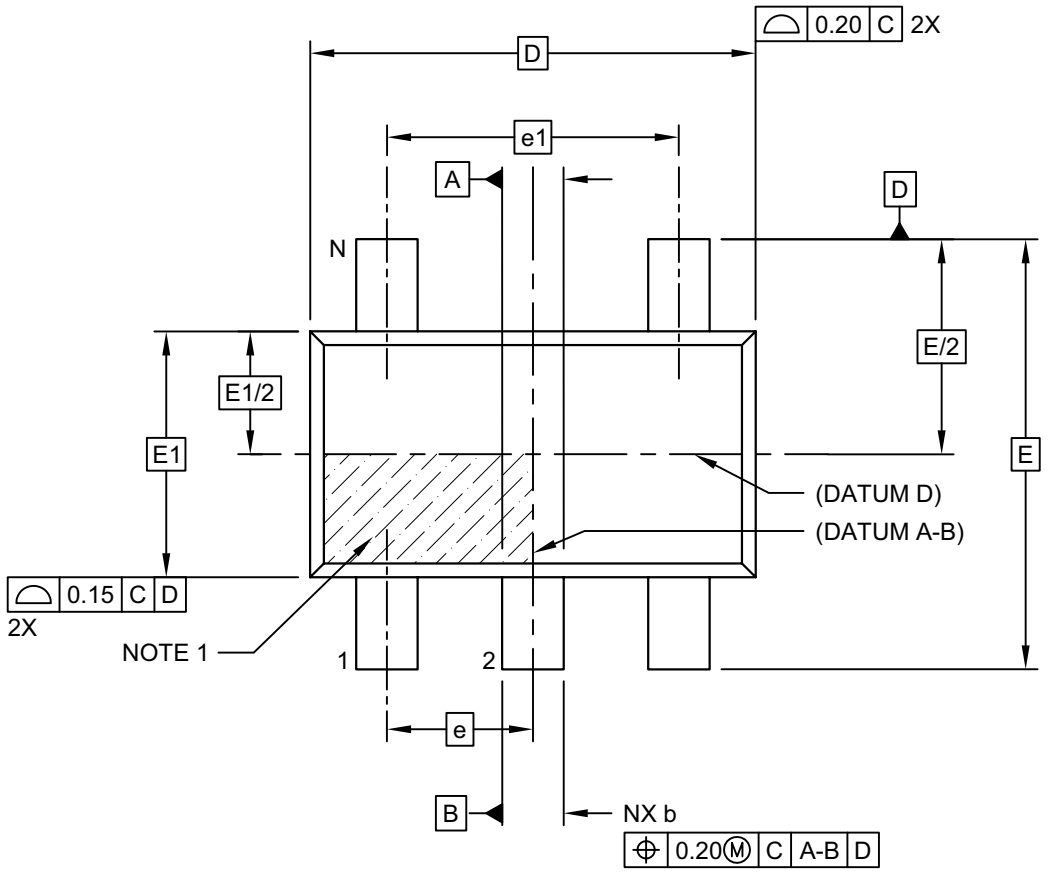
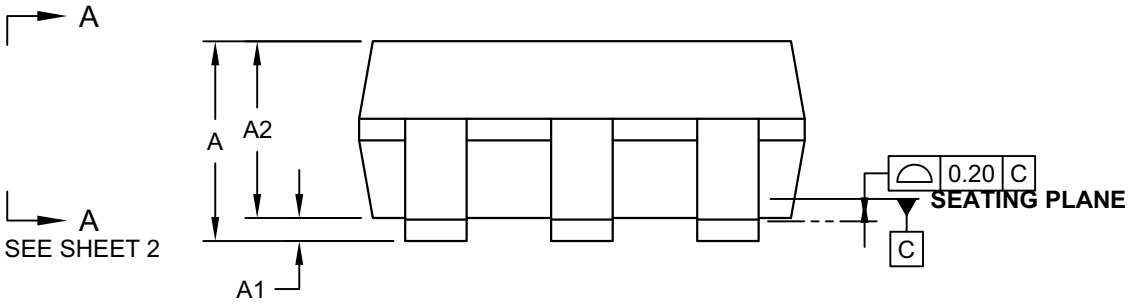


TOP VIEW

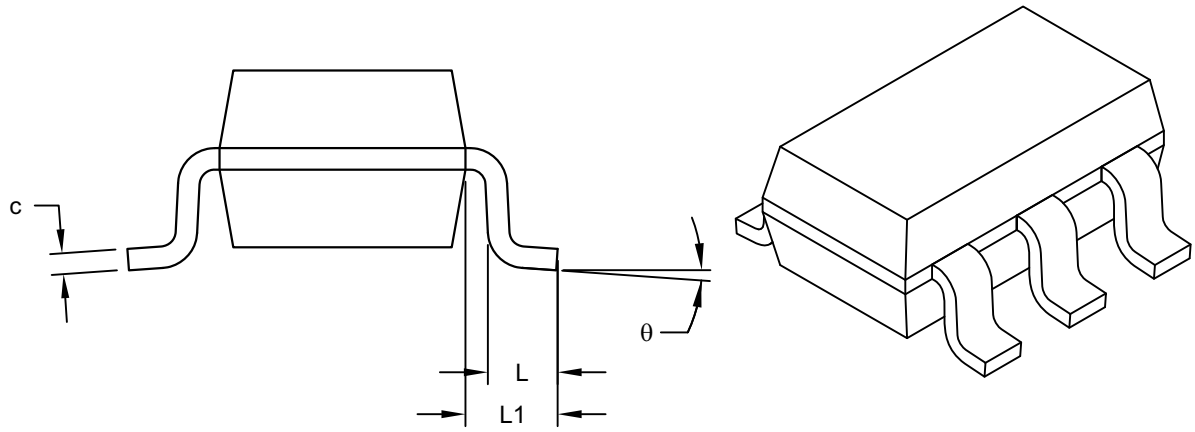


SIDE VIEW

Microchip Technology Drawing C04-028D [OT] Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091D [OT] Sheet 2 of 2

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5-Lead Plastic Small Outline Transistor (OT) [SOT23]

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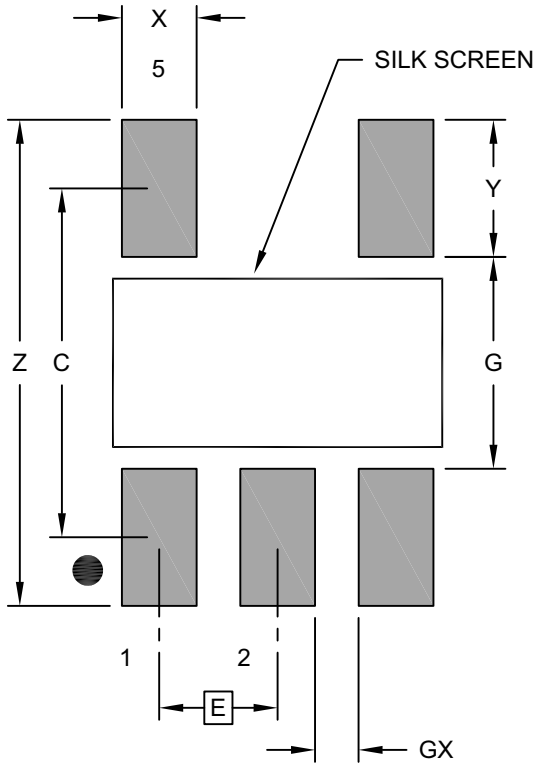

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A [OT]

NOTES:

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APPENDIX A: REVISION HISTORY

Revision B (January 2018)

The following is the list of modifications:

1. Added more Standard Output Voltages in the Features, Description, AC/DC Characteristics, Device Overview sections.
2. Updated the Package Types section by adding the 3 Lead-SOT23 and 5 Lead-SOT23 packages.
3. Added two new parameters in the Temperature Specifications section, under Thermal Package Resistances.
4. Included the 3Ld-SOT23 and 5Ld-SOT23 packages in the Table 3-1.
5. Updated the Packaging Information section with two new packages: 3-Lead SOT23 and 5-Lead SOT23.
6. Updated the Product Identification System.
7. Minor typographical edits.

Revision A (September 2016)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X/	XXX
Device	Output Voltage	Temp.	Package

Device: MCP1810T: Ultra-Low Quiescent Current LDO Regulator, Tape and Reel

Standard Output Voltages*:
12 = 1.2V
15 = 1.5V
18 = 1.8V
20 = 2.0V
22 = 2.2V
25 = 2.5V
28 = 2.8V
30 = 3.0V
33 = 3.3V
35 = 3.5V
42 = 4.2V

*Contact factory for other output voltage options

Temperature: I = -40°C to +85°C (Industrial)

Package Type:
J8A = 8-Lead Very Thin Plastic Dual Flat, No Lead Package, VDFN, 8-Lead, with 1.7 x 0.9 mm Exposed Pad
TT = 3-Lead Plastic Small Outline Transistor, SOT-23
OT = 5-Lead Plastic Small Outline Transistor, SOT-23

Examples:

a) MCP1810T-12I/J8A: Tape and reel, 1.2V output voltage, Industrial temperature 8-LD VDFN package

b) MCP1810T-18I/J8A: Tape and reel, 1.8V output voltage, Industrial temperature, 8-LD VDFN package

c) MCP1810T-42I/J8A: Tape and reel, 4.2V output voltage, Industrial temperature, 8-LD VDFN package

d) MCP1810T-15I/TT: Tape and reel, 1.5V output voltage, Industrial temperature, 3-LD SOT-23 package

e) MCP1810T-20I/TT: Tape and reel, 2.0V output voltage, Industrial temperature, 3-LD SOT-23 package

f) MCP1810T-25I/TT: Tape and reel, 2.5V output voltage, Industrial temperature, 3-LD SOT-23 package

g) MCP1810T-33I/TT: Tape and reel, 3.3V output voltage, Industrial temperature, 3-LD SOT-23 package

h) MCP1810T-22I/OT: Tape and reel, 2.2V output voltage, Industrial temperature, 5-LD SOT-23 package

i) MCP1810T-28I/OT: Tape and reel, 2.8V output voltage, Industrial temperature, 5-LD SOT-23 package

j) MCP1810T-30I/OT: Tape and reel, 3.0V output voltage, Industrial temperature, 5-LD SOT-23 package

k) MCP1810T-35I/OT: Tape and reel, 3.5V output voltage, Industrial temperature, 5-LD SOT-23 package

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NOTES:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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