2N7008

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

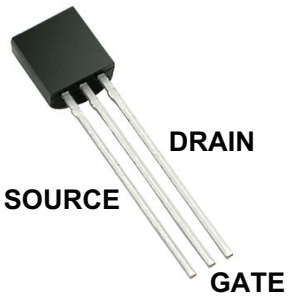
General Description

The 2N7008 is a low-threshold Enhancement-mode (normally-off) transistor that uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Type

3-lead TO-92
(Top view)



See Table 2-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage..... ±30V
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = –10 µA
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2.5	V	V_{GS} = V_{DS}, I_D = 250 µA
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±30V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{GS} = 0V, V_{DS} = 50V
		—	—	500	µA	V_{GS} = 0V, V_{DS} = 50V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	500	—	—	mA	V_{GS} = 10V, V_{DS} ≥ $2V_{DS(ON)}$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	7.5	Ω	V_{GS} = 5V, I_D = 50 mA
		—	—	7.5	Ω	V_{GS} = 10V, I_D = 500 mA

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	80	—	—	mmho	V_{DS} = 10V, I_D = 200 mA
Input Capacitance	C_{ISS}	—	—	50	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C_{OSS}	—	—	25	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	5	pF	
Turn-On Delay Time	$t_{(ON)}$	—	—	20	ns	V_{DD} = 30V, I_D = 200 mA, R_{GEN} = 25Ω
Turn-Off Delay Time	$t_{(OFF)}$	—	—	20	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.5	V	V_{GS} = 0V, I_{SD} = 150 mA (**Note 1**)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

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TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-92	θ_{JA}	—	132	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at T_A = 25°C (W)	I_{DR} (Note 1) (mA)	I_{DRM} (A)
3-lead TO-92	230	1.3	1	230	1.3

Note 1: I_D (continuous) is limited by maximum T_J.

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2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in 2N7008.
Refer to **Package Type** for the location of the pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

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3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for 2N7008.

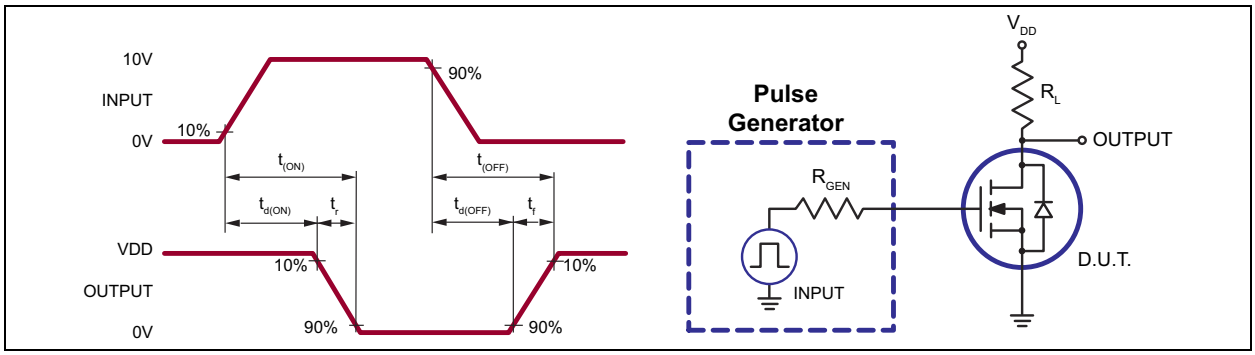


FIGURE 3-1: *Switching Waveforms and Test Circuit.*

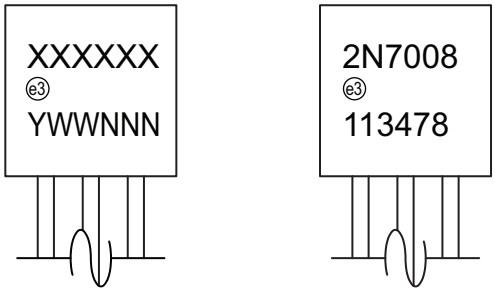
TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (mA)
60	7.5	500

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

3-lead TO-92 Example

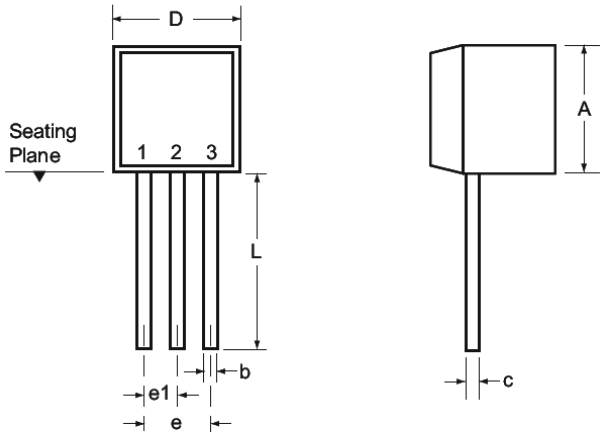


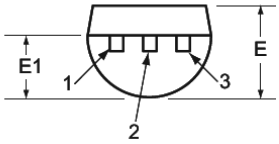
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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3-Lead TO-92 Package Outline (L/LL/N3)





Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2021)

- Converted Supertex Doc# DSFP-2N7008 to Microchip DS20005800A
- Changed the package marking format
- Removed the TO-92 N3 P002, P003, P005, P013, and P014 media types to align package specifications with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	2N7008	=	N-Channel Enhancement-Mode Vertical DMOS FET
Package:	N3	=	3-lead TO-92
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	1000/Bag for an N3 Package

Examples:

a) 2N7008N3-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag

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