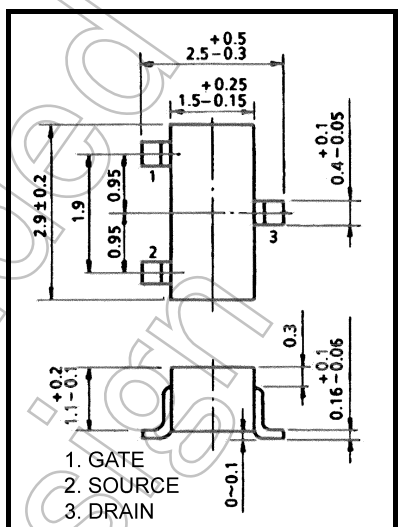
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

2SJ168

High Speed Switching Applications
Analog Switch Applications
Interface Applications

- Excellent switching time: t_{on} = 14 ns (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 100 mS (min) @I_D = −50 mA
- Low on resistance: $R_{DS\ (ON)}$ = 1.3 Ω (typ.) @ I_D = −50 mA
- Enhancement-mode
- Complementary to 2SK1062

Unit: mm



S-MINI

JEDEC	—
JEITA	SC-59
TOSHIBA	2-3F1F

Weight: 0.012 g (typ.)

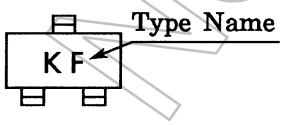
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	−200	mA
	Pulse	I_{DP}	−800	
Drain power dissipation (Ta = 25°C)		P_D	200	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: This transistor is the electrostatic sensitive device. Please handle with caution.

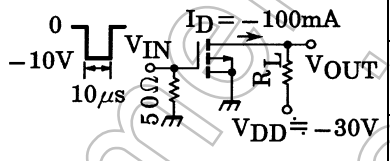
Marking



Not Recommended for New Design

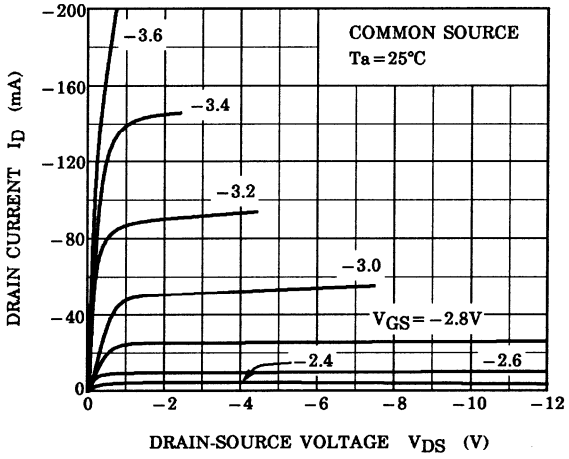
Start of commercial production
1988-06

Electrical Characteristics (Ta = 25°C)

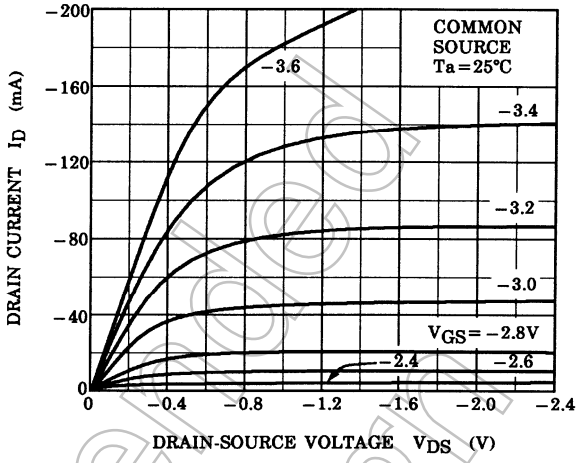
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±100	nA
Drain cut-off current		I_{DSS}	V_{DS} = −60 V, V_{GS} = 0	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−2	—	−3.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −50 mA	100	—	—	mS
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = −50 mA, V_{GS} = −10 V	—	1.3	2.0	Ω
Drain-source ON voltage		$V_{DS\ (ON)}$	I_D = −50 mA, V_{GS} = −10 V	—	−65	−100	mV
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	73	85	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	15	22	pF
Output capacitance		C_{oss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	48	60	pF
Switching time	Rise time	t_r		—	8	—	ns
	Turn-on time	t_{on}		—	14	—	
	Fall time	t_f		—	35	—	
	Turn-off Time	t_{off}	V_{IN}: t_r, t_f < 5 ns D.U. ≤ 1% (Z_{out} = 50 Ω)	—	100		

Not Recommended for New Design

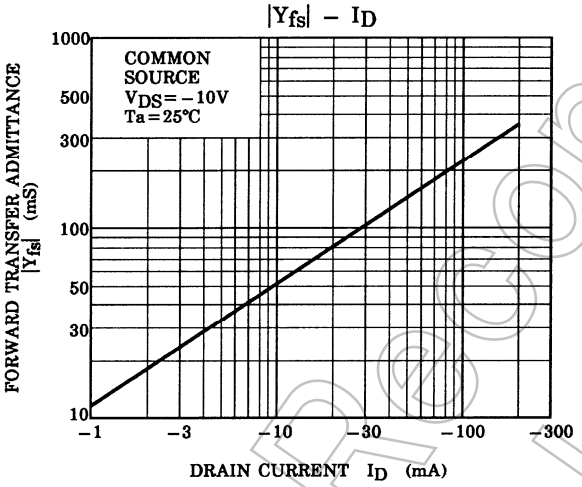
$I_D - V_{DS}$



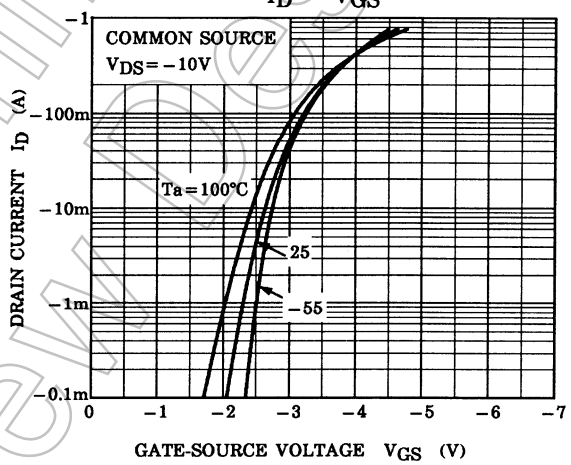
$I_D - V_{DS}$ (LOW VOLTAGE REGION)



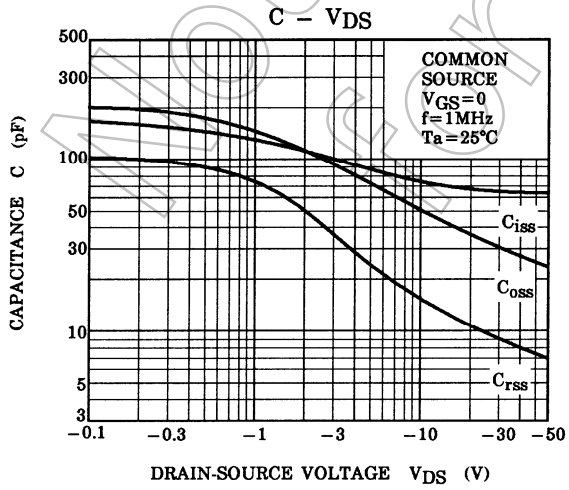
$|Y_{fs}| - I_D$



$I_D - V_{GS}$

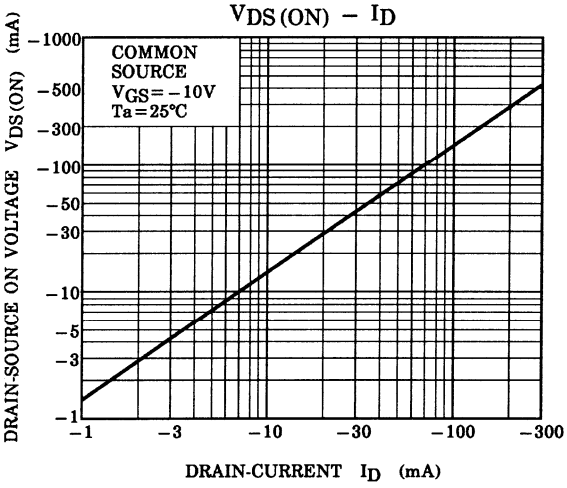


$C - V_{DS}$

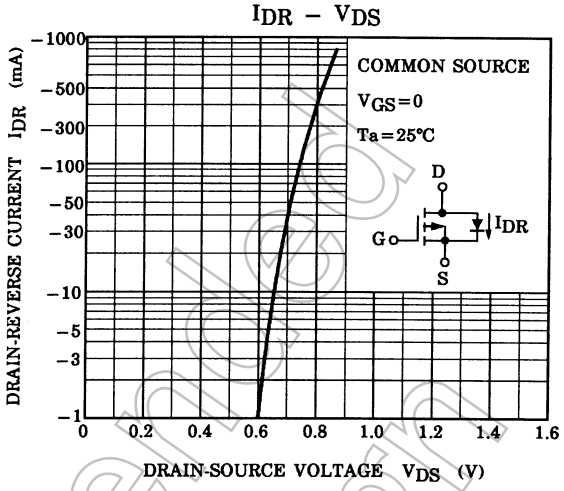


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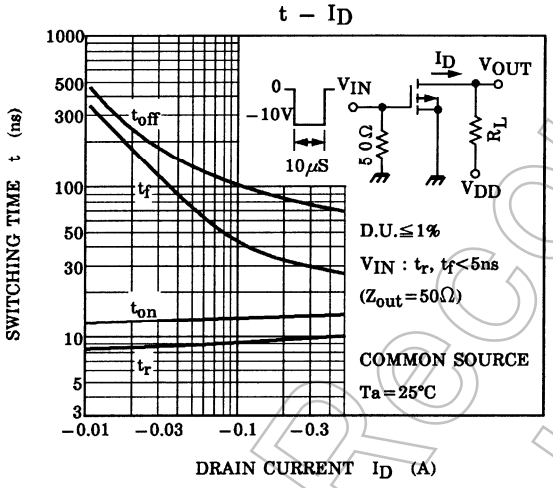
$V_{DS\,(ON)}$ – I_D



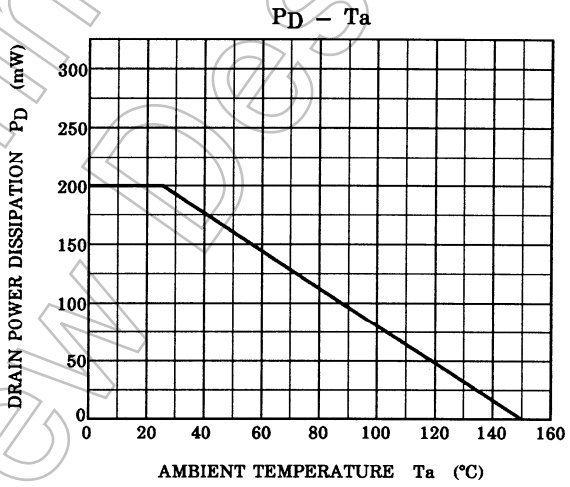
I_{DR} – V_{DS}



t – I_D



P_D – Ta



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