To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR
2SJ649

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ649 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ649	Isolated TO-220

FEATURES

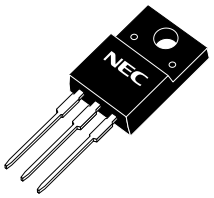
- Low on-state resistance:

  $R_{DS(on)1}$ = 48 mΩ MAX. (V_{GS} = –10 V, I_D = –10 A)

  $R_{DS(on)2}$ = 75 mΩ MAX. (V_{GS} = –4.0 V, I_D = –10 A)
- Low input capacitance:

  C_{iss} = 1900 pF TYP. (V_{DS} = –10 V, V_{GS} = 0 V)
- Built-in gate protection diode

(Isolated TO-220)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓20	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓70	A
Total Power Dissipation (T_C = 25°C)	P_T	25	W
Total Power Dissipation (T_A = 25°C)	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	–20	A
Single Avalanche Energy Note2	E_{AS}	40	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = –30 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

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Date Published May 2003 NS CP(K)
Printed in Japan

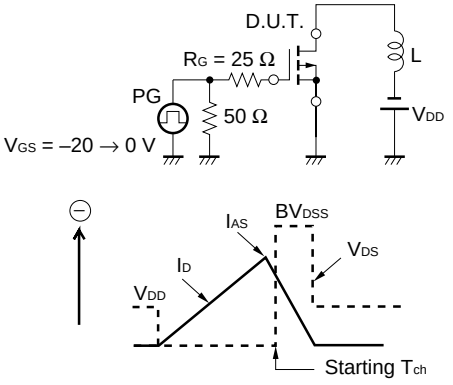
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

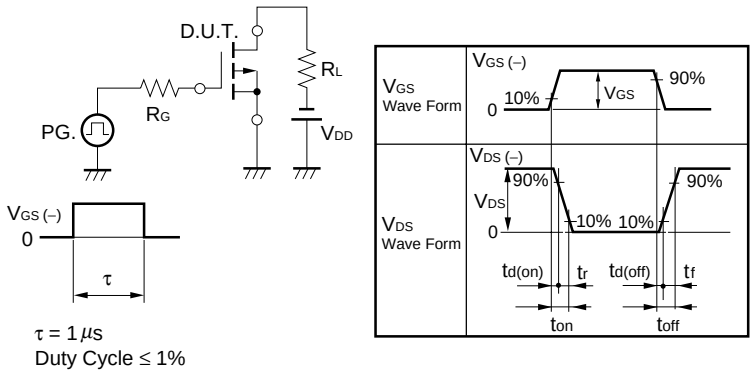
Characteristics	Symbol	Test Condtions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.5	–2.0	–2.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –10 A	10	20		S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –10 A		38	48	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –10 A		47	75	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		1900		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		350		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		140		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –30 V, I_D = –10 A		10		ns
Rise Time	t_r	V_{GS} = –10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		73		ns
Fall Time	t_f			17		ns
Total Gate Charge	Q_G	V_{DD} = –48 V		38		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		7		nC
Gate to Drain Charge	Q_{GD}	I_D = –20 A		10		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 20 A, V_{GS} = 0 V		0.95		V
Reverse Recovery Time	t_{rr}	I_F = 20 A, V_{GS} = 0 V		49		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		100		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

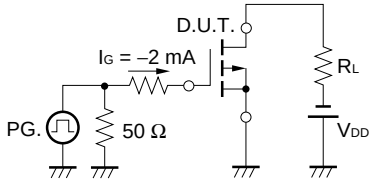
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

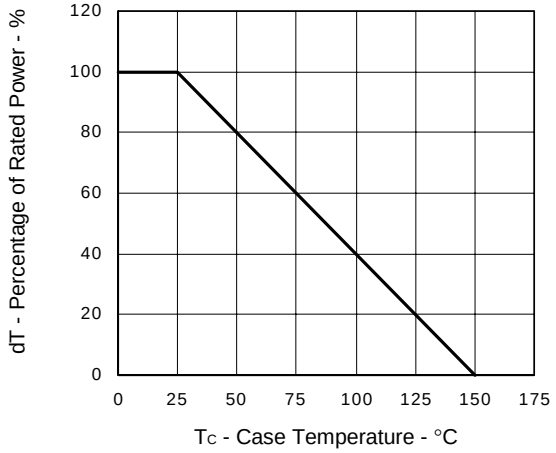


TEST CIRCUIT 3 GATE CHARGE

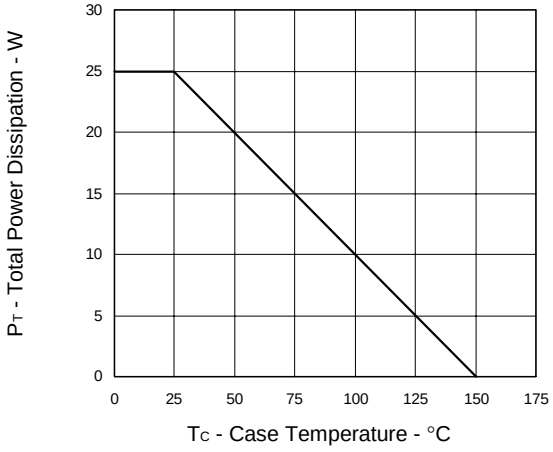


TYPICAL CHARACTERISTICS (T_A = 25°C)

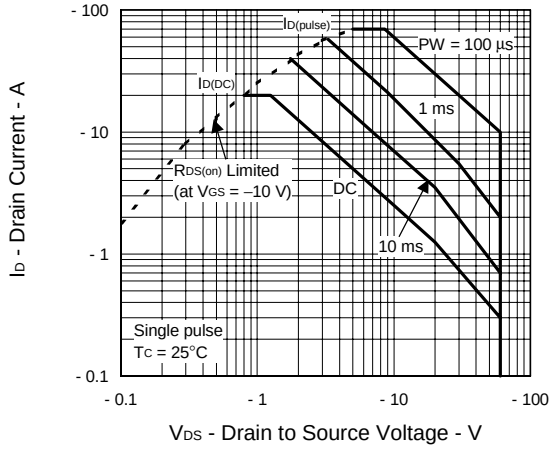
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



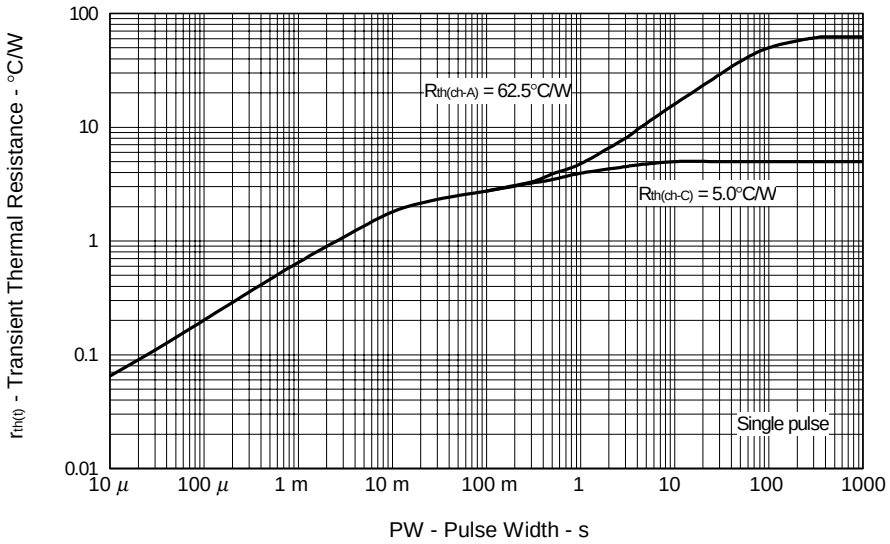
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



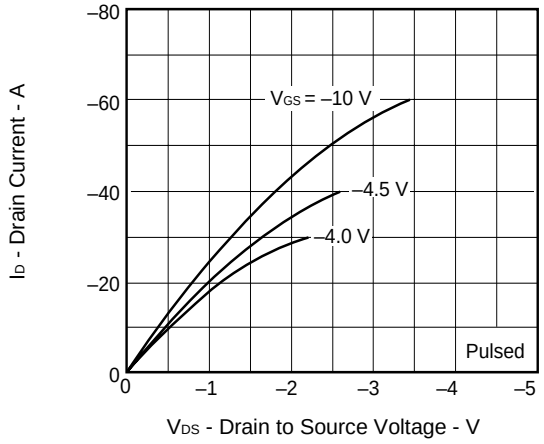
FORWARD BIAS SAFE OPERATING AREA



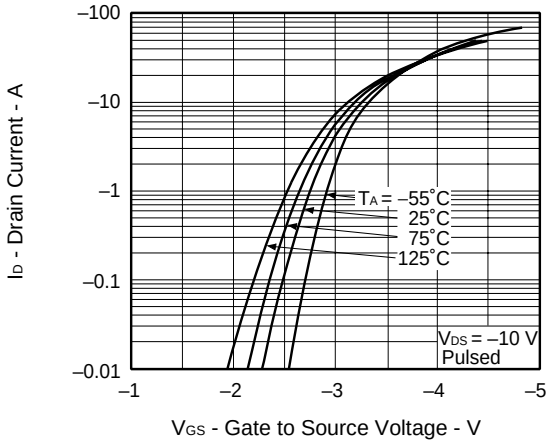
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



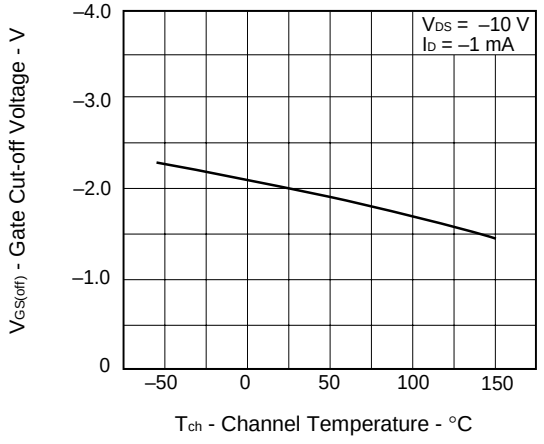
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



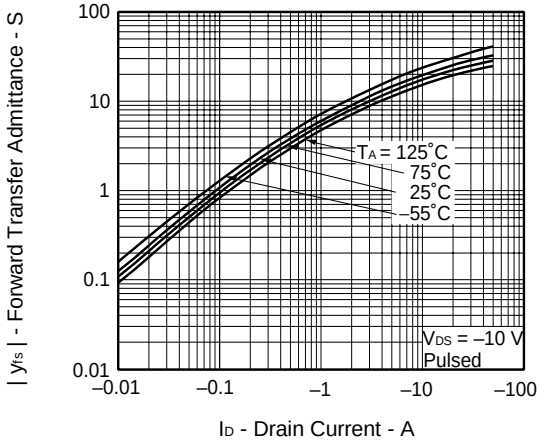
FORWARD TRANSFER CHARACTERISTICS



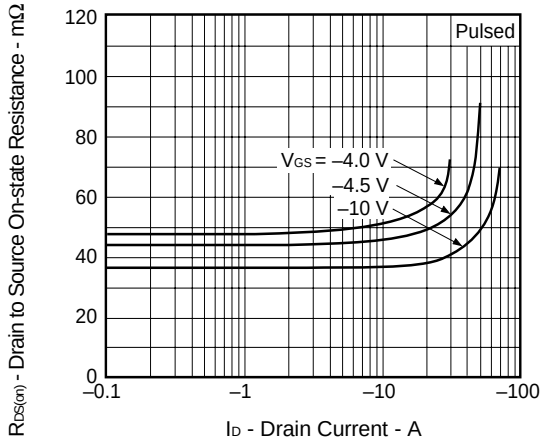
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



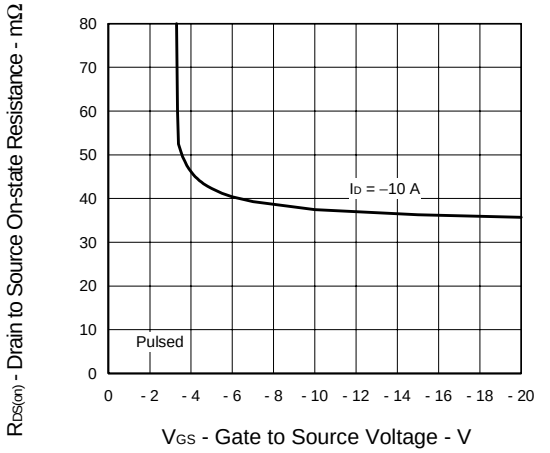
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



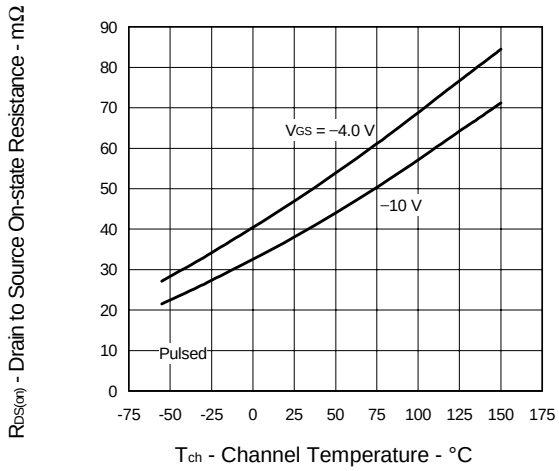
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



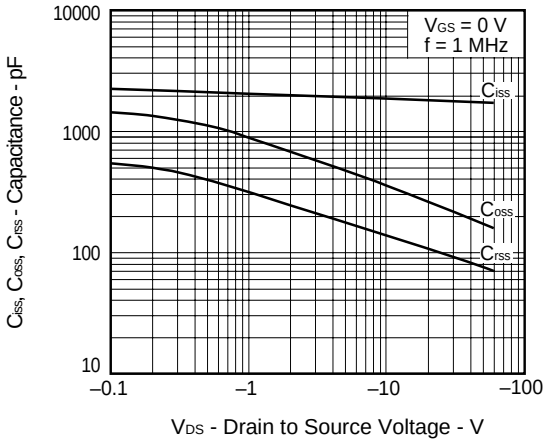
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



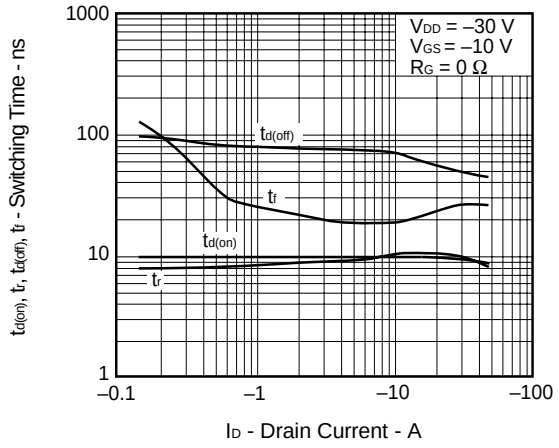
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



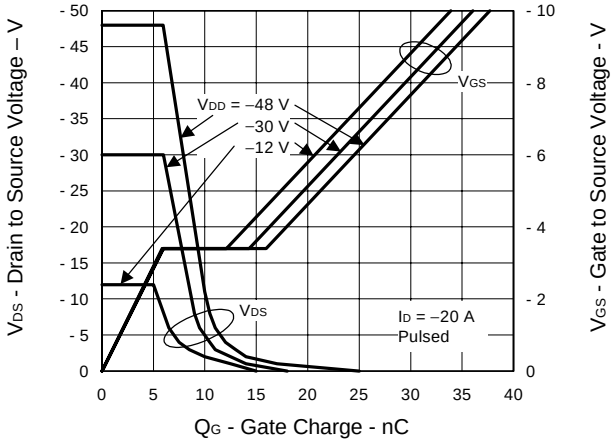
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



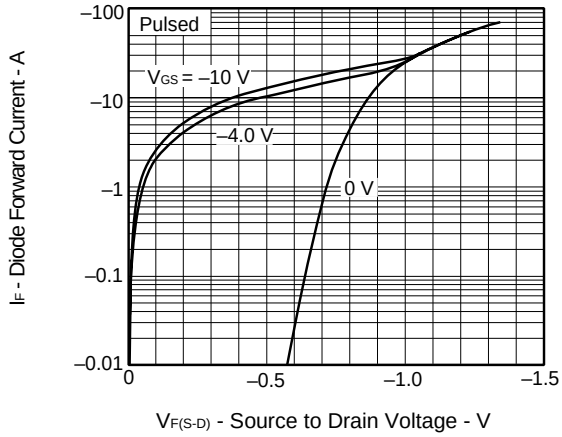
SWITCHING CHARACTERISTICS



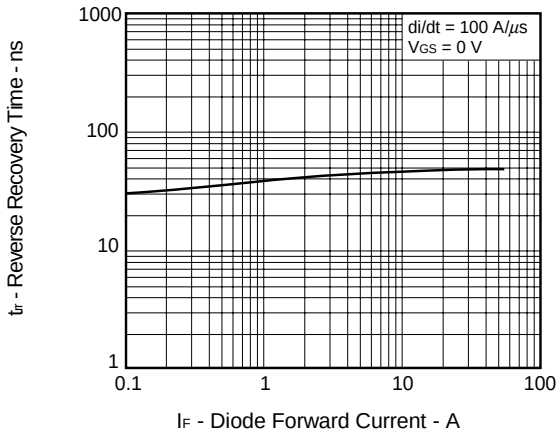
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



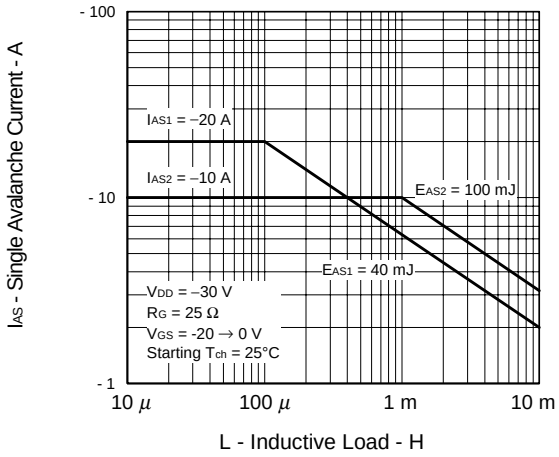
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



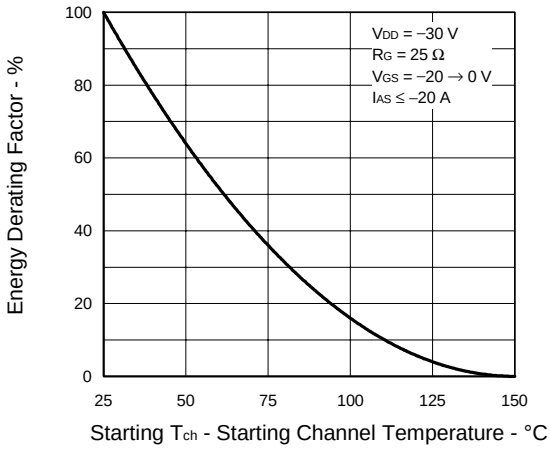
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

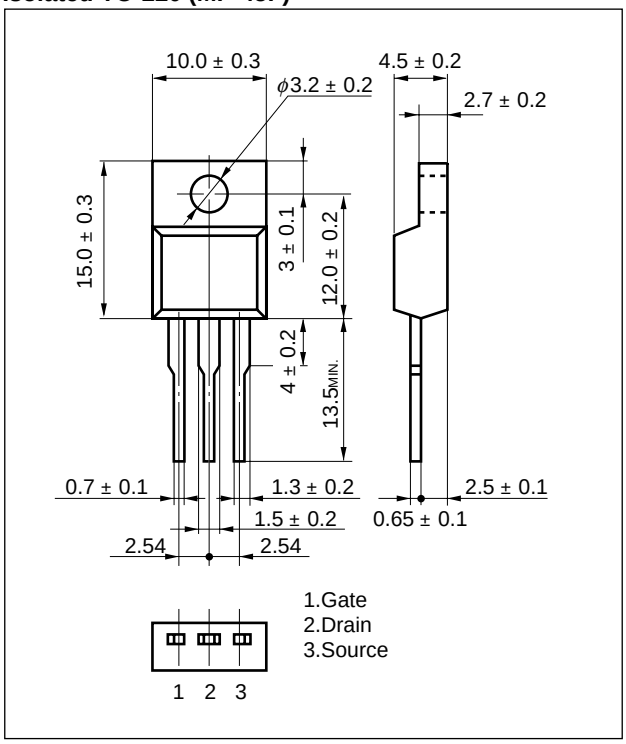


SINGLE AVALANCHE ENERGY
DERATING FACTOR

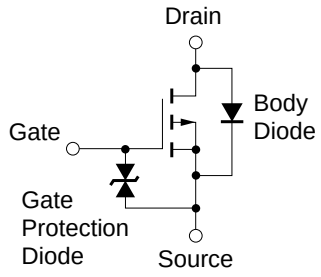


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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