UMW AO3413A

20V P-Channel MOSFET

1.Description

The AO3413A uses advanced trench technology to provide excellent Rps(on), low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

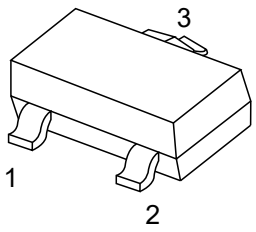
2.Features

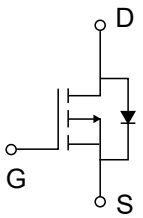
- $V_{DS\ (V)}$= -20V
- I_D=-3A(V_{GS}=-4.5V)
- $R_{DS(ON)}$<66mΩ(V_{GS}=-4.5V)
- $R_{DS(ON)}$<80mΩ(V_{GS}=-2.5V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [A]	T_A=25°C	I_D	-3	A
	T_A=70°C		-2.4	
Pulsed Drain Current [B]		I_{DM}	-15	
Power Dissipation [A]	T_A=25°C	P_D	1.4	W
	T_A=70°C		0.9	
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		100	125	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	63	80	°C/W

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±8V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.4	-0.65	-1	V
On state drain current	$I_{D(ON)}$	V_{GS}=-4.5V, V_{DS}=-5V	-15			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-3A			66	mΩ
		V_{GS}=-2.5V, I_D=-2.6A			80	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-3A		12		S
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.7	-1	V
Maximum Body-Diode Continuous Current	I_S				-1.4	A
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-10V, f=1MHz		560	745	pF
Output Capacitance	C_{oss}			80		pF
Reverse Transfer Capacitance	C_{rss}			70		pF
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		15	23	Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_g	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-3A		8.5	11	nC
Gate Source Charge	Q_{gs}			1.2		nC
Gate Drain Charge	Q_{gd}			2.1		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=-10V, R_L=3.3Ω,R_{GEN}=6Ω		7.2		ns
Turn-On Rise Time	t_r			36		ns
Turn-Off DelayTime	$t_{D(off)}$			53		ns
Turn-Off Fall Time	t_f			56		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=-3A, dI/dt=100A/μs		37	49	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-3A, dI/dt=100A/μs		27		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.The current rating is based on the t ≤10s thermal resistance rating.

B. Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 300μs pulse width, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

7.1TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

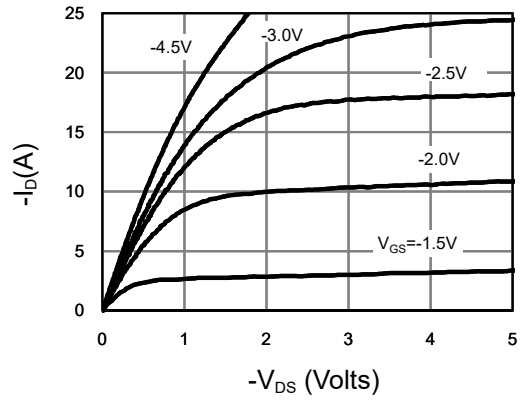


Fig 1: On-Region Characteristics (Note E)

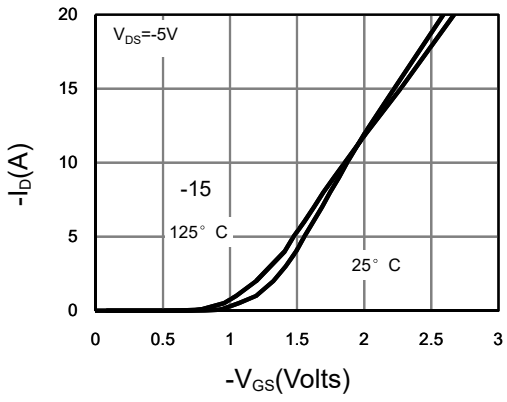


Figure 2: Transfer Characteristics (Note E)

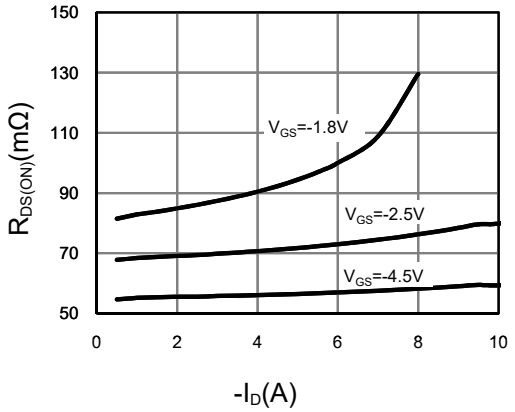


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

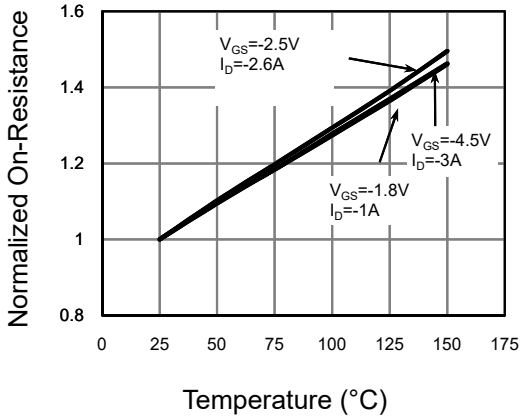


Figure 4: On-Resistance vs. Junction Temperature (Note E)

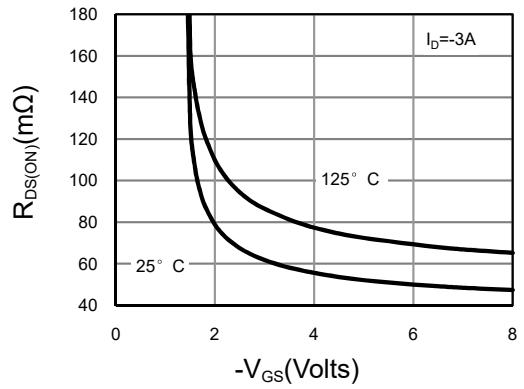


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

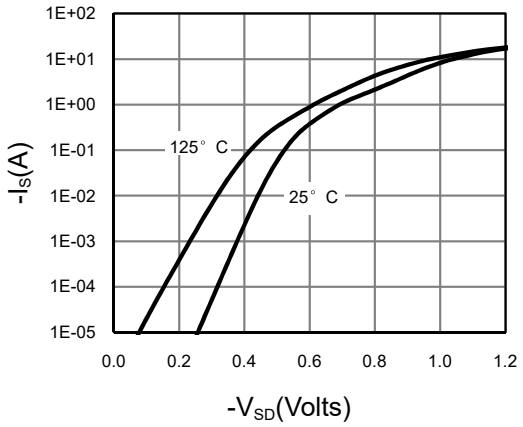


Figure 6: Body-Diode Characteristics(Note E)

7.2TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

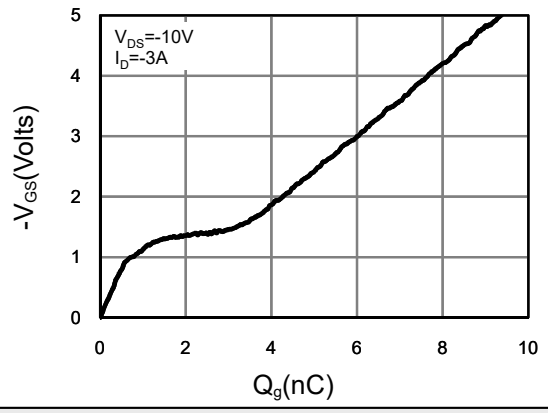


Figure 7: Gate-Charge Characteristics

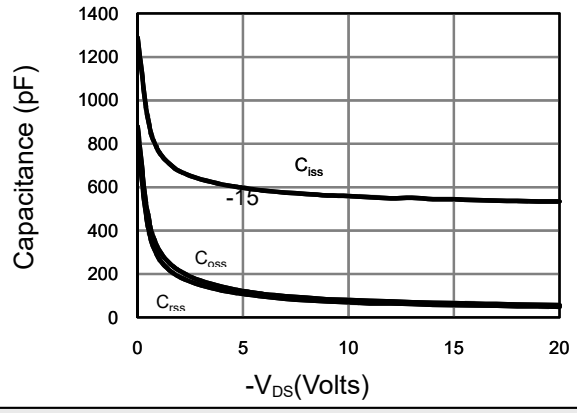


Figure 8: Capacitance Characteristics

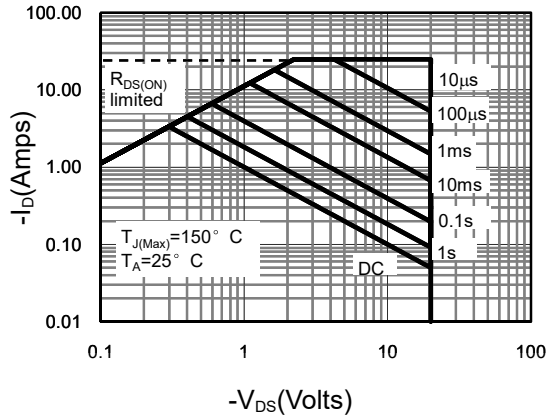


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

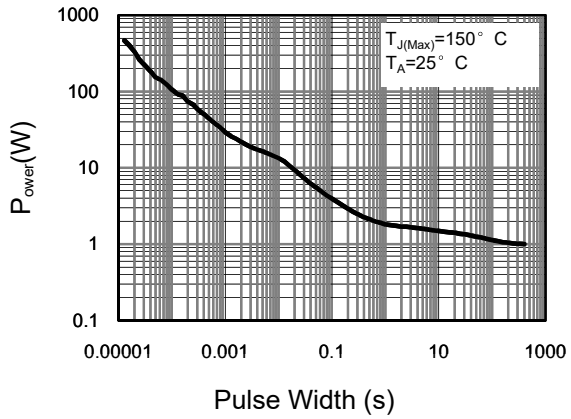


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

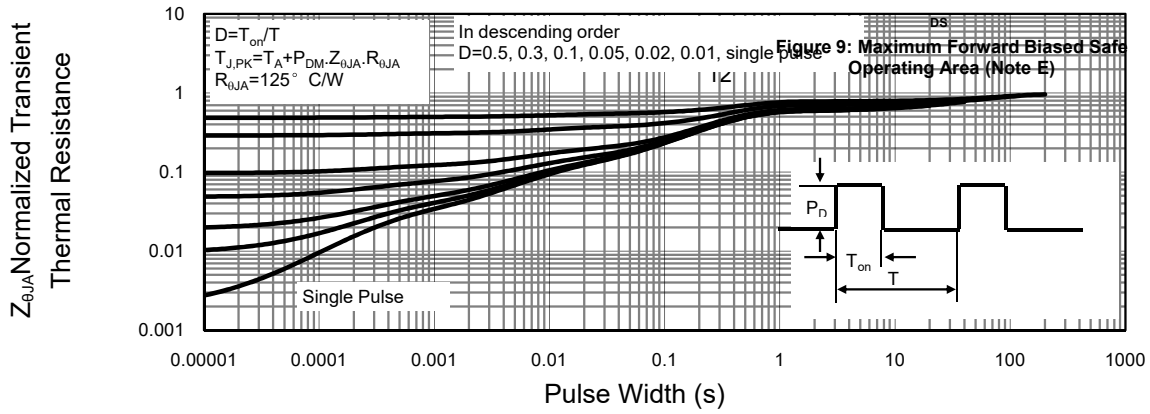
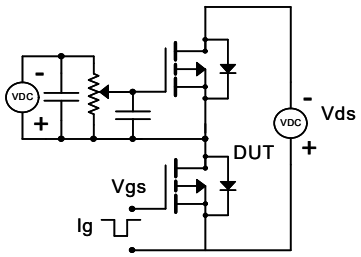
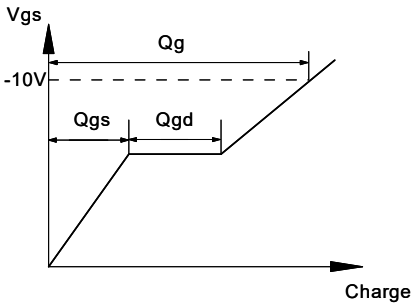


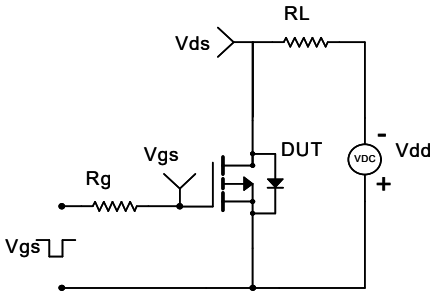
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

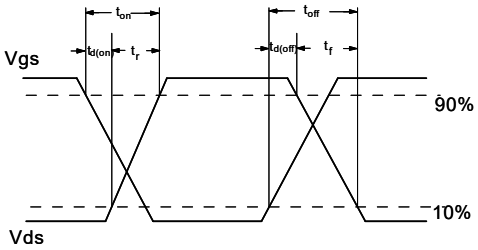
Gate Charge Test Circuit & Waveform



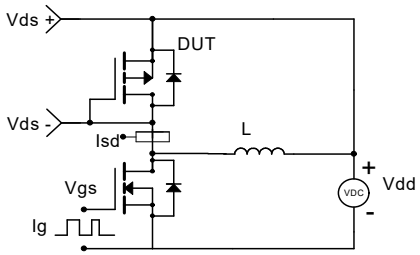


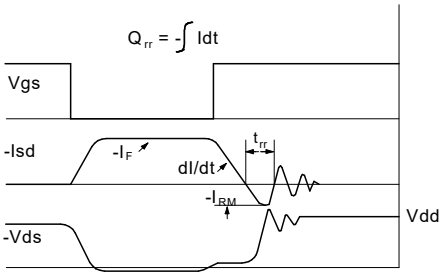
Resistive Switching Test Circuit & Waveforms



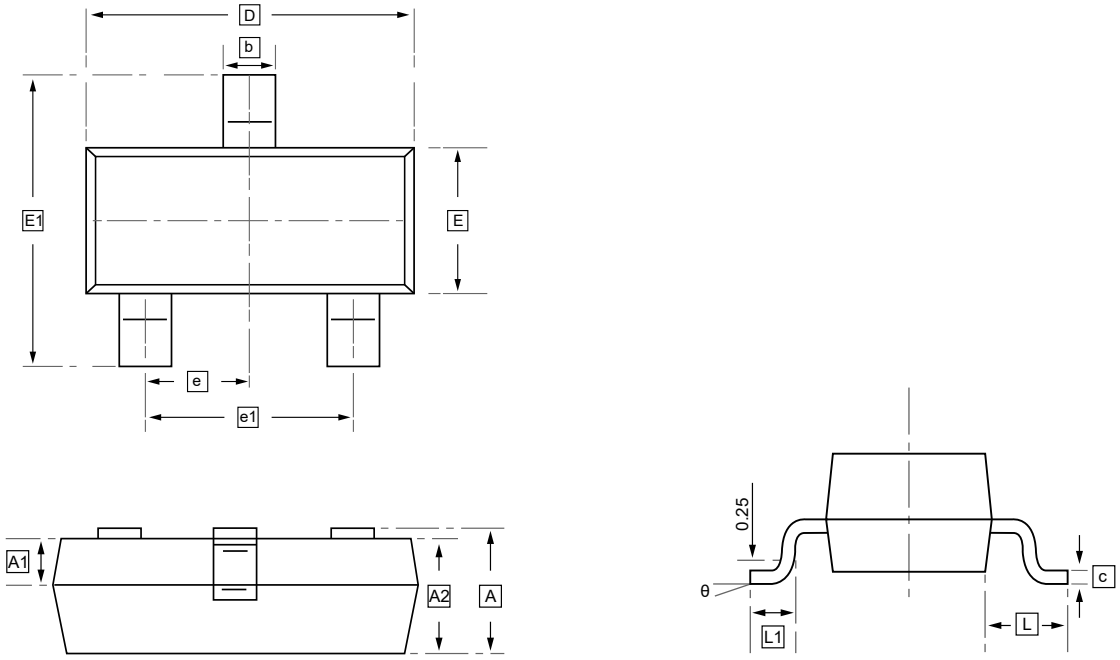


Diode Recovery Test Circuit & Waveforms





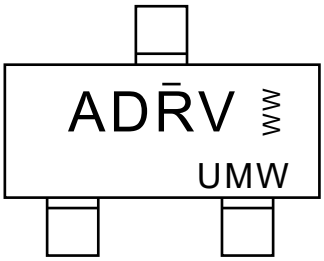
8.SOT-23 PACKAGE OUTLINE DIMENSIONS



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	L1	θ
Min	0.900	0.000	0.900	0.300	0.080	2.800	1.200	2.250	0.950	1.800	0.550	0.300	0°
Max	1.150	0.100	1.050	0.500	0.150	3.000	1.400	2.550	TYP.	2.000	REF.	0.500	8°

9.Ordering information



WW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO3413A	SOT-23	3000	Tape and reel

10.Disclaimer

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