MIC47050

500 mA ULDO with Low Input and Low Output Voltage

Features

- Voltage Range
  - Input Voltage: 1.0V to 3.6V
  - Bias Voltage: 2.3V to 5.5V
- 0.4V to 2.0V Output Voltage Range
- Low Dropout Voltage of 44 mV at 500 mA
- ±1.5% Initial Output Voltage Accuracy
- High Bandwidth, Very Fast Transient Response
- Stable with a 1 µF Ceramic Output Capacitor
- Logic Level Enable Input
- UVLO on both Supply Voltages
- Available in Thermally Enhanced 2 mm x 2 mm DFN and TDFN Packages
- –40°C to +125°C Junction Temperature Range
- AEC-Q100 Qualified and PPAP Capable Available for DFN Package Only

Applications

- Point-of-Load Applications
- PDAs, Notebooks, and Desktops
- Datacom and Telecom Systems
- DSP, PLD and FPGA Power Supply
- Low Voltage Post Regulation

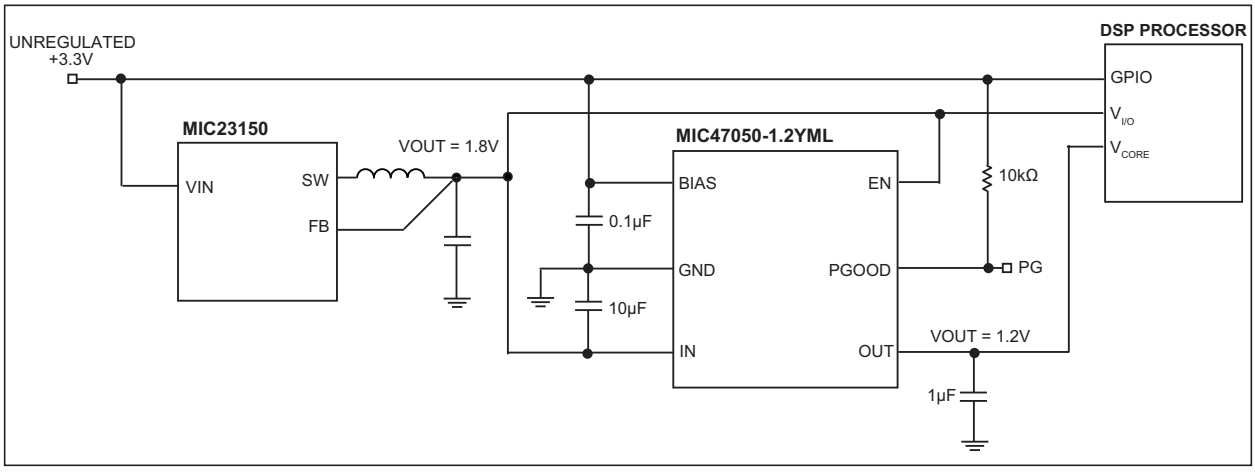
General Description

The MIC47050 is a high speed, ultra-low dropout (ULDO), dual supply NMOS regulator designed to take advantage of point-of-load applications that use multiple supply rails to generate a low voltage, high-current power supply. The MIC47050 can source 500 mA of output current while only requiring a 1 µF ceramic output capacitor for stability. A 1.5% output voltage accuracy, low dropout voltage (44 mV @ 500 mA), and low ground current makes this device ideally suited for mobile and point-of-load applications.

The MIC47050 has an NMOS output stage that offers very low output impedance. The NMOS output stage makes for a unique ability to respond very quickly to sudden load changes such as that required by a microprocessor, DSP, or FPGA. The MIC47050 consumes little quiescent current and can be used for driving the core voltages of mobile processors, post regulating a core DC/DC converter in any processor.

The MIC47050 is available in fixed and adjustable output voltages in a tiny 2 mm x 2 mm DFN and TDFN packages with an operating junction temperature range of –40°C to +125°C.

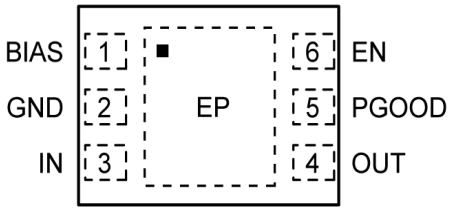
Typical Application Circuit



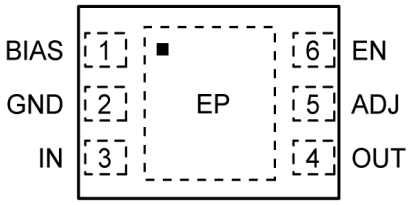
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Package Types

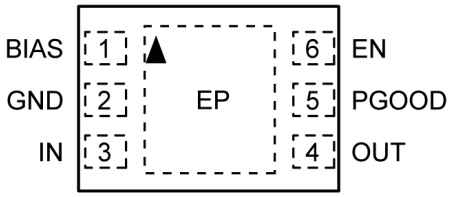
MIC47050
6-Pin 2 mm x 2 mm DFN Fixed (ML)
Top View



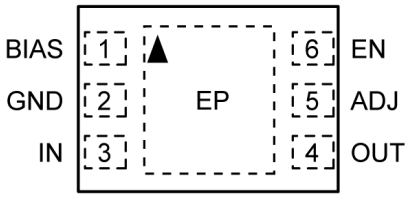
MIC47050
6-Pin 2 mm x 2 mm DFN Adjustable (ML)
Top View



MIC47050
6-Pin 2 mm x 2 mm TDFN Fixed (MT)
Top View



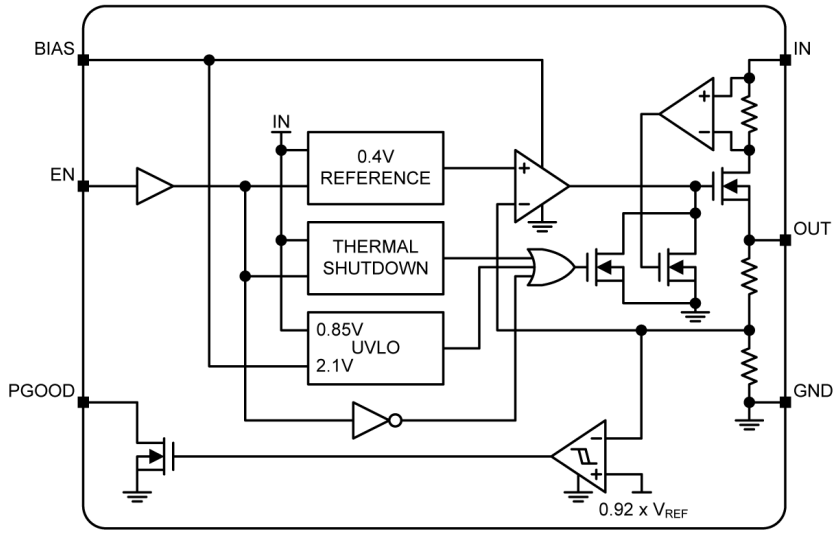
MIC47050
6-Pin 2 mm x 2 mm TDFN Adjustable (MT)
Top View



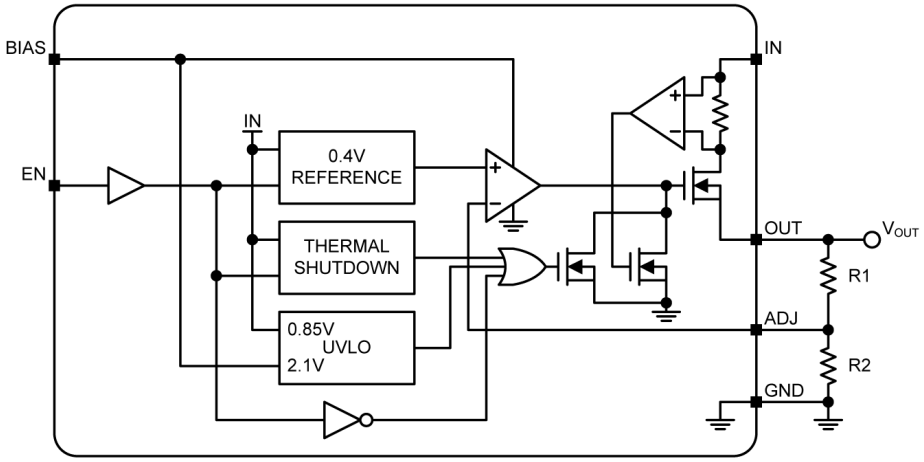
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Functional Block Diagrams

MIC47050 Fixed Output



MIC47050 Adjustable Output



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

IN Supply Voltage (V_{IN}) ..... –0.3V to +4V
Bias Supply Voltage (V_{BIAS}) ..... –0.3V to +6V
Enable Voltage (V_{EN}) ..... –0.3V to +6V
Power Good Voltage (V_{PGOOD}) ..... –0.3V to +6V
ADJ Pin Voltage (V_{ADJ}) ..... –0.3V to +6V
OUT Pin Voltage (V_{OUT}) ..... –0.3V to V_{IN}
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ‡

IN Supply Voltage (V_{IN}) ..... +1.0V to +3.6V (V_{IN} < V_{BIAS})
Bias Voltage (V_{BIAS}) ..... +2.3V to +5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{BIAS}
Power Good Voltage (V_{PGOOD}) ..... .0V to V_{BIAS}
Output Voltage Range ..... +0.4V to +2.0V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{OUT} + 0.5V$; $V_{BIAS} = V_{OUT} + 2.1V$; $C_{OUT} = 1\ \mu F$; $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **Bold** values indicate $–40°C \le T_J \le +125°C$; unless otherwise noted. Specification for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Supply						
Input Voltage Range	V_{IN}	**1.0**	—	**3.6**	V	—
V_{IN} UVLO Threshold (Note 1)	V_{IN_UVLO}	**0.7**	0.85	**1.0**	V	V_{IN} Rising
V_{IN} UVLO Hysteresis (Note 2)	$V_{IN_UVLO_HYST}$	—	40	—	mV	—
Ground Current in Shutdown	I_{GND}	—	0.1	**1.0**	µA	$V_{EN} \le 0.2V$ (Regulator Shutdown)
IN Bias Current	I_{IN}	—	6	**15**	µA	I_{OUT} = 500 mA; $V_{IN} = V_{OUT}$ + 0.5V
BIAS Supply						
BIAS Input Voltage	V_{BIAS}	**2.3**	—	**5.5**	V	—
V_{BIAS} UVLO Threshold (Note 1)	BIAS_UVLO	**1.7**	2.1	**2.3**	V	V_{BIAS} Rising
V_{BIAS} UVLO Hysteresis (Note 2)	BIAS_UVLO_HYS	—	75	—	mV	—
Dropout Voltage	$V_{BIAS} - V_{OUT}$	—	1.15	—	V	I_{OUT} = 100 mA (Note 2)
		—	1.25	**2.1**		I_{OUT} = 500 mA
V_{BIAS} Supply Current	I_{BIAS}	—	330	**500**	µA	I_{OUT} = 1 mA; $V_{BIAS} = V_{OUT}$ + 2.1V

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 0.5V$; $V_{BIAS} = V_{OUT} + 2.1V$; $C_{OUT} = 1\ \mu F$; $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **Bold** values indicate $–40°C \le T_J \le +125°C$; unless otherwise noted. Specification for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{BIAS} Supply Current in Shutdown (I_{BIAS})	I_{BIAS_SHDN}	—	0.1	**1.0**	µA	$V_{EN} \le 0.2V$ (Regulator Shutdown)
Output Voltage						
Dropout Voltage	$V_{IN} - V_{OUT}$	—	9	**50**	mV	I_{OUT} = 100 mA
		—	44	**120**		I_{OUT} = 500 mA
Output Voltage Accuracy	V_{OUT}	–1.5	—	+1.5	%	I_{OUT} = 100 µA, variation from nominal V_{OUT}
		–2.0	—	**+2.0**		
V_{BIAS} Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{BIAS})$	–0.1	0.015	0.1	%/V	$V_{BIAS} = V_{OUT} + 2.1V$ to 5.5V
V_{IN} Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	–0.05	0.005	0.05	%/V	$V_{IN} = V_{OUT} + 0.5V$ to 3.6V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	0.5	%	I_{OUT} = 10 mA to 500 mA
Current-Limit						
Short-Circuit Current Limit	I_{SC}	0.6	1.6	3	A	$V_{IN} = 2.7V; V_{OUT} = 0V$
Enable Input						
EN Logic Level High	V_{EN_HIGH}	**1.0**	0.77	—	V	—
EN Logic Level Low	V_{EN_LOW}	—	0.67	**0.2**	V	—
EN Hysteresis (Note 2)	V_{EN_HYST}	—	100	—	mV	—
Enable Bias Current	I_{EN_SHDN}	—	1	**2**	µA	$V_{EN} \le 0.2V$ (Regulator Shutdown)
	I_{EN}	—	6	**10**		V_{EN} = 1.0V (Regulator Enabled)
Turn-On Time	t_{ON}	—	15	**500**	µs	C_{OUT} = 1 µF; 90% of typical V_{OUT}
Thermal Protection						
Overtemperature Shutdown (Note 3)	T_{SD}	—	160	—	°C	T_J Rising
Overtemperature Shutdown Hysteresis (Note 3)	ΔT_{SD}	—	20	—	°C	—
Power Good						
Power Good Threshold Voltage	$V_{PWRGD_TH_R}$	—	91	95	%	V_{OUT} Rising
	$V_{PWRGD_TH_F}$	85	89	—		V_{OUT} Falling
Power Good Hysteresis (Note 2)	$PWRGD_{HYST}$	—	2	—	%	—
Power Good Output Low Voltage	V_{PWRGD_L}	—	0.02	0.1	V	I_{PG} = 250 µA
Power Good Leakage Current	I_{PWRGD_L}	–1	0.01	+1	µA	V_{PG} = 5.0V

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 0.5V$; $V_{BIAS} = V_{OUT} + 2.1V$; $C_{OUT} = 1\ \mu F$; $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **Bold** values indicate $–40°C \le T_J \le +125°C$; unless otherwise noted. Specification for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Reference Voltage (Adjustable Option Only)						
Feedback Reference Voltage	V_{FB}	0.394	0.4	0.406	V	I_{OUT} = 100 µA
		0.392		**0.408**	V	
FB Bias Current (Note 2)	I_{FB}	—	20	—	nA	V_{FB} = 0.8V
Output Voltage Noise and Ripple Rejection						
Output Voltage Noise (Note 3)	e_N	—	122.71	—	μV_{RMS}	f = 10 Hz to 100 kHz; I_{OUT} = 100 mA; C_{OUT} = 1 µF
Ripple Rejection (Note 3)	PSRR	—	50	—	dB	f = 10 kHz; C_{OUT} = 1.0 µF, I_{OUT} = 100 mA
		—	37	—		f = 100 kHz; C_{OUT} = 1.0 µF, I_{OUT} = 100 mA

1: Both V_{IN} and V_{BIAS} UVLO thresholds must be met for the output voltage to turn on. If either of the two input voltages is below the UVLO thresholds, the output is disabled.

2: These parameters are characterized but not production tested.

3: Design guidance only, not production tested.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Lead Temperature	—	—	—	260	°C	Soldering, 10 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance DFN-6	θ_{JA}	—	90	—	°C/W	—
	θ_{JC}	—	45	—		—
Thermal Resistance TDFN-6	θ_{JA}	—	90	—	°C/W	—
	θ_{JC}	—	45	—		—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

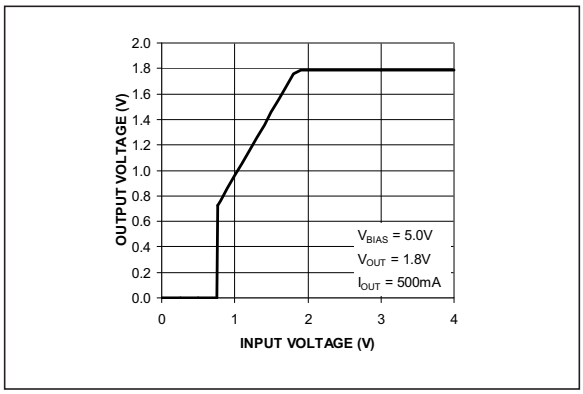


FIGURE 2-1: *Output Voltage vs. Input Voltage.*

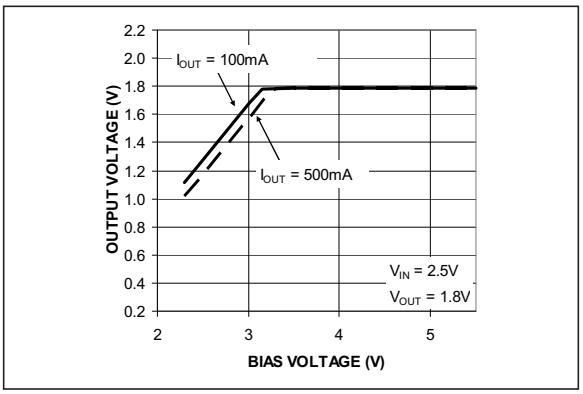


FIGURE 2-4: *Output Voltage vs. Bias Voltage.*

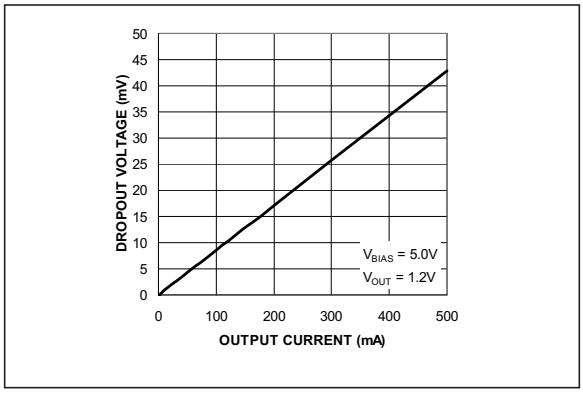


FIGURE 2-2: *Input Dropout Voltage vs. Output Current.*

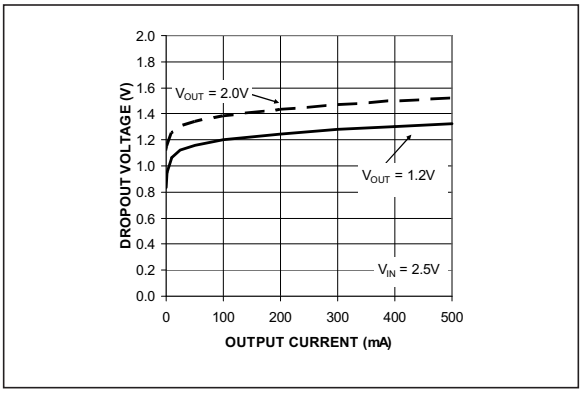


FIGURE 2-5: *Bias Dropout Voltage vs. Output Current.*

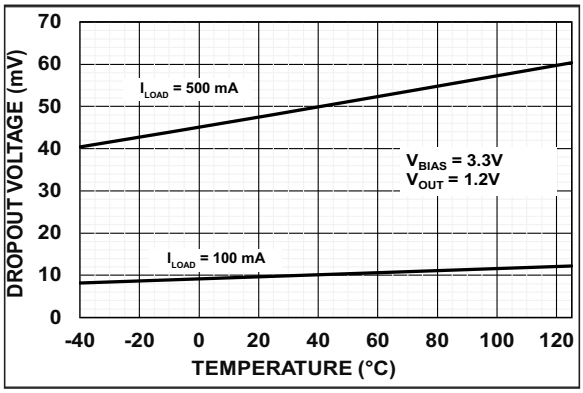


FIGURE 2-3: *Input Dropout Voltage vs. Temperature.*

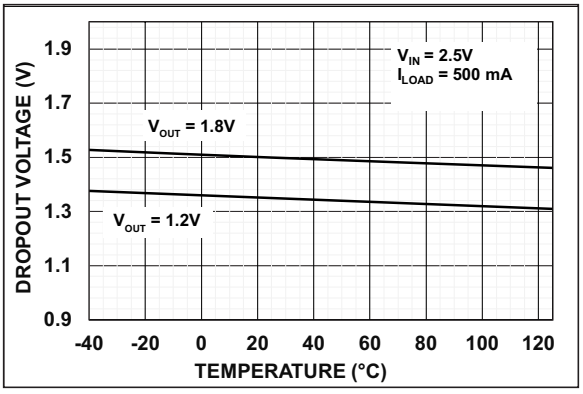


FIGURE 2-6: *Bias Dropout Voltage vs. Temperature.*

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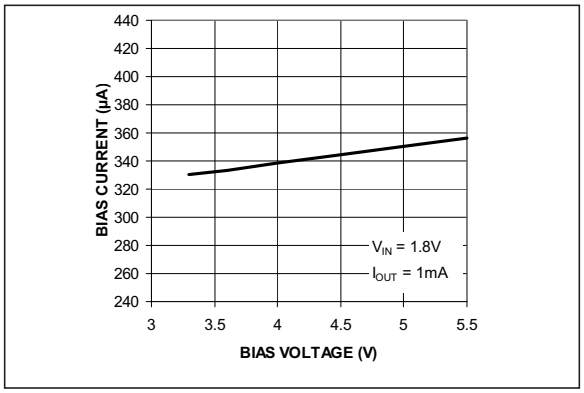


FIGURE 2-7: *Bias Current vs. Bias Voltage.*

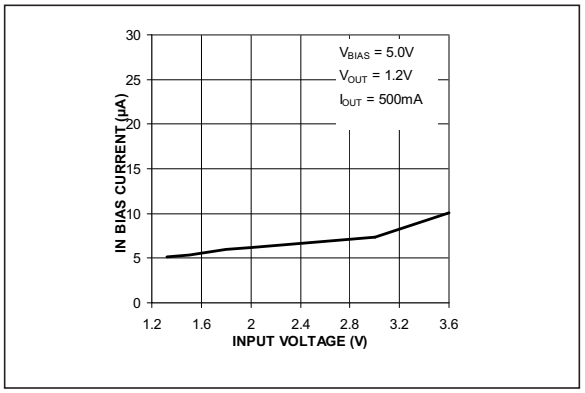


FIGURE 2-10: *Input Bias Current vs. Input Voltage.*

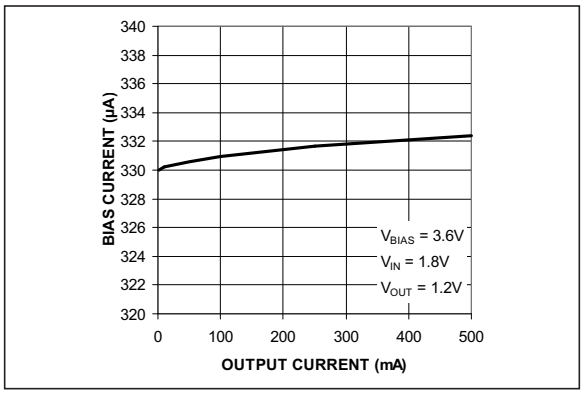


FIGURE 2-8: *Bias Current vs. Output Current.*

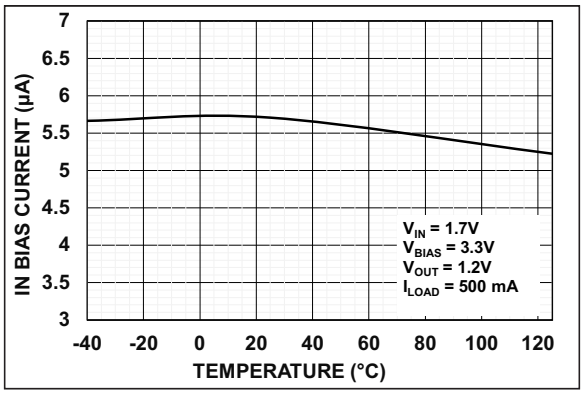


FIGURE 2-11: *Input Bias Current vs. Temperature.*

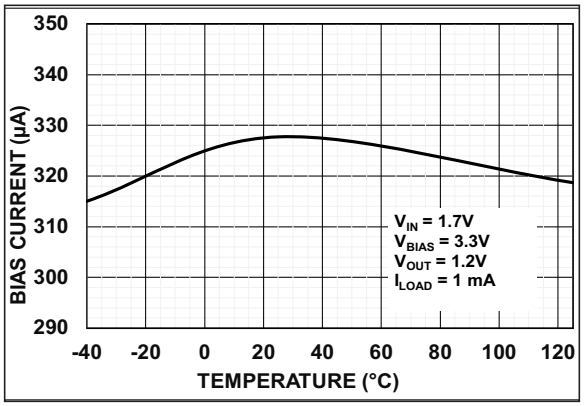


FIGURE 2-9: *Bias Current vs. Temperature.*

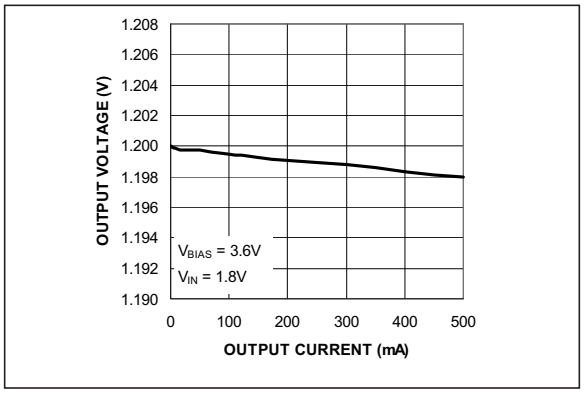


FIGURE 2-12: *Output Voltage vs. Output Current.*

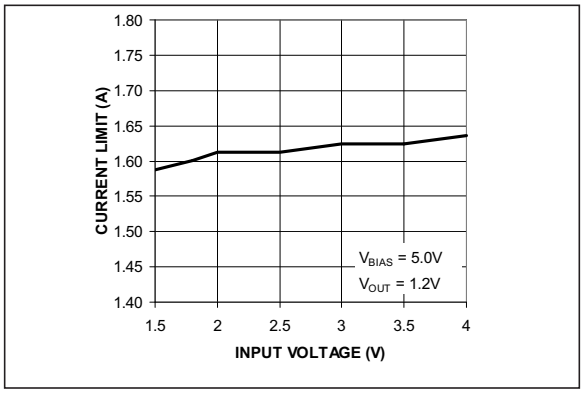


FIGURE 2-13: *Current-Limit vs. Input Voltage.*

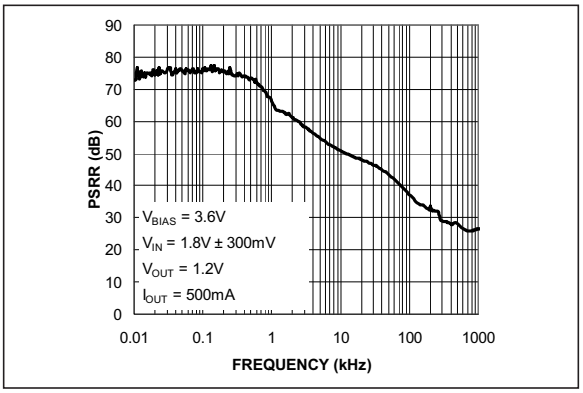


FIGURE 2-16: *Power Supply Ripple Rejection (Input Voltage).*

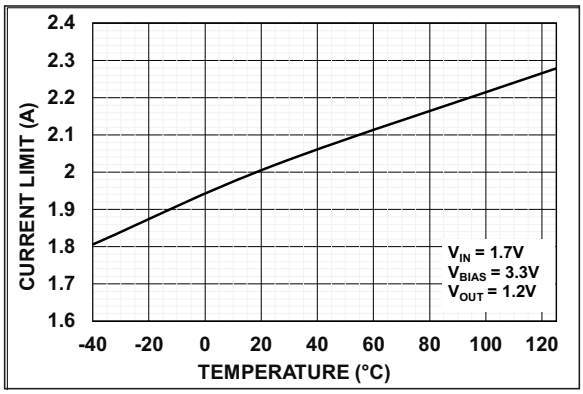


FIGURE 2-14: *Current-Limit vs. Input Temperature.*

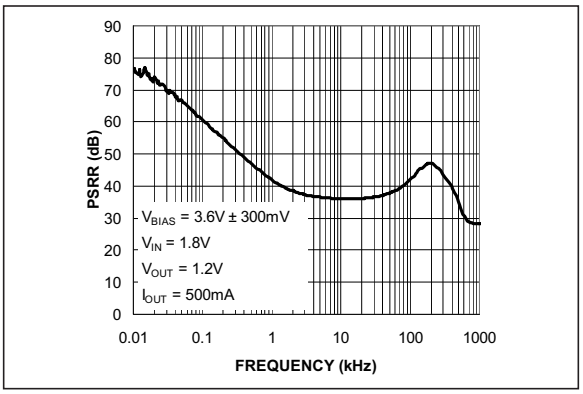


FIGURE 2-17: *Power Supply Ripple Rejection (Bias Voltage).*

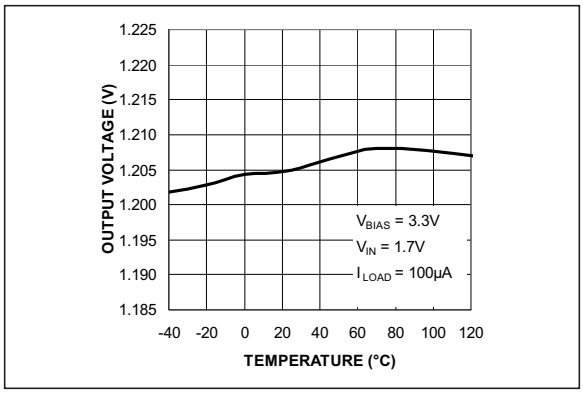


FIGURE 2-15: *Output Voltage vs. Temperature.*

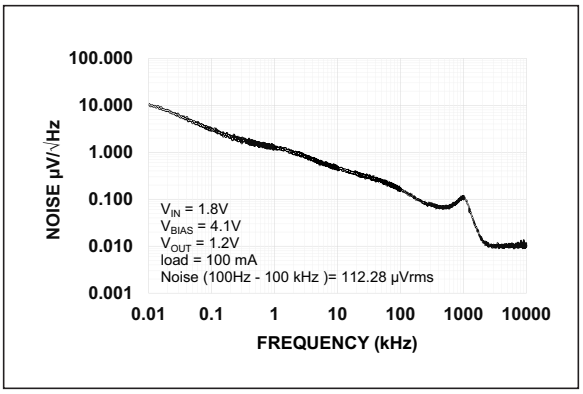


FIGURE 2-18: *Output Noise.*

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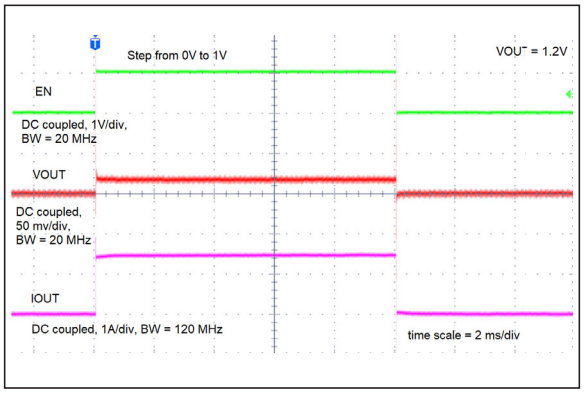


FIGURE 2-19: *Enabled into Short-Circuit.*

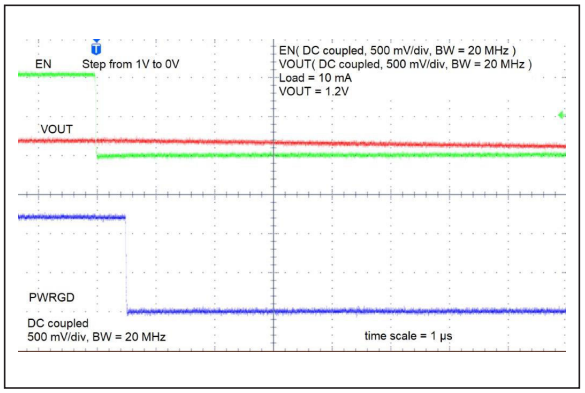


FIGURE 2-22: *Enable Turn-Off Time.*

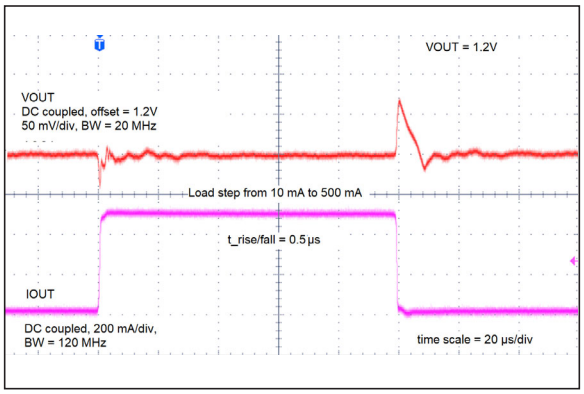


FIGURE 2-20: *Load Transient Response.*

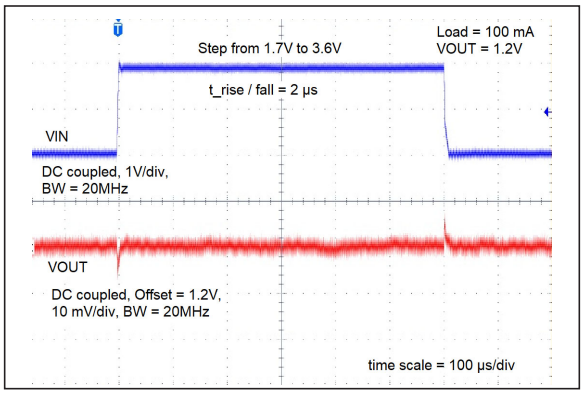


FIGURE 2-23: *Input Line Transient.*

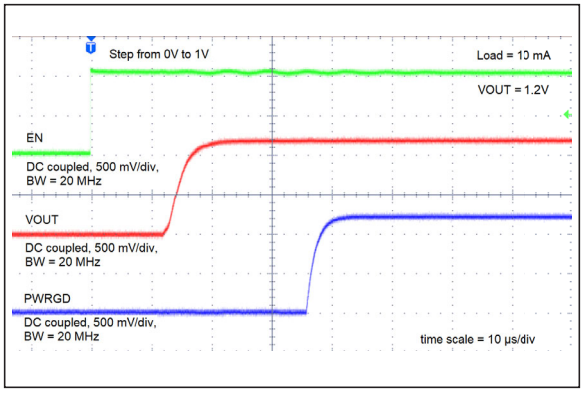


FIGURE 2-21: *Enable Turn-On Time.*

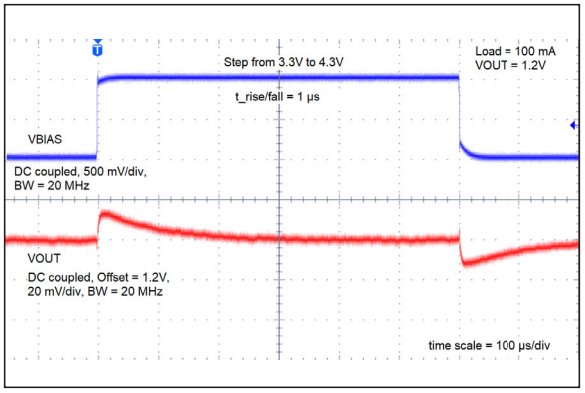


FIGURE 2-24: *Bias Line Transient.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (Fixed)	Pin Number (Adjustable)	Pin Name	Description
1	1	BIAS	Bias Supply. The bias supply is the power supply for the internal circuitry of the regulator.
2	2	GND	Ground. Ground pins and exposed pad must be connected externally.
3	3	IN	Input Supply. Drain of NMOS pass transistor, which is the power input voltage for regulator. The NMOS pass transistor steps down this input voltage to create the output voltage.
4	4	OUT	Output. Output voltage of regulator.
5	—	PGOOD	Power Good Output. Open-drain output. Output is driven low when the output voltage is less than the power good threshold of its programmed nominal output voltage. When the output goes above the power good threshold, the open-drain output goes high impedance, allowing it to be pulled up to a fixed voltage.
—	5	ADJ	Adjust Input. Connect external resistor divider to program the output voltage.
6	6	EN	Enable: TTL/CMOS compatible input. Logic-high = enable, Logic-low = shutdown. Do not leave floating.
ePAD	ePAD	GND	Exposed thermal pad. Connect to the ground plane to maximize thermal performance.

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4.0 FUNCTIONAL DESCRIPTION

The MIC47050 is a high speed, ultra-low dropout, dual supply NMOS ULDO designed to take advantage of point-of-load applications that use multiple supply rails to generate a low voltage, high-current power supply. The MIC47050 can source 0.5A of output current while only requiring a 1 µF ceramic output capacitor for stability. The MIC47050 regulator is fully protected from damage due to fault conditions, offering linear current limiting and thermal shutdown.

4.1 Bias Supply Voltage

V_{BIAS}, requiring relatively light current, provides power to the control portion of the MIC47050. Bypassing on the bias pin is recommended to improve performance of the regulator during line and load transients. Small 0.1 µF ceramic capacitors from V_{BIAS} to ground help reduce high frequency noise from being injected into the control circuitry from the bias rail and are good design practice.

4.2 Input Supply Voltage

V_{IN} provides the supply to power the LDO. The minimum input voltage is 1.0V. This allows conversion from low voltage supplies to reduce the power dissipation in the pass element.

4.3 Input Capacitor

The MIC47050 is a high-performance, high bandwidth device. Therefore, it requires a well bypassed input supply for optimal performance. A 1 µF capacitor is the minimum required for stability. A 10 µF ceramic capacitor is recommended for most applications, especially if the LDO's headroom (V_{IN}–V_{OUT}) is small and/or if large load transients are present. Fast load transient and low headroom requires a larger input filter capacitor to ensure that the regulator does not drop out of regulation. A 10 µF will better attenuate any voltage glitches from exceeding the maximum voltage rating of the part.

Additional high frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high frequency noise and are good practice in any RF based circuit.

X7R and X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors are not recommended since they change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic or a tantalum capacitor to ensure the same capacitance value over the operating temperature range.

Tantalum capacitors have a very stable dielectric (10% over their operating temperature range) and can also be used with this device. See **Section 2.0 "Typical Performance Curves"** for examples of load transient response.

4.4 Output Capacitor

The MIC47050 requires an output capacitor of 1 µF or greater to maintain stability. The design is optimized for use with low ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

The output capacitor type and placement criteria are the same as the input capacitor. See the **Section 4.3 "Input Capacitor"** for a detailed description.

4.5 Minimum Load Current

The MIC47050, unlike most other regulators, does not require a minimum load to maintain output voltage regulation.

4.6 Adjustable Regulator Design

The MIC47050 adjustable version allows programming the output voltage from 0.4V to 2.0V. Two external resistors are required. The R1 resistor value between V_{OUT} and the ADJ pin should not exceed 10 kΩ, as larger values can cause instability. R2 connects between the ADJ pin and ground. The resistor values are calculated as follows:

EQUATION 4-1:

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Where:

V_{OUT} = The desired output voltage
V_{REF} = The internal reference voltage
V_{REF} = 0.4V

4.7 Enable/Shutdown

The MIC47050 comes with a single active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a "zero" off mode current state. In this state, current

consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The active-high enable pin uses CMOS technology and the enable pin cannot be left floating. A floating enable pin may cause an indeterminate state on the output.

4.8 Power Good (PGOOD)

The Power Good (PGOOD) pin is an open-drain output that goes low when the output voltage (fixed version) drops below the PGOOD threshold voltage.

The pull-up resistor value should be large enough to guarantee a proper low voltage when the PGOOD pin pulls low. The PGOOD low voltage is typically 0.1V at 250 µA current. A 10 kΩ resistor or greater is recommended when pulling up to 3.3V bias.

If the PGOOD function is not required, the PGOOD pin may be left unconnected.

4.9 Thermal Shutdown

The MIC47050 has an internal overtemperature protection feature. This feature is for protection only. The device should never be intentionally operated near this temperature as this may reduce long term reliability. The device will turn off when the overtemperature threshold is exceeded. A 20°C hysteresis is built in to allow the device to cool before turning back on.

4.10 Thermal Considerations

The MIC47050 is designed to provide 0.5A of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. Given that the input voltage is 1.8V, the output voltage is 1.2V and the output current is 0.5A. The actual power dissipation of the regulator circuit can be determined using Equation 4-2:

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS}$$

Because this device is CMOS, the ground current is insignificant for power dissipation and can be ignored for this calculation.

EQUATION 4-3:

$$P_D = (1.8V - 1.2V) \times 0.5A = 0.3W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-4:

$$P_{D(MAX)} = \left[\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right]$$

Where:

$T_{J(MAX)}$ = 125°C, the maximum junction temperature of the die

θ_{JA} = 90°C/W, the thermal resistance

Table 4-1 shows junction-to-ambient thermal resistance for the MIC47050 in the DFN or TDFN packages.

TABLE 4-1: THERMAL RESISTANCE

Package	θ_{JA} Recommended Min. Footprint	θ_{JC}
6-Pin 2 mm x 2 mm DFN	90°C/W	45°C/W
6-Pin 2 mm x 2 mm TDFN	90°C/W	45°C/W

Substituting P_D for $P_{D(max)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is 90°C/W. The maximum power dissipation must not be exceeded for proper operation. For example, when operating the MIC47050-1.2YML at an input voltage of 1.8V and a 0.5A load with a minimum footprint layout, the maximum ambient operating temperature T_A can be determined as follows:

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EQUATION 4-5:

$$T_A = T_{J(MAX)} - \theta_{JA} \times P_{D(MAX)}$$

$$T_A = 125°C - 90°C/\mathrm{W} \times 0.3W$$

$$T_A = 98°C$$

Therefore, a 1.2V application with 0.5A of output current can accept an ambient operating temperature of 98°C in a 2 mm x 2 mm DFN or TDFN package.

4.11 Thermal Measurements

Measuring the IC's case temperature is recommended to insure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat sinking effect.

In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

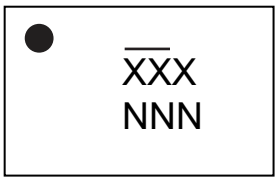
Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for the 2 mm x 2 mm DFN or TDFN package. An optional stand makes it easy to hold the beam on the IC for long periods of time.

For a full discussion of heat sinking and thermal effects of voltage regulators, refer to the "Regulator Thermals" section of Designing with Low-Dropout Voltage Regulators handbook.

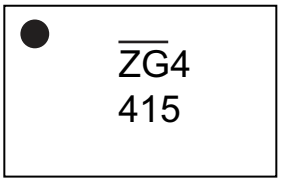
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

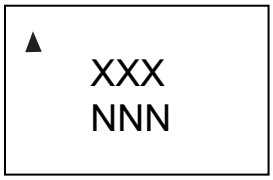
6-Lead DFN*



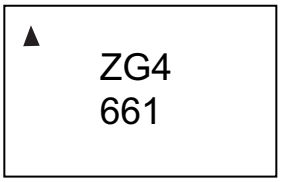
Example



6-Lead TDFN*



Example



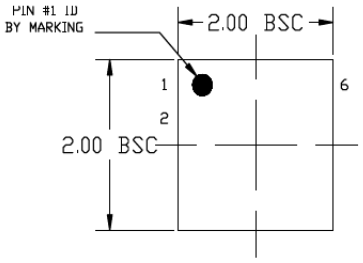
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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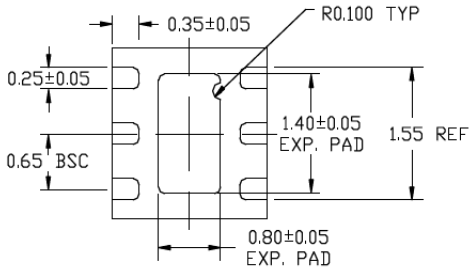
6-Lead 2 mm x 2 mm DFN Package Outline and Recommended Land Pattern

TITLE
6 LEAD DFN 2x2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

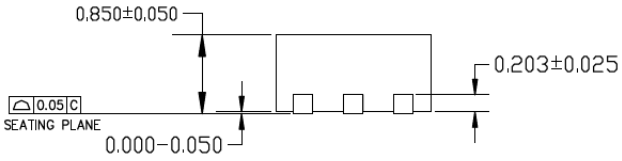
DRAWING #	DFN22-6LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



END VIEW
NOTE: 1, 2, 3

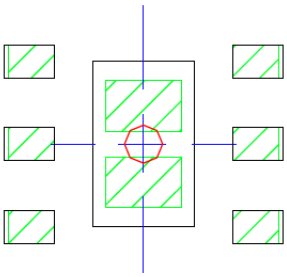
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.40 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

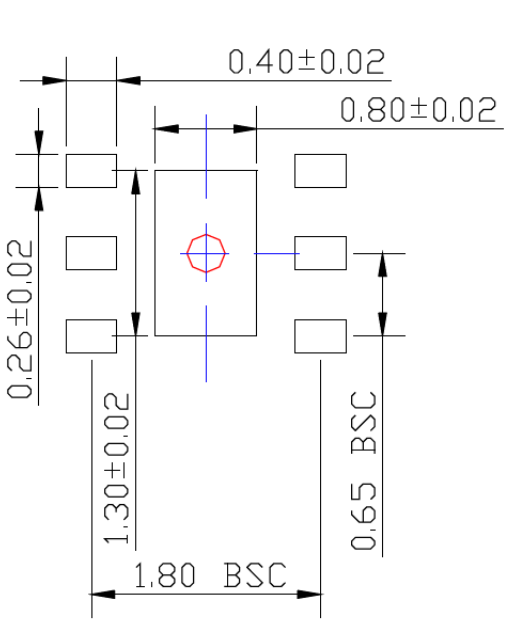
POD-Land Pattern drawing # DFN22-6LD-PL-1

RECOMMENDED LAND PATTERN

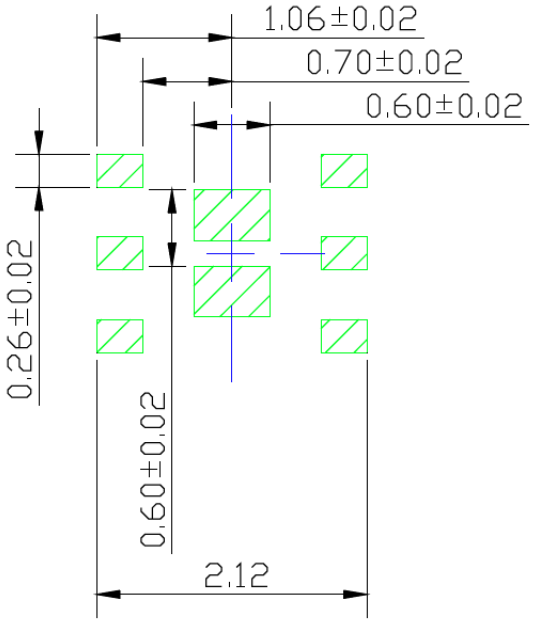
NOTE: 4,5



STACKED-UP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

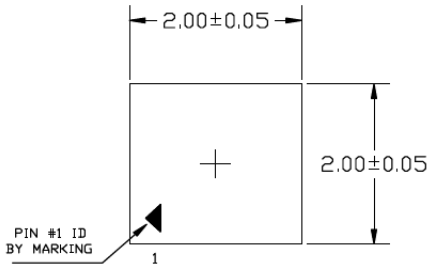
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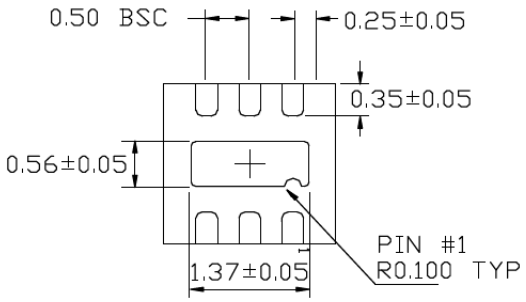
6-Lead 2 mm x 2 mm TDFN Package Outline and Recommended Land Pattern

TITLE
6 LEAD TDFN 2X2mm (0.50mm LEAD PITCH) PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

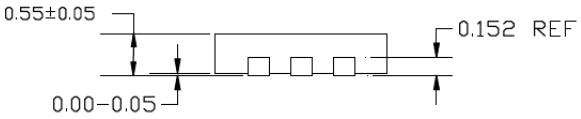
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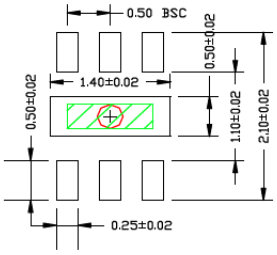
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLE (SHADED AREA) REPRESENTS OPTIONAL SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.00x0.30 MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (July 2018)

- Converted Micrel document MIC47050 to Microchip data sheet DS20006050C.
- Added Automotive feature AEC-Q100 Qualified and PPAP Capable in the **Section "Features"**
- Updated images for Figure 2-10, Figure 2-11, Figure 2-18, Figure 2-19 through Figure 2-24.

Revision B (September 2018)

- Updated images for Figure 2-3, Figure 2-6, Figure 2-9, Figure 2-11, Figure 2-14 and Figure 2-15.

Revision C (February 2019)

- Added Note 2 and Note 3 to the Electrical table.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X	X	XX	–XX
Device	Output Voltage	Junction Temperature Range	Package	Media Type

Device:	MIC47050: 500 mA ULDO with Low Input and Low Output Voltage
Output Voltage:	1.2 = 1.2V Fixed 1.8 = 1.8V Fixed <blank> = Adjustable
Junction Temperature Range:	Y = –40°C to +125°C, RoHS Compliant
Package:	ML = 6-Lead 2 mm x 2 mm x 0.9 mm DFN MT = 6-Lead 2 mm x 2 mm x 0.5 mm TDFN
Media Type:	TR = 5000/Reel

Examples:

a) MIC47050YML-TR:	500 mA ULDO with Low Input and Low Output Voltage, Adjustable Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.9 mm DFN Package, 5000/ Reel
b) MIC47050-1.2YML-TR:	500 mA ULDO with Low Input and Low Output Voltage, 1.2V Fixed Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.9 mm DFN Package, 5000/ Reel
c) MIC47050-1.8YML-TR:	500 mA ULDO with Low Input and Low Output Voltage, 1.8V Fixed Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.9 mm DFN Package, 5000/ Reel
e) MIC47050YMT-TR:	500 mA ULDO with Low Input and Low Output Voltage, Adjustable Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.5 mm TDFN Package, 5000/ Reel
f) MIC47050-1.2YMT-TR:	500 mA ULDO with Low Input and Low Output Voltage, 1.2V Fixed Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.5 mm TDFN Package, 5000/ Reel
g) MIC47050-1.8YMT-TR:	500 mA ULDO with Low Input and Low Output Voltage, 1.8V Fixed Output Voltage, –40°C to +125°C Temperature Range, 6-Lead 2 mm x 2 mm x 0.5 mm TDFN Package, 5000/ Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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NOTES:

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