N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.0165 at V_{GS} = 10 V	60
	0.0190 at V_{GS} = 6 V	56

FEATURES

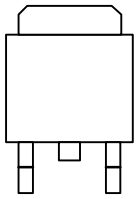
- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- PWM Optimized for Fast Switching
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT

APPLICATIONS

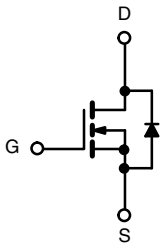
- Isolated DC/DC converters
  - Primary-Side Switch

TO-263



Top View

Ordering Information: SUM60N10-17-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	60[a]	A
	T_C = 125 °C		34[a]	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current		I_{AS}	40	
Single Pulse Avalanche Energy[b]	L = 0.1 mH	E_{AS}	80	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	150[c]	W
	T_A = 25 °C[d]		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Limit**	**Unit**
Junction-to-Ambient	PCB Mount (TO-263)[d]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)		R_{thJC}	1.0	

Notes:
a. Package limited.
b. Duty cycle ≤ 1 %.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).

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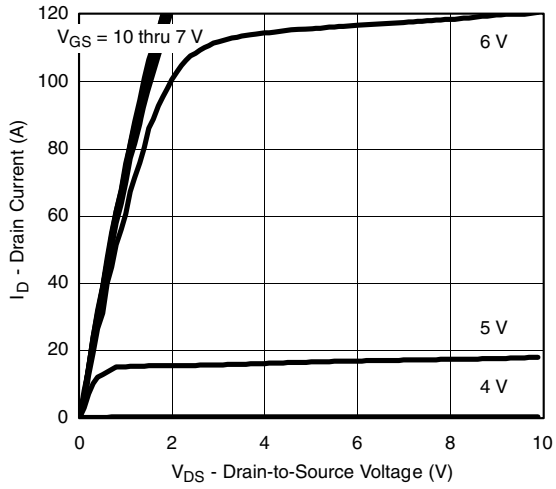
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{DS} = 0 V, I_D = 250 µA	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 175 °C			250	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	100			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.013	0.0165	Ω
		V_{GS} = 6 V, I_D = 20 A		0.015	0.019	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125 °C			0.031	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175 °C			0.041	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	25			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4300		pF
Output Capacitance	C_{oss}			450		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 60 A		65	100	nC
Gate-Source Charge[c]	Q_{gs}			25		
Gate-Drain Charge[c]	Q_{gd}			19		
Gate Resistance	R_g	f = 1 MHz	0.3	1.5	3	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.5 Ω I_D ≅ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15		ns
Rise Time[c]	t_r			12	20	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	45	
Fall Time[c]	t_f			10	15	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)[b]						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				100	
Forward Voltage[a]	V_{SD}	I_F = 30 A, V_{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, dI/dt = 100 A/µs		125	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	Q_{rr}			0.5	1.2	µC

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

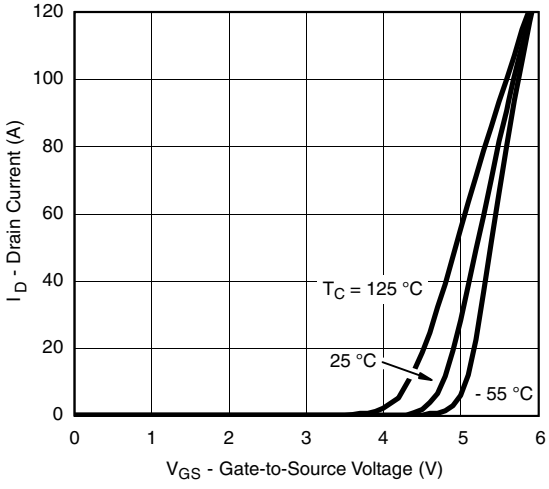
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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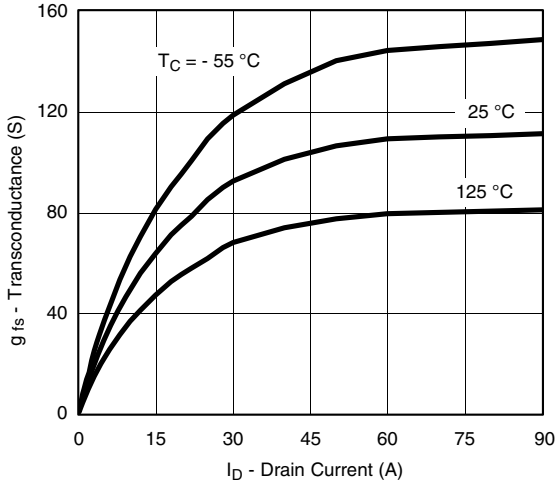
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



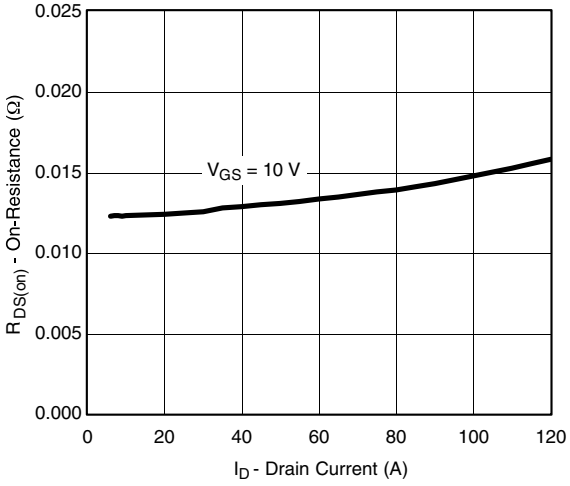
Output Characteristics



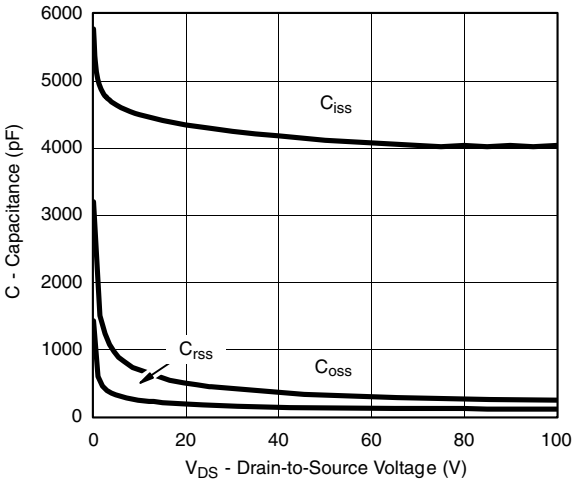
Transfer Characteristics



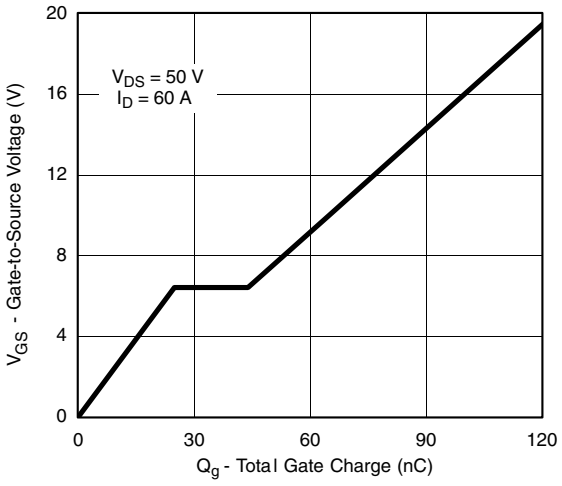
Transconductance



On-Resistance vs. Drain Current



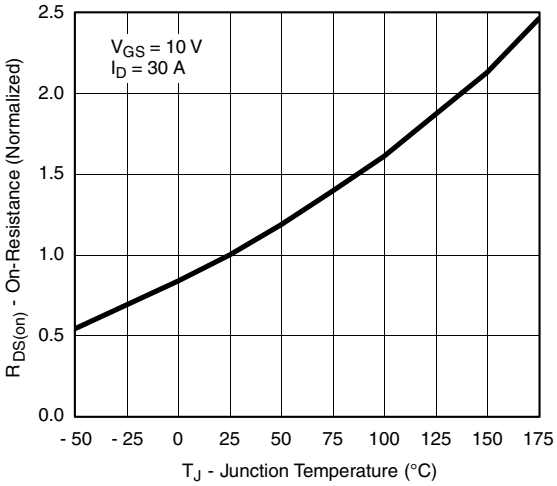
Capacitance



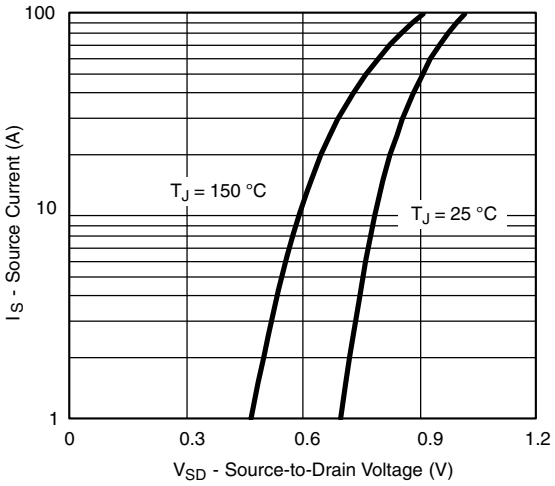
Gate Charge

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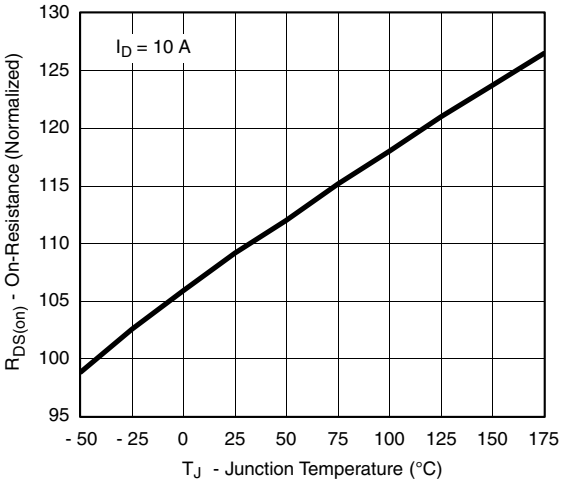
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature



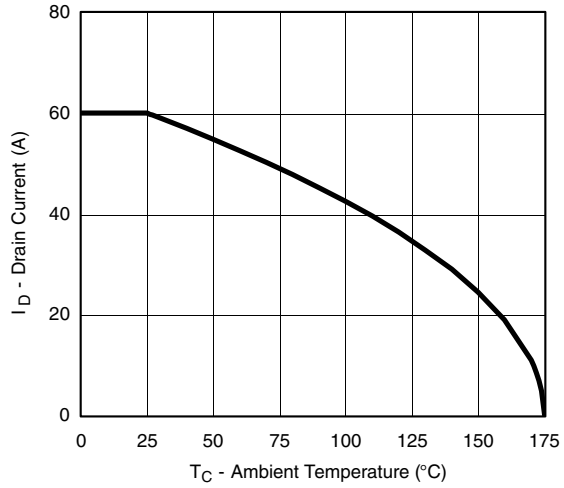
Source-Drain Diode Forward Voltage



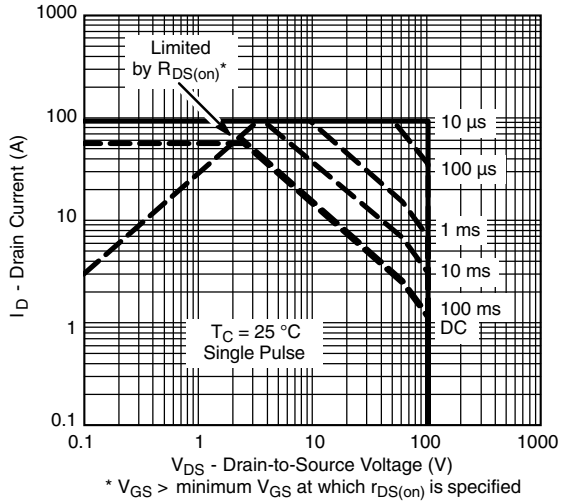
On-Resistance vs. Junction Temperature

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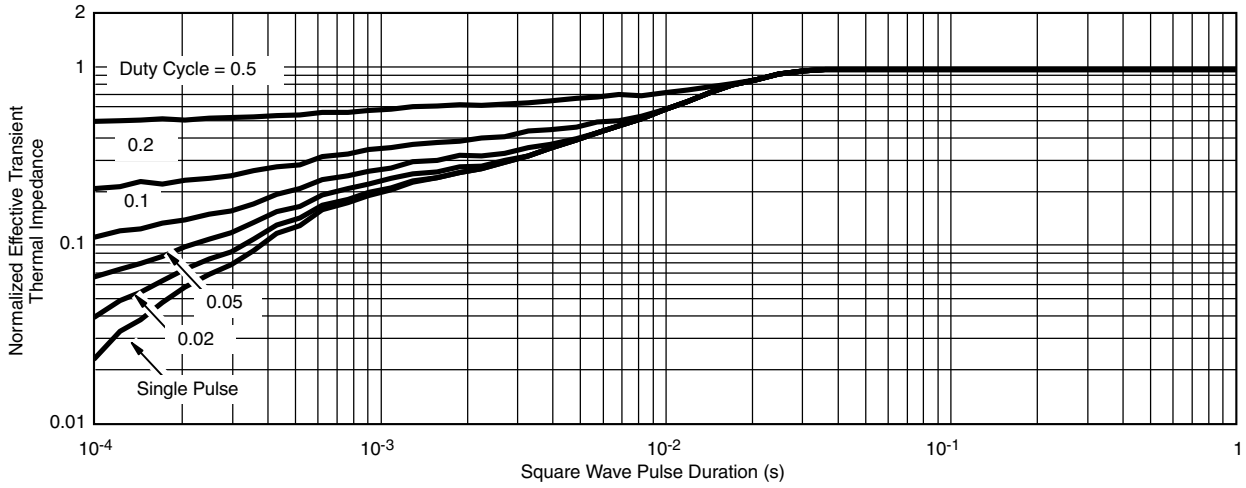
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



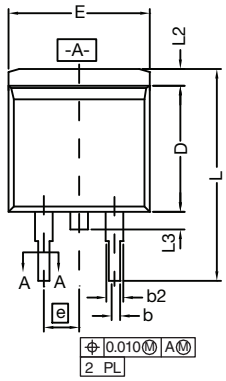
Normalized Thermal Transient Impedance, Junction-to-Case

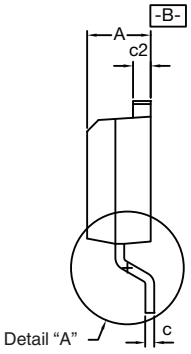
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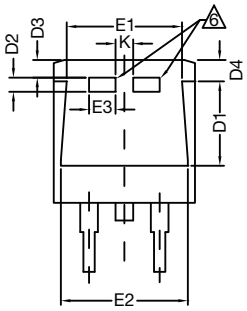
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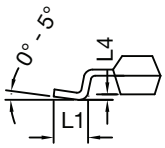
TO-263 (D²PAK): 3-LEAD

VERSION 1: FACILITY CODE = T

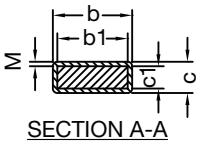








DETAIL A (ROTATED 90°)



SECTION A-A

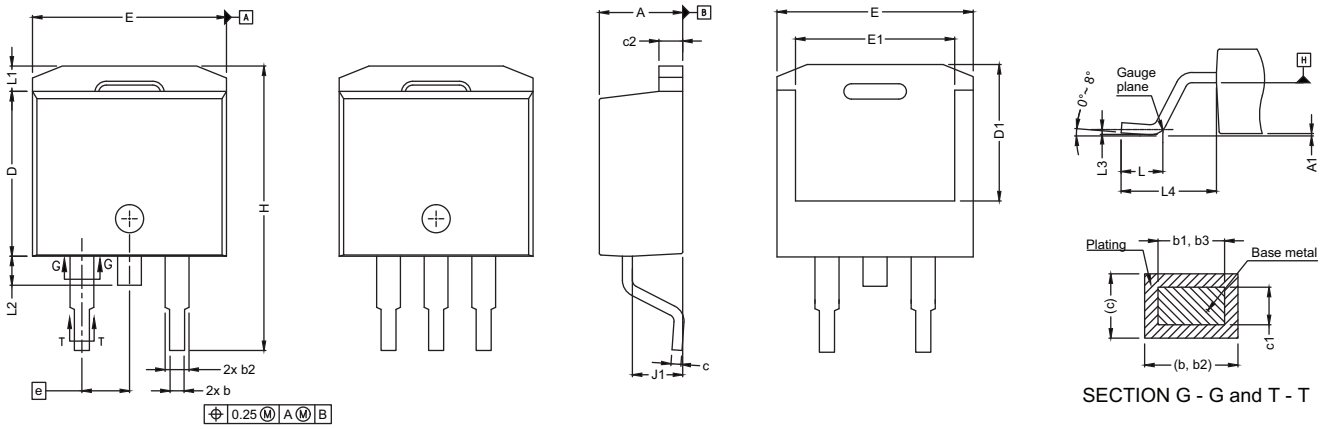
DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

Notes

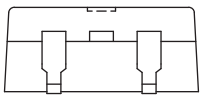
1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

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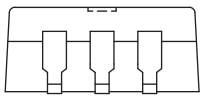
VERSION 2: FACILITY CODE = N



SECTION G - G and T - T



OPTION 1
2 leads

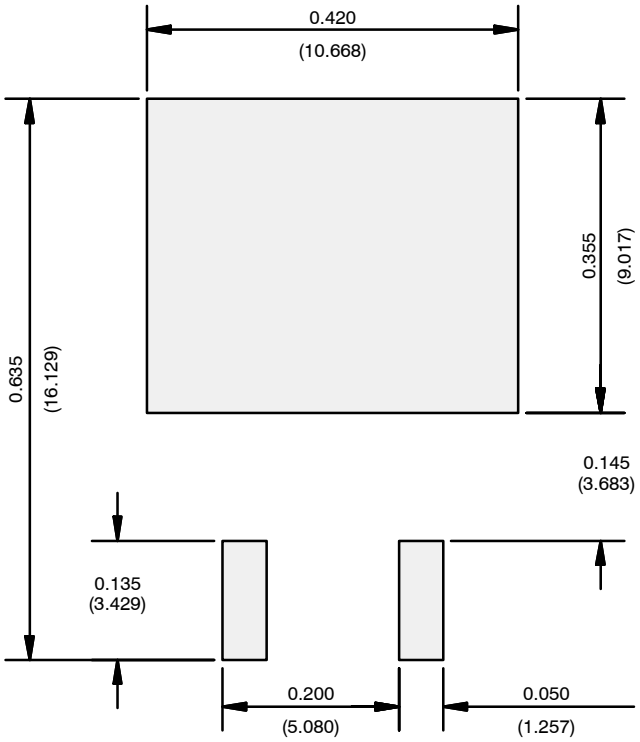


OPTION 2
3 leads

DIM.	MIN.	MAX.
A	4.36	4.56
A1	0	0.25
b	0.70	0.90
b1	0.51	0.89
b2	1.20	1.46
b3	1.17	1.37
c	0.38	0.694
c1	0.38	0.534
c2	1.19	1.34
D	8.60	9.00
D1	6.9	7.5
E	10.15	10.55
E1	8.1	8.7
e	2.54 BSC	
H	15.0	15.6
L	1.9	2.5
L1	-	1.65
L2	-	1.78
L3	0.25 typ.	
L4	4.78	5.28
J1	2.56	2.96
ECN: S24-1080-Rev. L, 28-Oct-2024 DWG: 5843		

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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