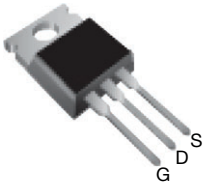
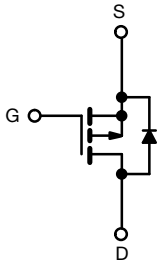
Power MOSFET

TO-220AB





P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	3.0
Q_g max. (nC)	11	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	4.0	
Configuration	Single	

DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF9610PbF
Lead (Pb)-free and halogen-free	IRF9610PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-200	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	-1.8	A
		T_C = 100 °C		-1.0	
Pulsed drain current [a]			I_{DM}	-7.0	
Linear derating factor				0.16	W/°C
Single pulse avalanche energy [b]			P_D	20	W
Repetitive avalanche current [a]			I_{LM}	-7.0	A
Repetitive avalanche energy [a]			dV/dt	-5.0	V/ns
Maximum power dissipation	T_C = 25 °C		T_J, T_{stg}	-55 to +150	°C
Peak diode recovery dV/dt [c]				300	
Operating junction and storage temperature range				10	lbf · in
Soldering recommendations (peak temperature) [d]	For 10 s			1.1	N · m

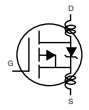
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
b. Not applicable
c. I_{SD} ≤ -1.8 A, dI/dt ≤ 70 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
d. 1.6 mm from case

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THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	6.4	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = -1 mA	-	-0.23	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -200 V, V_{GS} = 0 V	-	-	-100	µA
		V_{DS} = -160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = -10 V; I_D = -0.90 A [b]	-	-	3.0	Ω
Forward transconductance	g_{fs}	V_{DS} = -50 V, I_D = -0.90 A [b]	0.90	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 10	-	170	-	pF
Output capacitance	C_{oss}		-	50	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Total gate charge	Q_g	V_{GS} = -10 V; I_D = -3.5 A, V_{DS} = -160 V, see fig. 11 and 18 [b]	-	-	11	nC
Gate-source charge	Q_{gs}		-	-	7.0	
Gate-drain charge	Q_{gd}		-	-	4.0	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -100 V, I_D = -0.90 A, R_g = 50 Ω, R_D = 110 Ω, see fig. 17 [b]	-	8.0	-	ns
Rise time	t_r		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	10	-	
Fall time	t_f		-	8.0	-	
Gate input resistance	R_g	f = 1 MHz, open drain	2.5	-	14.3	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-1.8	A
Pulsed diode forward current [a]	I_{SM}		-	-	-7.0	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = -1.8 A, V_{GS} = 0 V [b]	-	-	-5.8	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = -1.8 A, dI/dt = 100 A/µs [b]	-	240	360	ns
Body diode reverse recovery charge	Q_{rr}		-	1.7	2.6	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

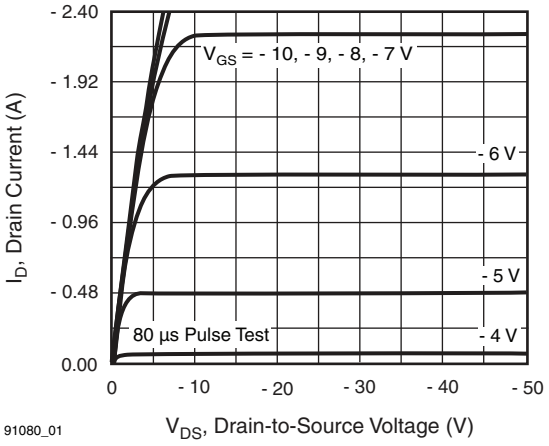


Fig. 1 - Typical Output Characteristics

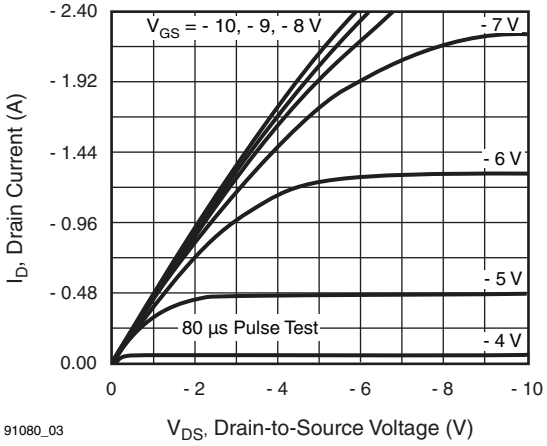


Fig. 3 - Typical Saturation Characteristics

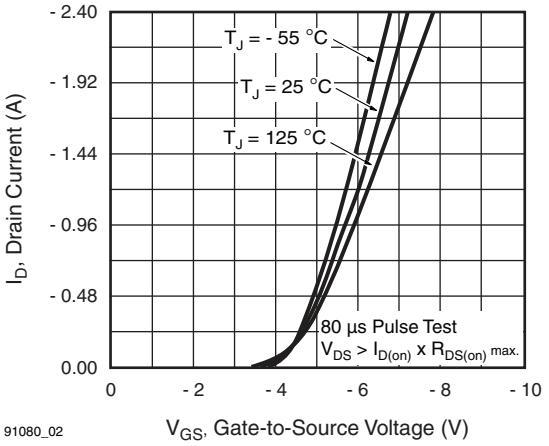


Fig. 2 - Typical Transfer Characteristics

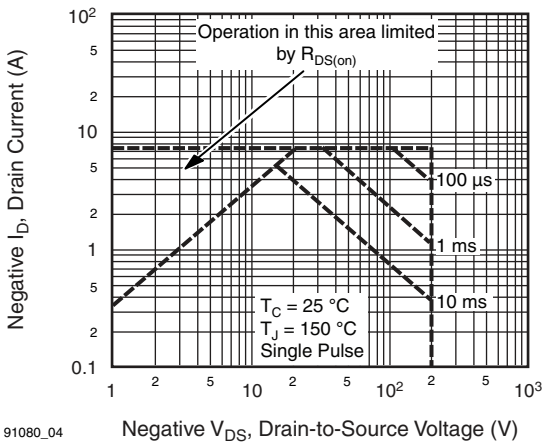


Fig. 4 - Maximum Safe Operating Area

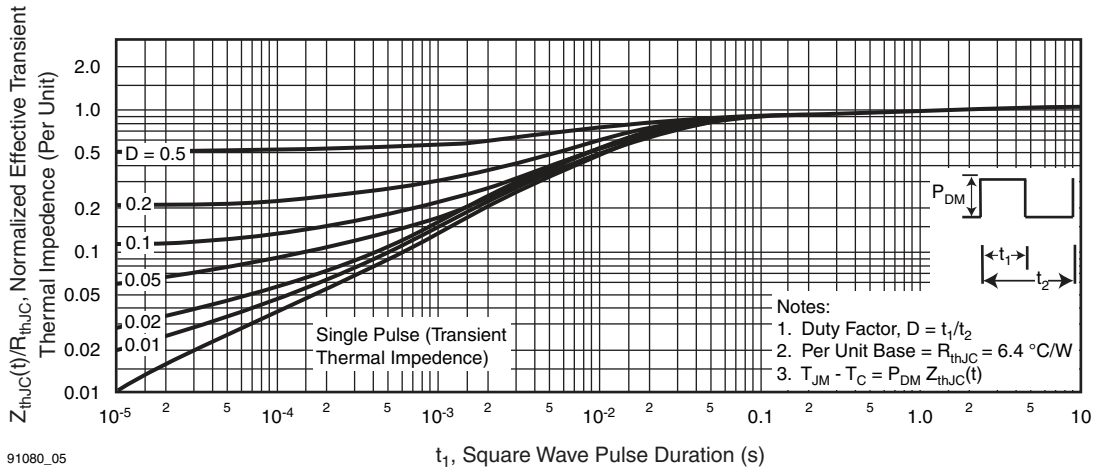


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

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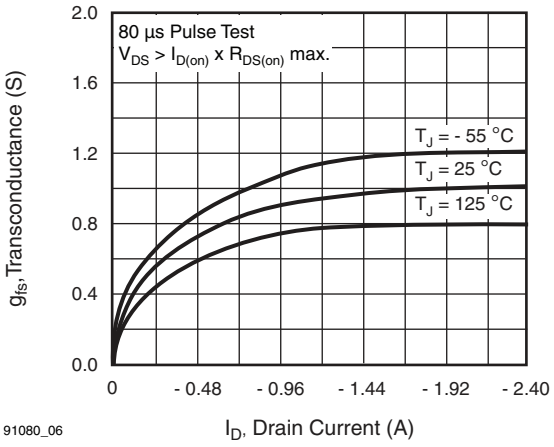


Fig. 6 - Typical Transconductance vs. Drain Current

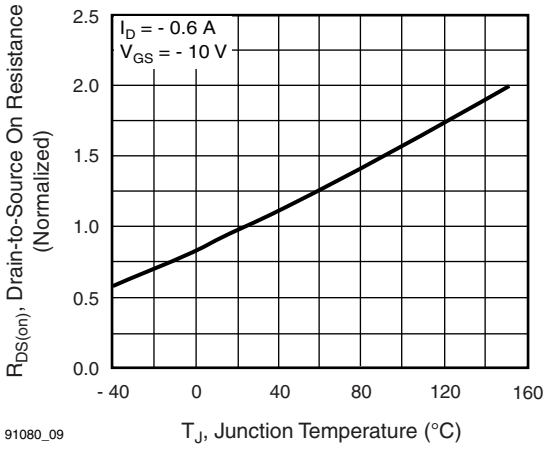


Fig. 9 - Normalized On-Resistance vs. Temperature

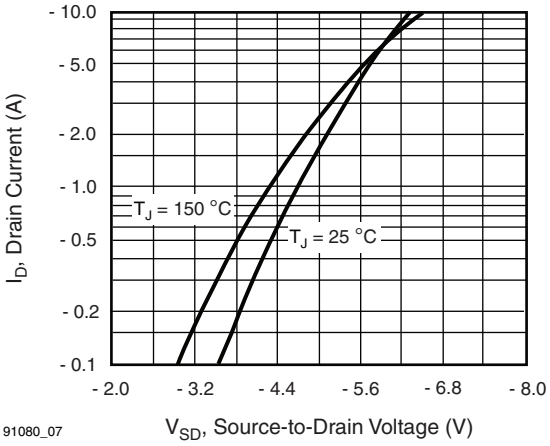


Fig. 7 - Typical Source-Drain Diode Forward Voltage

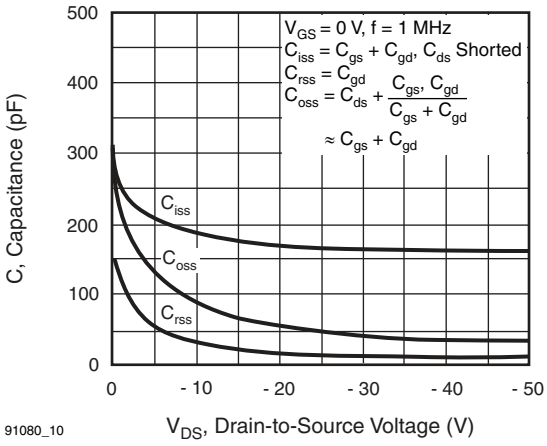


Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

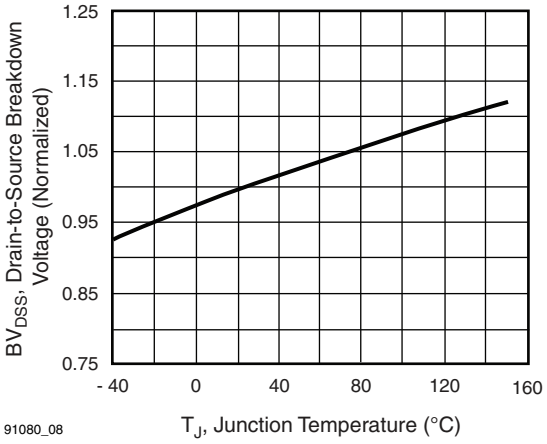


Fig. 8 - Breakdown Voltage vs. Temperature

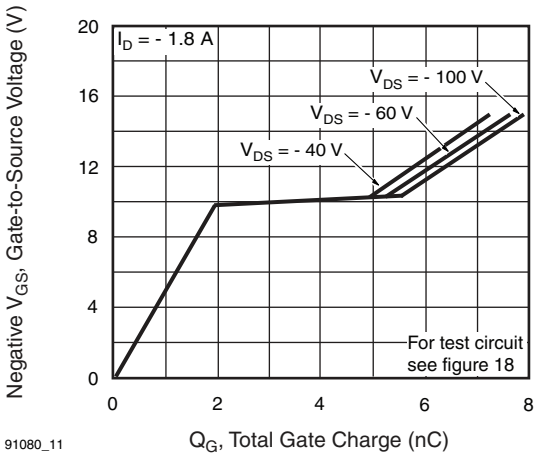


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

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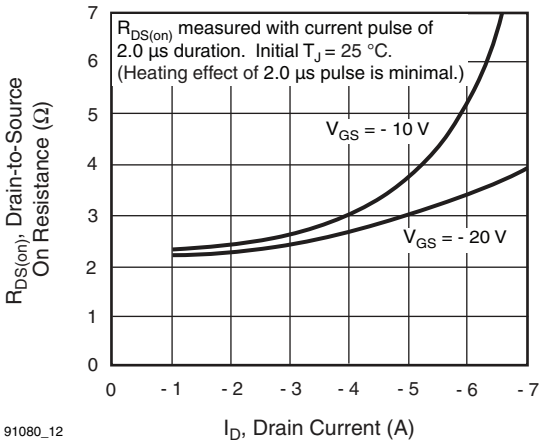


Fig. 12 - Typical On-Resistance vs. Drain Current

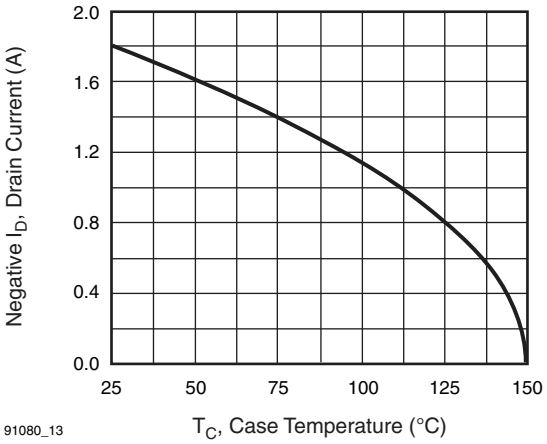


Fig. 13 - Maximum Drain Current vs. Case Temperature

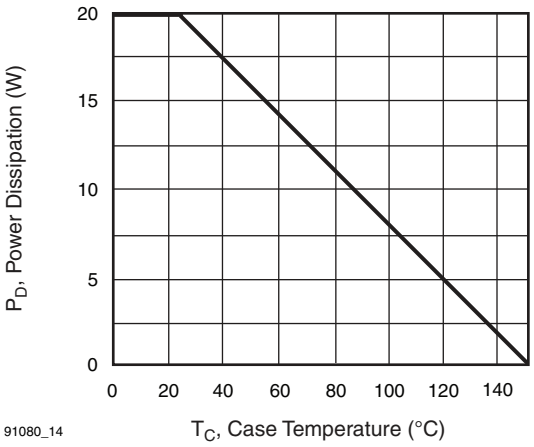


Fig. 14 - Power vs. Temperature Derating Curve

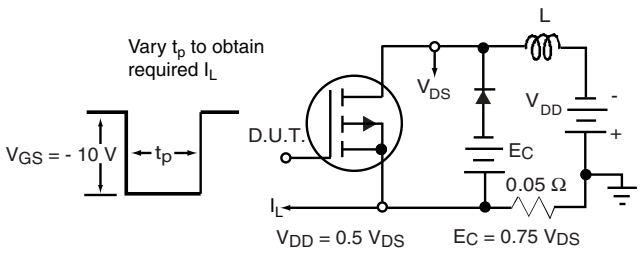


Fig. 15 - Clamped Inductive Test Circuit

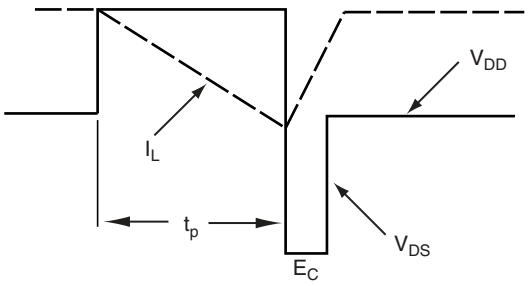


Fig. 16 - Clamped Inductive Waveforms

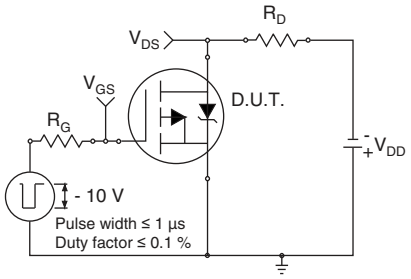


Fig. 17a - Switching Time Test Circuit

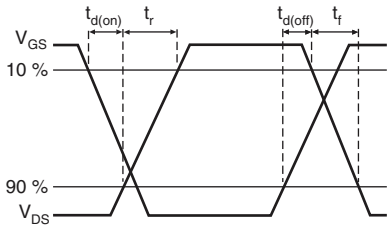


Fig. 17b - Switching Time Waveforms

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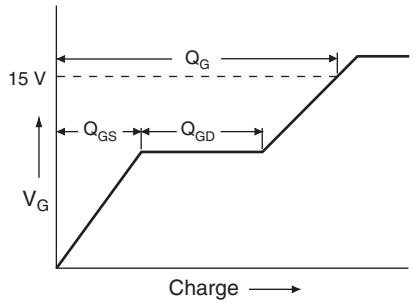


Fig. 18a - Basic Gate Charge Waveform

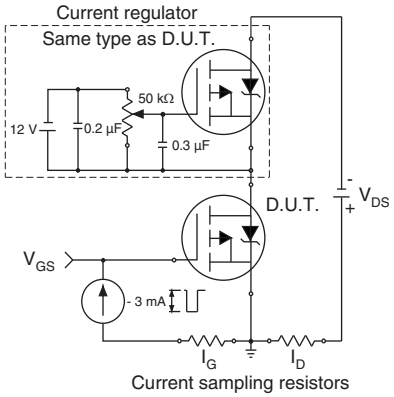
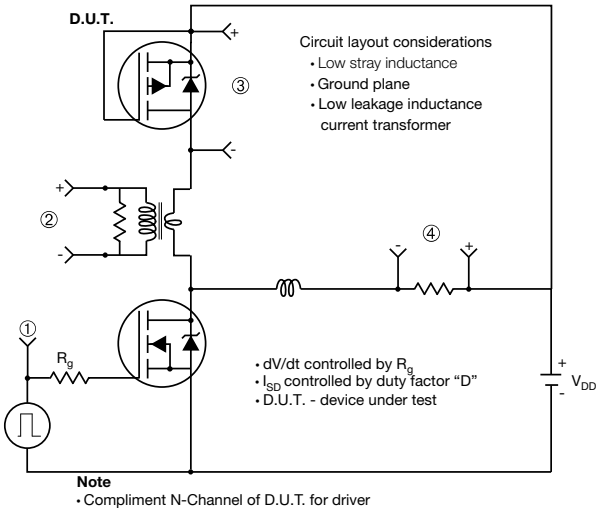


Fig. 18b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



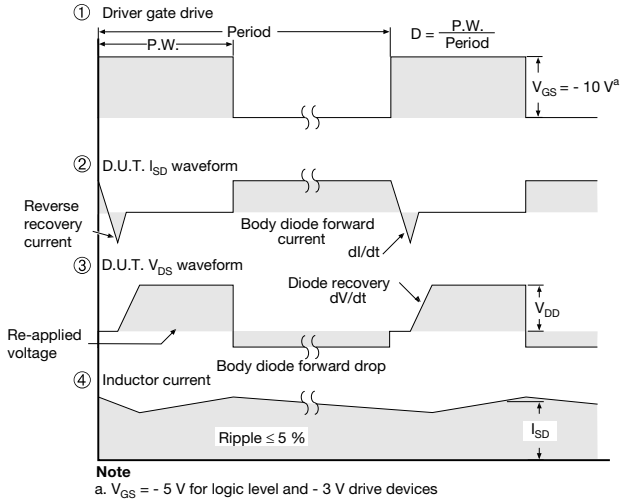


Fig. 19 - For P-Channel

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