Document Number: A2T09D400-23N
Rev. 0, 3/2016

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 93 W symmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 716 to 960 MHz.

800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, P_{out} = 93 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
776 MHz	17.8	45.9	7.0	–36.8
806 MHz	18.2	46.8	7.2	–37.8
836 MHz	17.9	48.0	7.1	–37.1

Features

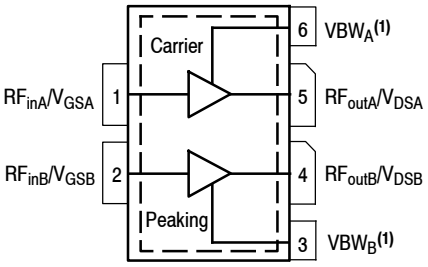
- Production Tested in a Symmetrical Doherty Configuration
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T09D400-23NR6

716–960 MHz, 93 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-1230-4L2S PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 93 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, 806 MHz	$R_{\theta JC}$	0.29	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1200 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.5	2.2	2.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.1	0.14	0.3	Vdc
On Characteristics - Side B (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.05	0.14	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests – 776 MHz (1,2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, P_{out} = 93 W Avg., f = 776 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.5	17.8	19.0	dB
Drain Efficiency	η_D	43.5	45.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.0	—	dB
Adjacent Channel Power Ratio	ACPR	—	–36.8	–34.7	dBc
Functional Tests – 836 MHz (1,2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, P_{out} = 93 W Avg., f = 836 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.5	17.9	19.0	dB
Drain Efficiency	η_D	43.5	48.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	–37.1	–34.7	dBc
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, f = 806 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 497 W Pulsed CW Output Power (3 dB Input Overdrive from 400 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1200 mA, V_{GSB} = 1.12 Vdc, 776–836 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	400	—	W
P_{out} @ 3 dB Compression Point (3)	P3dB	—	540	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 776–836 MHz bandwidth)	Φ	—	–7.1	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	35	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 93 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.01	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T09D400-23NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L2S

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

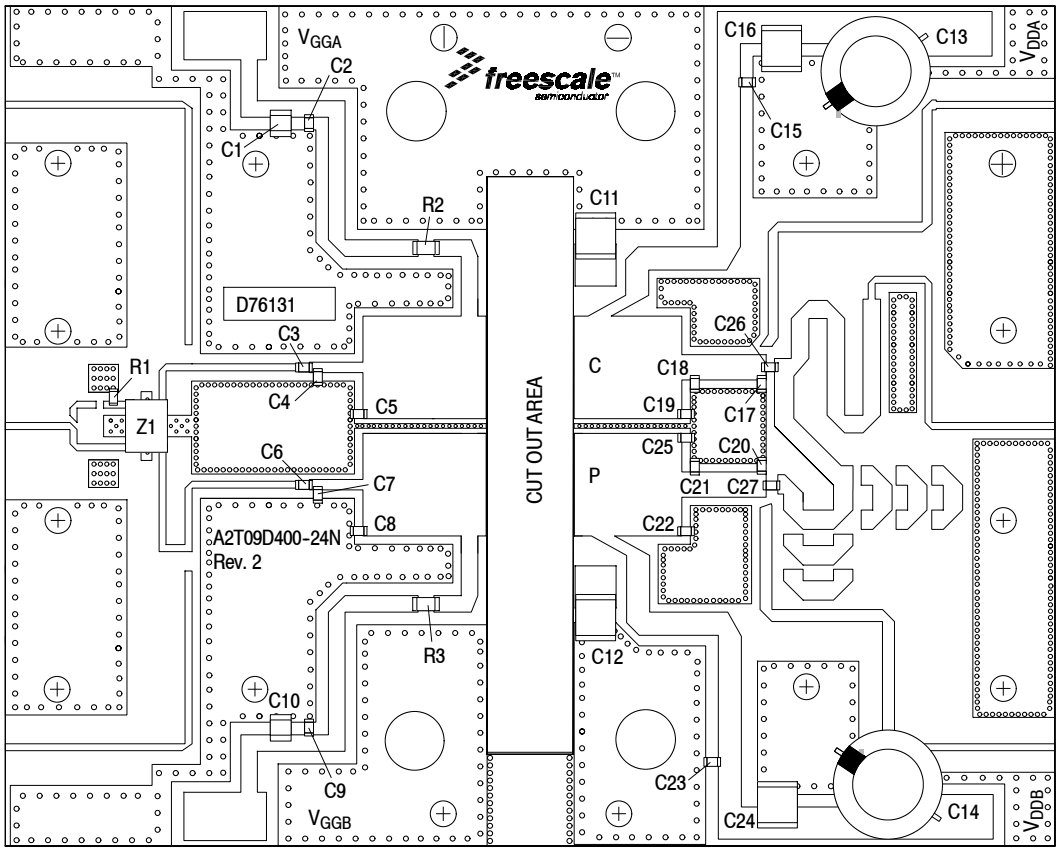


Figure 2. A2T09D400–23NR6 Test Circuit Component Layout

Table 7. A2T09D400–23NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C10	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C2, C3, C6, C9, C15, C23	68 pF Chip Capacitors	ATC600F680R0BT250XT	ATC
C4, C7, C21	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C5, C8	6.2 pF Chip Capacitors	ATC600F6R2BT250XT	ATC
C11, C12, C16, C24	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C13, C14	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C17	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C18	8.2 pF Chip Capacitor	ATC600F8R2BT250XT	ATC
C19	12 pF Chip Capacitor	ATC600F120BT250XT	ATC
C20	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C22	15 pF Chip Capacitor	ATC600F150BT250XT	ATC
C25	2.4 pF Chip Capacitor	ATC600F2R4BT250XT	ATC
C26, C27	27 pF Chip Capacitors	ATC600F270BT250XT	ATC
R1	50 Ω, 10 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	12 Ω, 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
Z1	600–900 MHz Band, 90°, 3 dB Chip Hybrid Coupler	X3C07P1-03S	Anaren
PCB	Rogers RO3006, 0.025″, ε_r = 6.5	D76131	MTL

TYPICAL CHARACTERISTICS

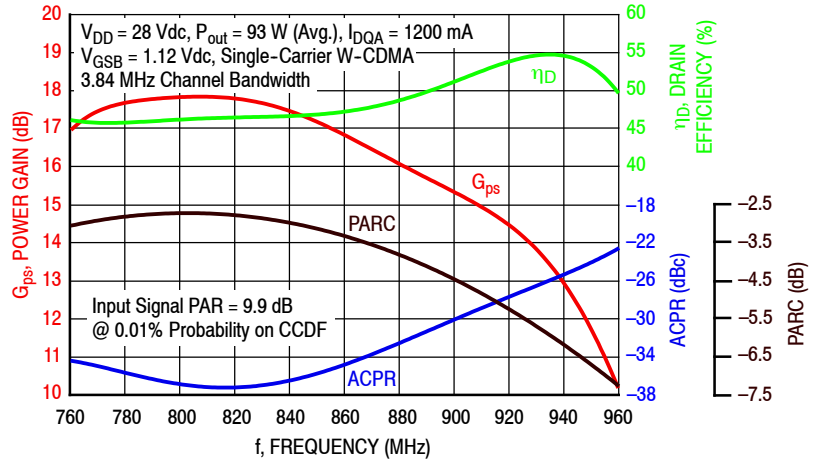


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 93 Watts Avg.

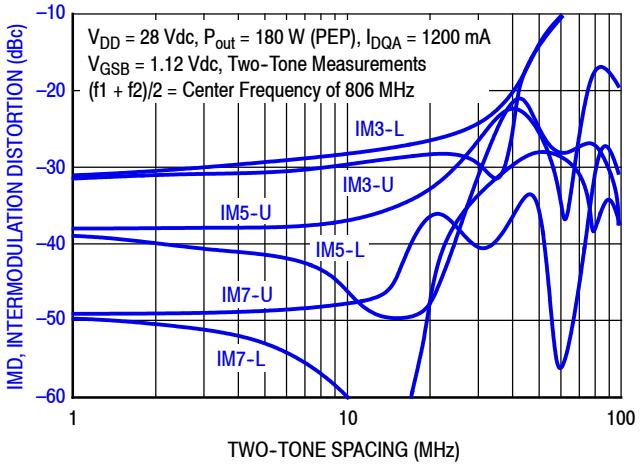


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

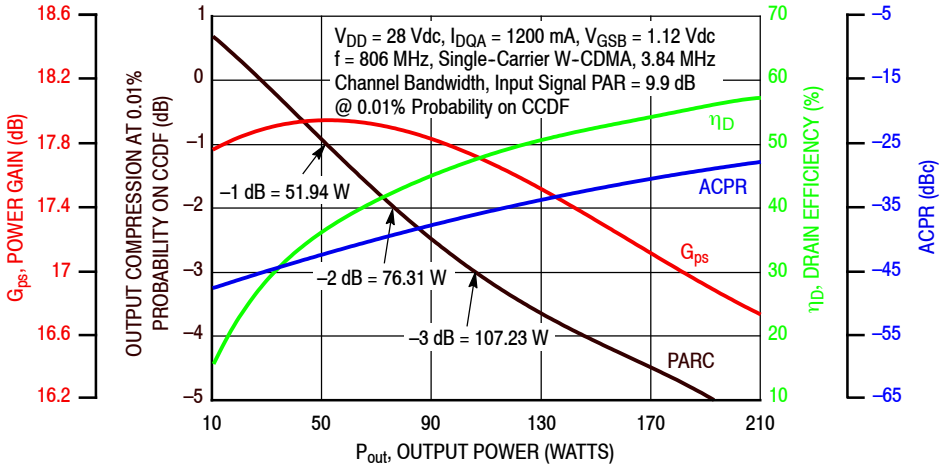


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

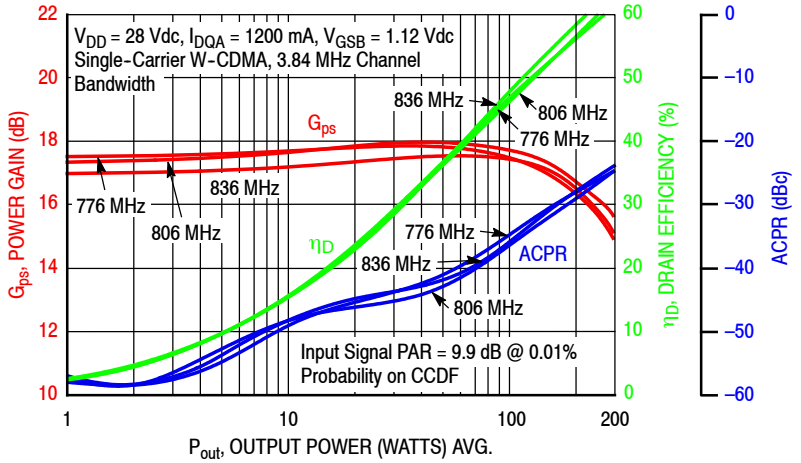


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

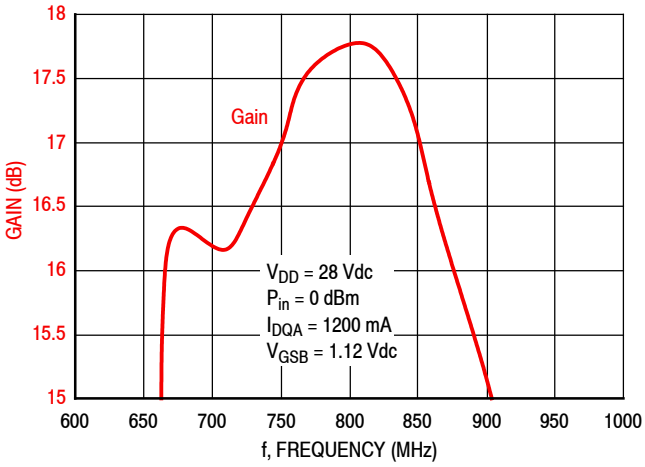


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1442 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	1.29 – j2.52	1.33 + j2.52	0.63 – j0.95	16.2	54.6	289	48.9	–4
748	1.36 – j2.68	1.38 + j2.62	0.69 – j0.80	16.5	54.6	286	52.4	–6
768	1.53 – j2.97	1.44 + j2.82	0.79 – j0.87	16.4	53.7	233	46.8	–4
790	1.61 – j3.18	1.61 + j3.02	0.69 – j0.95	16.2	54.5	283	51.4	–4
806	1.71 – j3.34	1.71 + j3.19	0.70 – j0.95	16.3	54.5	281	52.6	–4
822	1.76 – j3.51	1.82 + j3.36	0.71 – j0.99	16.3	54.5	279	53.1	–4

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	1.29 – j2.52	1.21 + j2.63	0.60 – j1.03	14.0	55.7	368	53.3	–8
748	1.36 – j2.68	1.28 + j2.74	0.64 – j1.03	14.0	55.4	347	53.1	–9
768	1.53 – j2.97	1.34 + j2.94	0.79 – j1.04	14.3	54.9	310	52.3	–7
790	1.61 – j3.18	1.49 + j3.14	0.71 – j1.05	14.1	55.3	342	54.4	–9
806	1.71 – j3.34	1.59 + j3.33	0.70 – j1.07	14.1	55.3	342	54.5	–8
822	1.76 – j3.51	1.72 + j3.52	0.55 – j1.18	13.0	55.3	337	48.9	–7

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

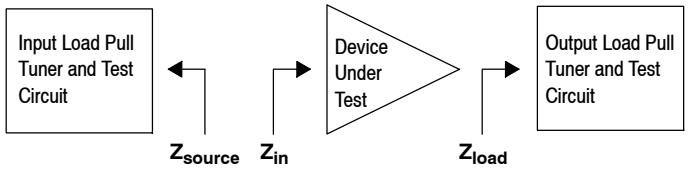


Table 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1442 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	1.29 – j2.52	1.19 + j2.57	2.14 – j0.27	20.3	52.1	164	67.8	–12
748	1.36 – j2.68	1.29 + j2.66	1.85 – j0.46	19.7	52.3	169	63.8	–13
768	1.53 – j2.97	1.35 + j2.86	2.11 – j0.11	20.2	51.4	138	60.4	–5
790	1.61 – j3.18	1.43 + j3.08	2.25 + j0.30	20.7	51.1	129	67.7	–12
806	1.71 – j3.34	1.50 + j3.24	1.92 + j0.22	20.4	51.4	138	68.1	–14
822	1.76 – j3.51	1.62 + j3.39	1.76 + j0.02	20.1	51.7	147	67.8	–13

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	1.29 – j2.52	1.11 + j2.65	2.52 – j0.44	18.6	52.4	173	69.5	–19
748	1.36 – j2.68	1.20 + j2.75	1.78 – j0.52	17.6	53.2	210	66.0	–19
768	1.53 – j2.97	1.30 + j3.03	3.21 – j0.14	19.3	51.3	134	66.5	–13
790	1.61 – j3.18	1.39 + j3.19	2.35 – j0.16	18.6	52.2	168	70.2	–16
806	1.71 – j3.34	1.46 + j3.36	2.14 – j0.09	18.4	52.2	168	69.6	–19
822	1.76 – j3.51	1.54 + j3.53	2.00 – j0.02	18.3	52.1	164	69.4	–20

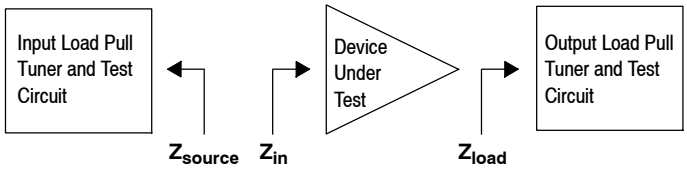
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 790 MHz

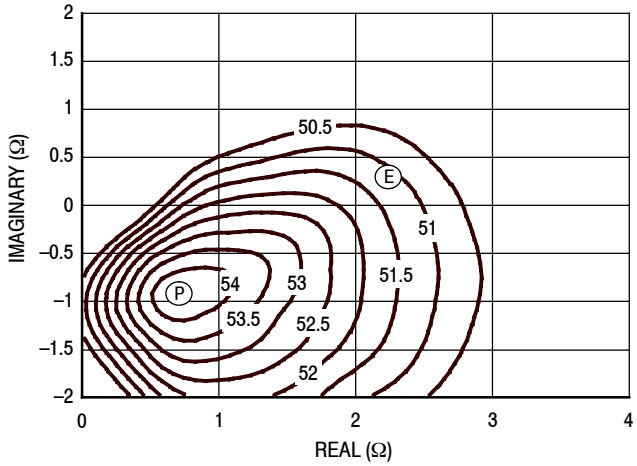


Figure 8. P1dB Load Pull Output Power Contours (dBm)

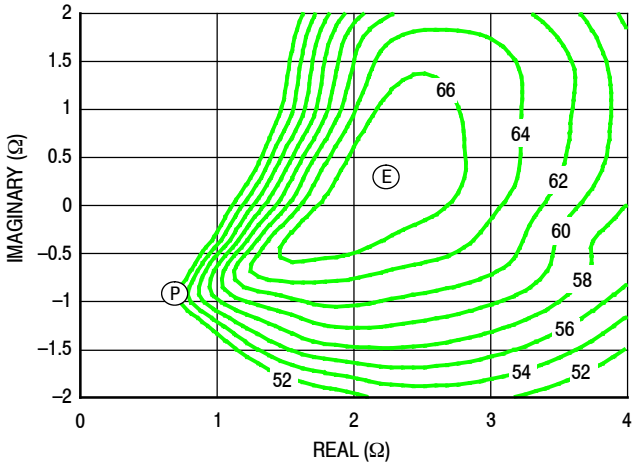


Figure 9. P1dB Load Pull Efficiency Contours (%)

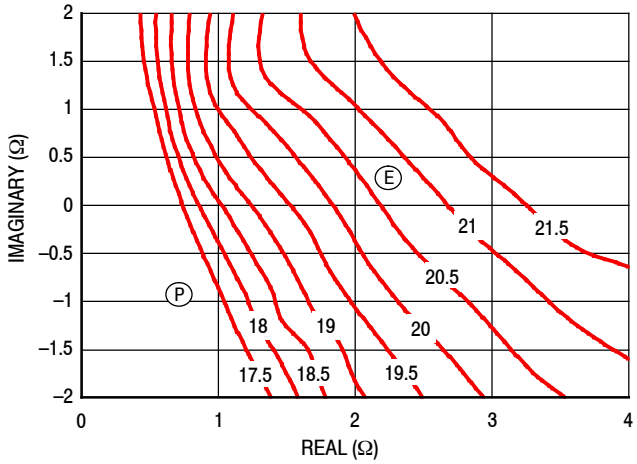


Figure 10. P1dB Load Pull Gain Contours (dB)

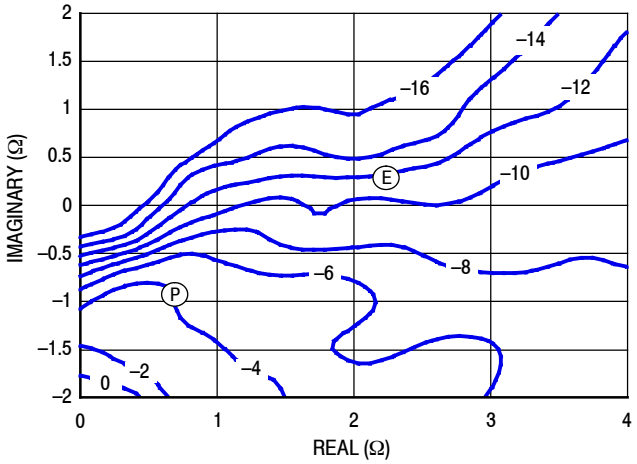


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 790 MHz

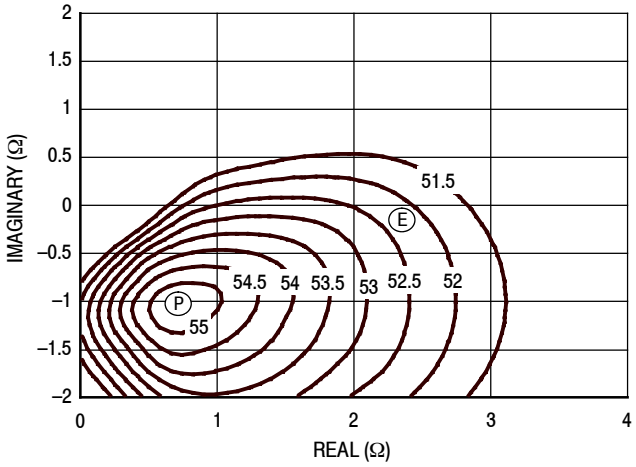


Figure 12. P3dB Load Pull Output Power Contours (dBm)

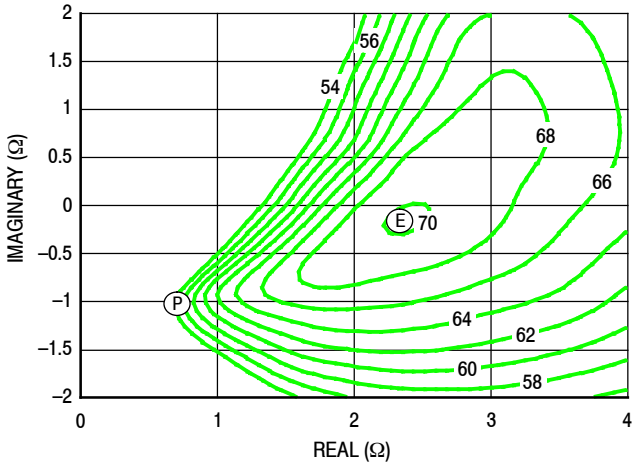


Figure 13. P3dB Load Pull Efficiency Contours (%)

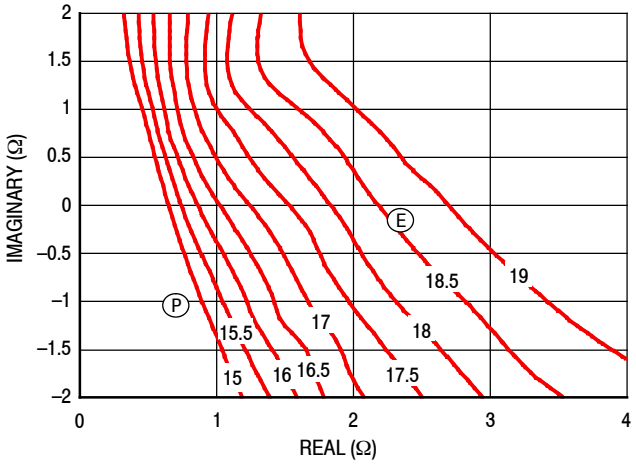


Figure 14. P3dB Load Pull Gain Contours (dB)

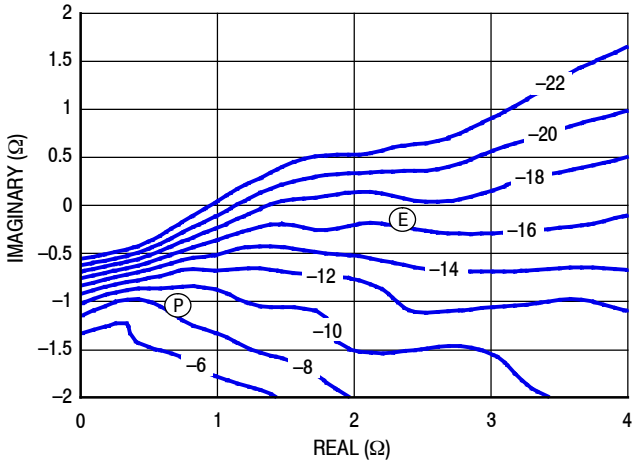


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

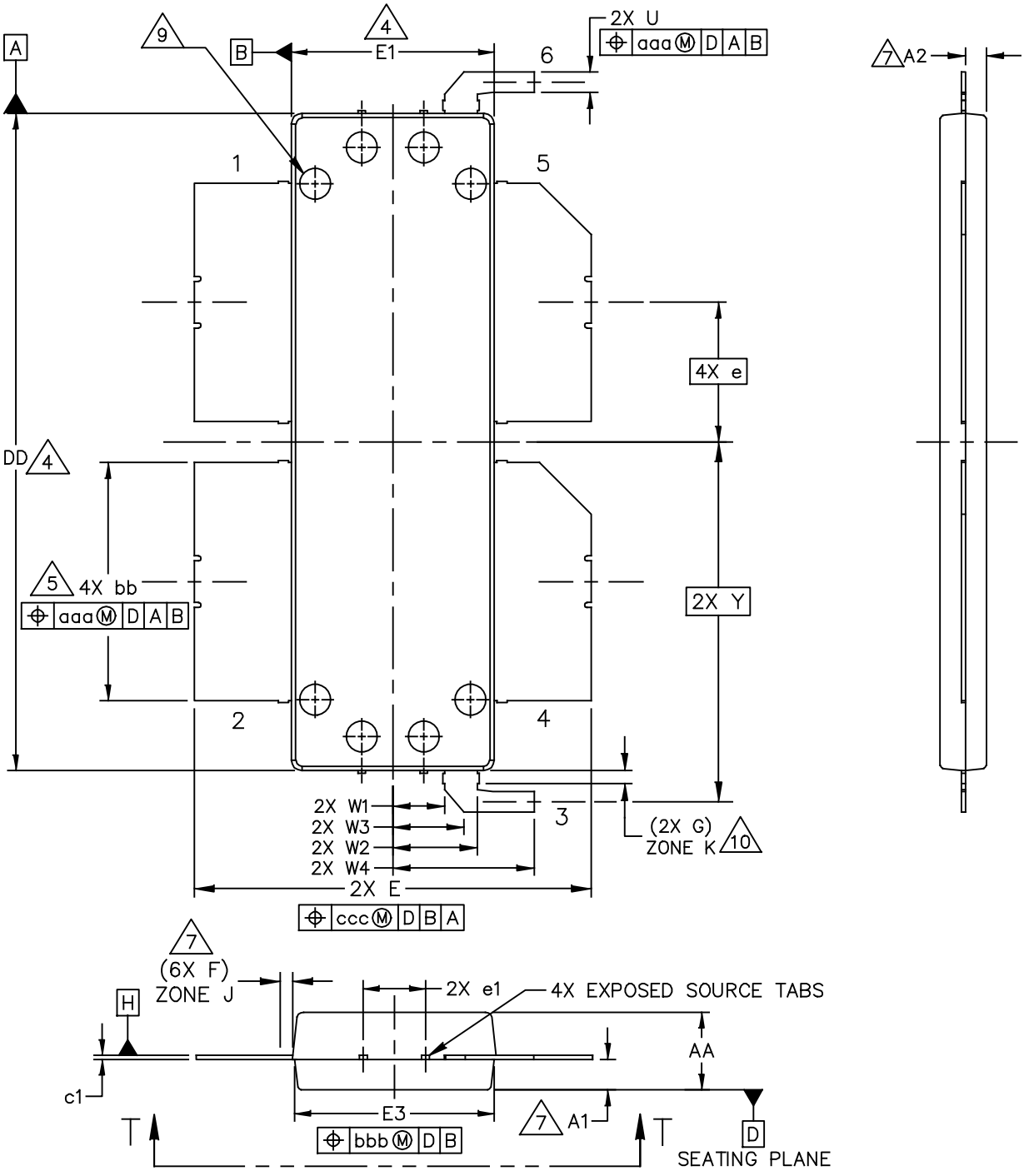
Gain

Drain Efficiency

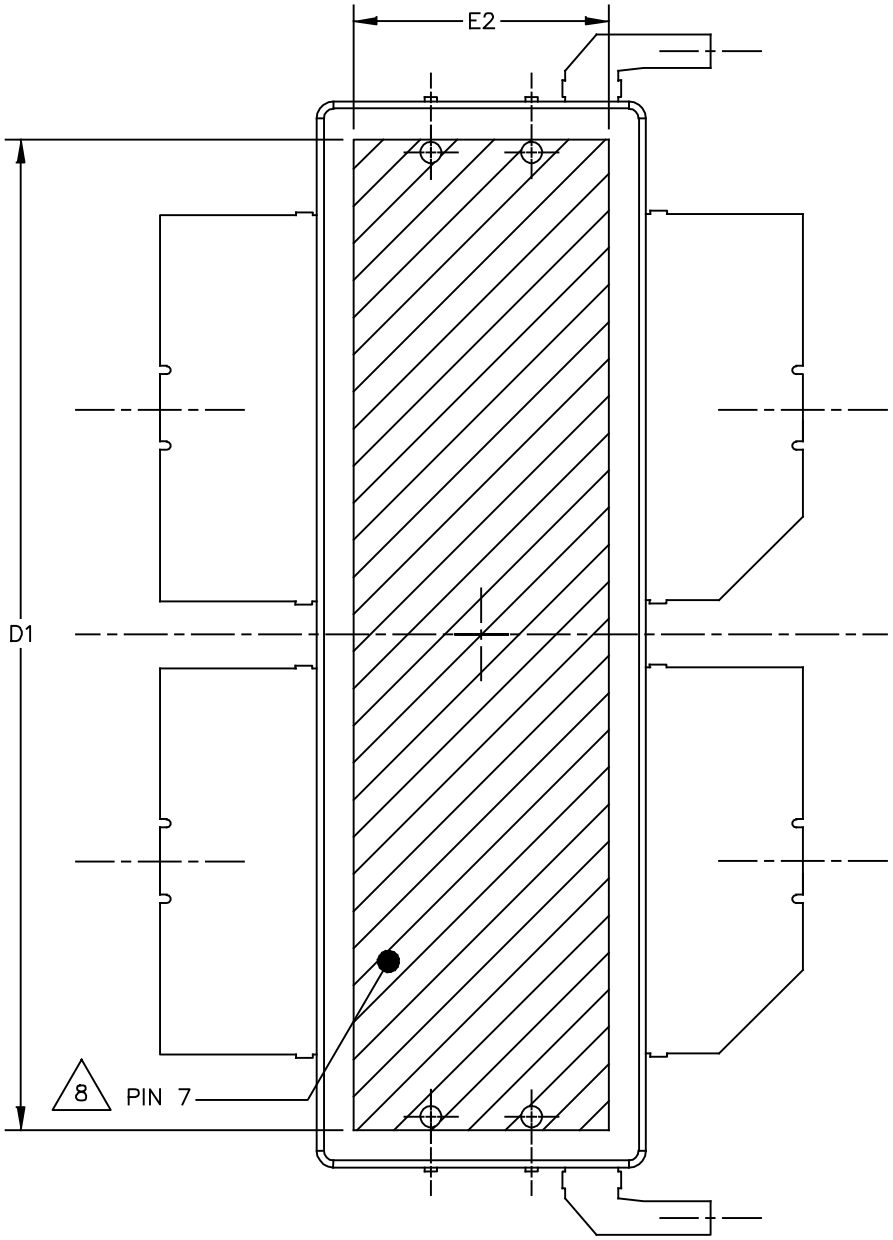
Linearity

Output Power

PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	
	10 JUL 2015	



BOTTOM VIEW
VIEW T–T

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	STANDARD: NON–JEDEC	
	10 JUL 2015	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON–SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	W2	.158	.168	4.01	4.27
A1	.059	.065	1.50	1.65	W3	.132	.142	3.35	3.61
A2	.056	.068	1.42	1.73	W4	.265	.281	6.73	7.14
DD	1.267	1.273	32.18	32.33	U	.037	.043	0.94	1.09
D1	1.180	----	29.97	----	Y	.695 BSC		17.65 BSC	
E	.762	.770	19.35	19.56	bb	.457	.463	11.61	11.76
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.270 BSC		6.86 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 REF		0.64 REF		aaa	.004		0.10	
G	.030 REF		0.76 REF		bbb	.006		0.15	
W1	.095	.105	2.41	2.67	ccc	.010		0.25	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2016	• Initial release of Data Sheet

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