Document Number: A3G18H500-04S
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RoHS

# RF Power GaN Transistor

**A3G18H500-04SR3**

**1805–2200 MHz, 107 W AVG., 48 V AIRFAST RF POWER GaN TRANSISTOR**

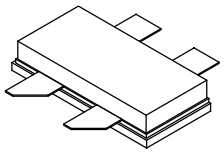
This 107 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1805 to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

### 1800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 200 mA, $V_{GSB}$ = –5 Vdc, $P_{out}$ = 107 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

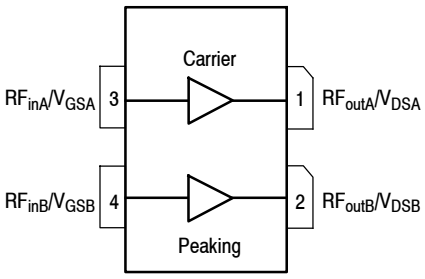
| Frequency | $G_{ps}$ (dB) | $\eta_D$ (%) | Output PAR (dB) | ACPR (dBc) |
|---|---|---|---|---|
| 1805 MHz | 15.3 | 58.4 | 7.1 | –31.9 |
| 1840 MHz | 15.4 | 57.7 | 7.0 | –33.2 |
| 1880 MHz | 15.4 | 57.7 | 6.7 | –33.8 |



**NI-780S-4L**

### Features

- High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Able to withstand extremely high output VSWR and broadband operating conditions




(Top View)

**Figure 1. Pin Connections**

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**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 125 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | –8, 0 | Vdc |
| Operating Voltage | $V_{DD}$ | 0 to +55 | Vdc |
| Maximum Forward Gate Current @ $T_C$ = 25°C | $I_{GMAX}$ | 25 | mA |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature Range | $T_C$ | –55 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | –55 to +225 | °C |
| Absolute Maximum Junction Temperature (1) | $T_{MAX}$ | 275 | °C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 76°C, $P_D$ = 94.2 W | $R_{\theta JC}$ (IR) | 0.60 (2) | °C/W |
| Thermal Resistance by Finite Element Analysis, Junction-to-Case Case Temperature 76°C, $P_D$ = 94.2 W | $R_{\theta JC}$ (FEA) | 1.02 (3) | °C/W |

**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 1B |
| Charge Device Model (per JESD22-C101) | C3 |

**Table 4. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics (4)** | | | | | | |
| Drain-Source Breakdown Voltage | | $V_{(BR)DSS}$ | | — | — | Vdc |
| ($V_{GS}$ = –8 Vdc, $I_D$ = 24.3 mAdc) | Carrier | | 150 | | | |
| ($V_{GS}$ = –8 Vdc, $I_D$ = 35.1 mAdc) | Peaking | | 150 | | | |
| **On Characteristics - Side A, Carrier** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 24.3 mAdc) | | $V_{GS(th)}$ | –3.8 | –3.0 | –2.3 | Vdc |
| Gate Quiescent Voltage ($V_{DD}$ = 48 Vdc, $I_D$ = 200 mAdc, Measured in Functional Test) | | $V_{GSA(Q)}$ | –3.6 | –3.0 | –2.3 | Vdc |
| Gate-Source Leakage Current ($V_{DS}$ = 0 Vdc, $V_{GS}$ = –5 Vdc) | | $I_{GSS}$ | –7.5 | — | — | mAdc |
| **On Characteristics - Side B, Peaking** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 20 mAdc) | | $V_{GS(th)}$ | –3.8 | –3.3 | –2.3 | Vdc |
| Gate-Source Leakage Current ($V_{DS}$ = 0 Vdc, $V_{GS}$ = –5 Vdc) | | $I_{GSS}$ | –7.7 | — | — | mAdc |

1. Functional operation above 225°C has not been characterized and is not implied. Operation at $T_{MAX}$ (275°C) reduces median time to failure by an order of magnitude; operation beyond $T_{MAX}$ could cause permanent damage.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
3. $R_{\theta JC}$ (FEA) must be used for purposes related to reliability and limitations on maximum junction temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the junction temperature in degrees Celsius, *A* = –10.3 and *B* = 8260.
4. Each side of device measured separately.

(continued)

**Table 4. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Functional Tests** (1,2) (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 200 mA, $V_{GSB}$ = –5 Vdc, $P_{out}$ = 107 W Avg., f = 1840 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. **[See note on correct biasing sequence.]** | | | | | |
| Power Gain | $G_{ps}$ | 14.5 | 15.4 | 17.5 | dB |
| Drain Efficiency | $\eta_D$ | 53.0 | 57.7 | — | % |
| Output Peak-to-Average Ratio @ 0.01% Probability on CCDF | PAR | 6.3 | 7.0 | — | dB |
| Adjacent Channel Power Ratio | ACPR | — | –33.2 | –29.0 | dBc |
| **Load Mismatch** (In NXP Test Fixture, 50 ohm system) $I_{DQA}$ = 200 mA, $V_{GSB}$ = –5 Vdc, f = 1840 MHz, 12 μsec(on), 10% Duty Cycle | | | | | |
| VSWR 10:1 at 55 Vdc, 575 W Pulsed CW Output Power (3 dB Input Overdrive from 417 W Pulsed CW Rated Power) | No Device Degradation | | | | |
| **Typical Performance** (2) (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD}$ = 48 Vdc, $I_{DQA}$ = 200 mA, $V_{GSB}$ = –5 Vdc, 1805–1880 MHz Bandwidth | | | | | |
| $P_{out}$ @ 3 dB Compression Point (3) | P3dB | — | 537 | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth) | Φ | — | –15 | — | ° |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | 200 | — | MHz |
| Gain Flatness in 75 MHz Bandwidth @ $P_{out}$ = 107 W Avg. | $G_F$ | — | 0.3 | — | dB |
| Gain Variation over Temperature (–30°C to +85°C) | ΔG | — | 0.009 | — | dB/°C |
| Output Power Variation over Temperature (–30°C to +85°C) | ΔP1dB | — | 0.004 | — | dB/°C |

**Table 5. Ordering Information**

| Device | Tape and Reel Information | Package |
|---|---|---|
| A3G18H500-04SR3 | R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel | NI-780S-4L |

1. Part internally input matched.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = $P_{avg}$ + 7.0 dB where $P_{avg}$ is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

## NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

### Bias ON the device

1. Set gate voltage $V_{GSA}$ and $V_{GSB}$ to –5 V.
2. Set drain voltage $V_{DSA}$ and $V_{DSB}$ to nominal supply voltage (+48 V).
3. Increase $V_{GSA}$ (carrier side) until $I_{DQA}$ current is attained.
4. Increase $V_{GSB}$ (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

### Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage $V_{GSA}$ and $V_{GSB}$ to –5 V.
3. Adjust drain voltage $V_{DSA}$ and $V_{DSB}$ to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable $V_{GSA}$ and $V_{GSB}$.

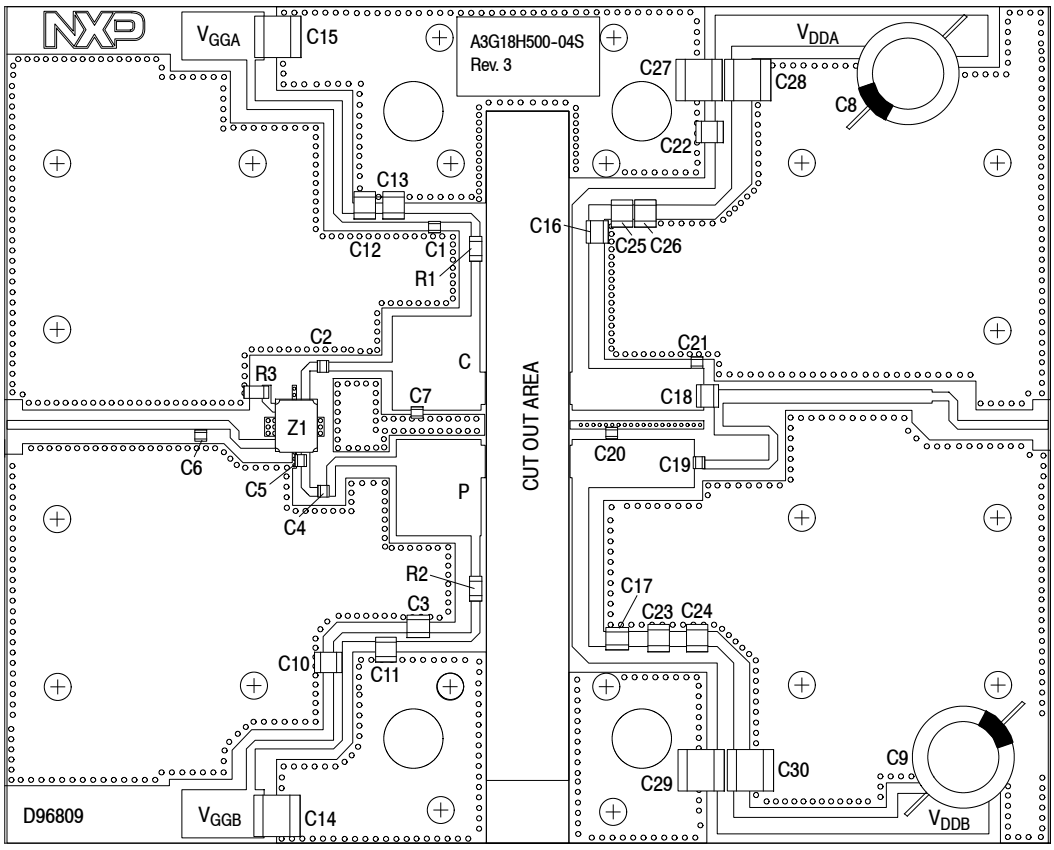



**Figure 2. A3G18H500-04SR3 Test Circuit Component Layout**

**Table 6. A3G18H500-04SR3 Test Circuit Component Designations and Values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C2 | 10 pF Chip Capacitor | GQM2195C2E100JB12 | Murata |
| C3, C16, C17 | 10 pF Chip Capacitor | ATC100B100GT500XT | ATC |
| C4, C19 | 15 pF Chip Capacitor | GQM2195C2E150JB12 | Murata |
| C5 | 0.9 pF Chip Capacitor | GQM2195C2ER90BB12 | Murata |
| C6 | 0.8 pF Chip Capacitor | GQM2195C2ER80BB12 | Murata |
| C7, C21 | 0.6 pF Chip Capacitor | GQM2195C2ER60BB12 | Murata |
| C8, C9 | 470 μF, 63 V Electrolytic Capacitor | MCGPR63V477M13X26-RH | Multicomp |
| C10, C11, C12, C13, C22, C23, C24, C25, C26 | 10 μF Chip Capacitor | C3225X7S1H106K | TDK |
| C14, C15, C27, C28, C29, C30 | 10 μF Chip Capacitor | C5750X7S2A106M | TDK |
| C18 | 3 pF Chip Capacitor | ATC100B3R0BT500XT | ATC |
| C20 | 1.3 pF Chip Capacitor | GQM2195C2E1R3BB12 | Murata |
| R1, R2 | 3.3 Ω, 1/4 W Chip Resistor | CRCW08053R30FKEA | Vishay |
| R3 | 50 Ω, 8 W Termination Chip Resistor | C8A50Z4A | Anaren |
| Z1 | 1800–2200 MHz Band, 90°, 2 dB Directional Coupler | X3C20F1-02S | Anaren |
| PCB | Rogers RO4350B, 0.020″, $\varepsilon_r$ = 3.66 | D96809 | MTL |

## TYPICAL CHARACTERISTICS — 1805–1880 MHz

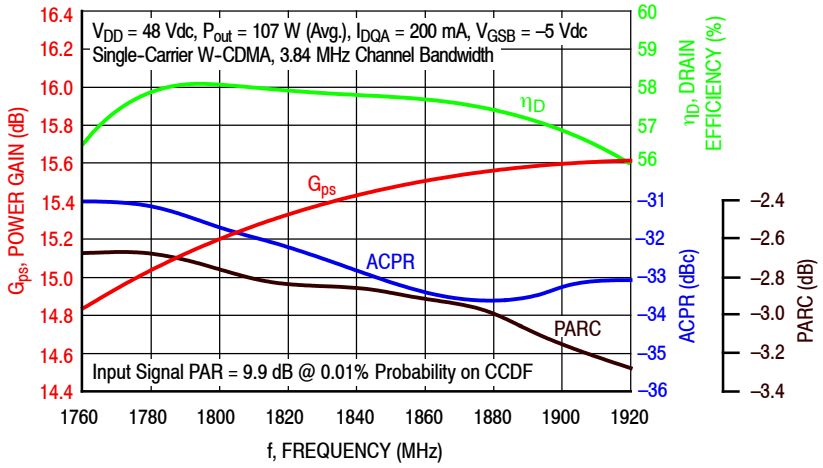



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 107 Watts Avg.**

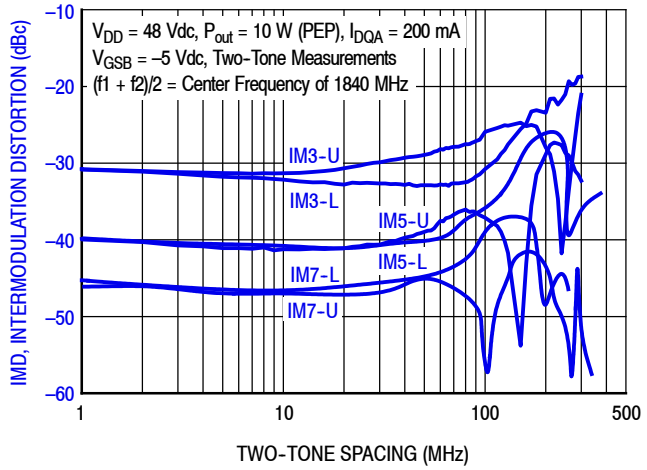



**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

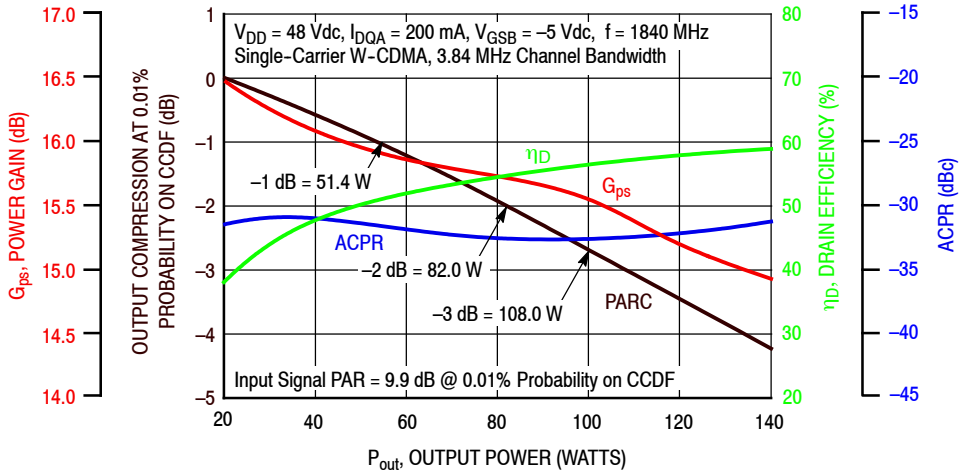



**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

## TYPICAL CHARACTERISTICS — 1805–1880 MHz

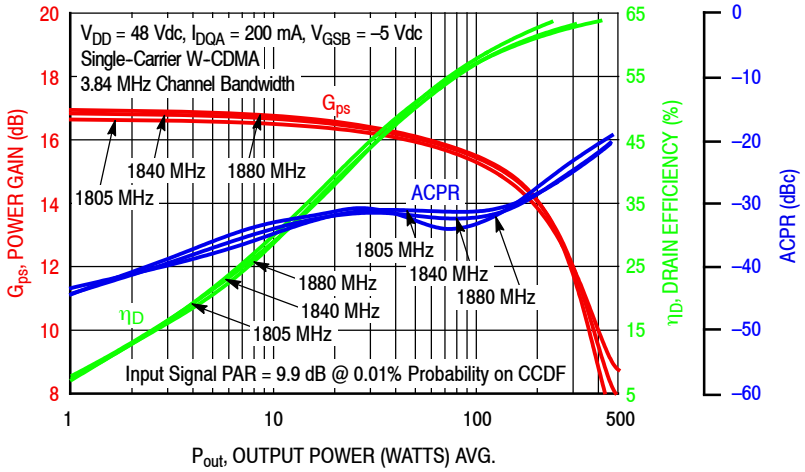



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

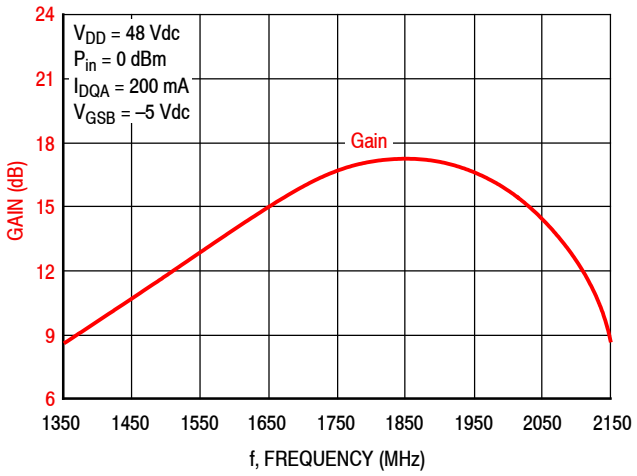



**Figure 7. Broadband Frequency Response**

**Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQA}$ = 250 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 2.56 – j6.80 | 2.88 + j6.46 | 4.22 – j7.66 | 17.9 | 53.3 | 215 | 60.6 | –9 |
| 1840 | 3.18 – j7.25 | 3.29 + j6.72 | 4.33 – j8.32 | 17.8 | 53.2 | 210 | 58.6 | –9 |
| 1880 | 3.88 – j7.65 | 3.69 + j6.85 | 4.43 – j8.45 | 17.8 | 53.0 | 201 | 58.1 | –9 |

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 2.56 – j6.80 | 2.63 + j6.74 | 5.40 – j8.08 | 16.2 | 54.2 | 265 | 65.1 | –11 |
| 1840 | 3.18 – j7.25 | 3.01 + j7.11 | 5.30 – j8.38 | 16.2 | 54.1 | 256 | 63.9 | –12 |
| 1880 | 3.88 – j7.65 | 3.52 + j7.35 | 5.88 – j9.20 | 16.2 | 54.0 | 251 | 62.5 | –12 |

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

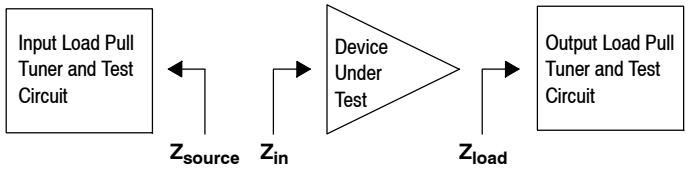
**Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQA}$ = 250 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 2.56 – j6.80 | 2.52 + j6.98 | 3.66 – j4.40 | 19.4 | 51.8 | 151 | 71.3 | –23 |
| 1840 | 3.18 – j7.25 | 2.81 + j7.53 | 3.39 – j4.12 | 19.6 | 51.0 | 126 | 70.5 | –26 |
| 1880 | 3.88 – j7.65 | 3.38 + j7.76 | 3.61 – j4.65 | 19.5 | 51.1 | 130 | 68.1 | –25 |

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 2.56 – j6.80 | 2.23 + j7.22 | 3.93 – j4.40 | 17.5 | 52.6 | 181 | 75.4 | –29 |
| 1840 | 3.18 – j7.25 | 2.63 + j7.72 | 4.03 – j4.47 | 17.6 | 52.4 | 175 | 74.3 | –29 |
| 1880 | 3.88 – j7.65 | 3.25 + j8.11 | 4.53 – j5.02 | 17.7 | 52.5 | 176 | 72.2 | –27 |

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



## P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

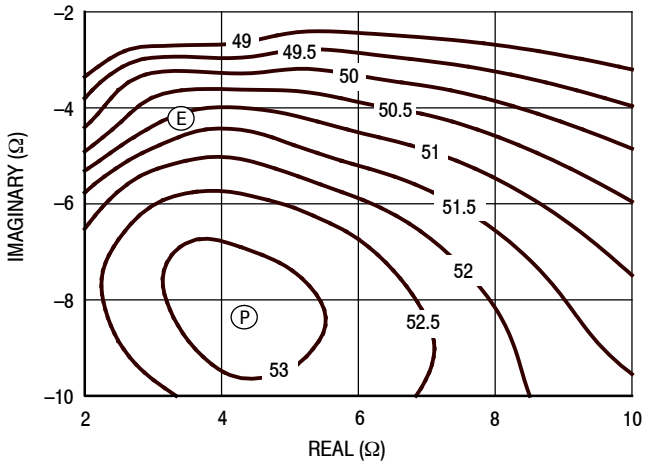



**Figure 8. P1dB Load Pull Output Power Contours (dBm)**

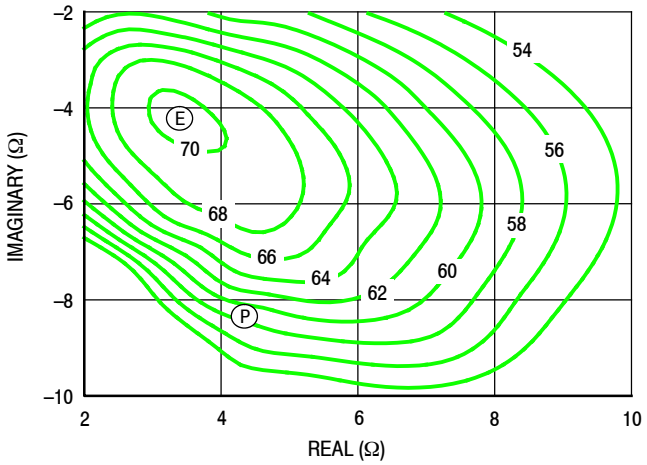



**Figure 9. P1dB Load Pull Efficiency Contours (%)**

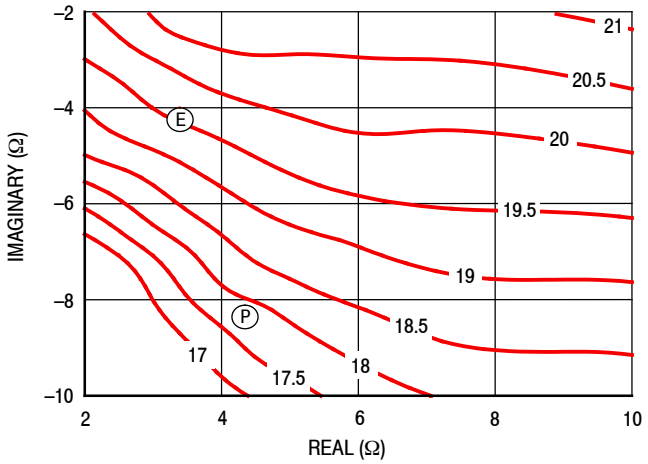



**Figure 10. P1dB Load Pull Gain Contours (dB)**

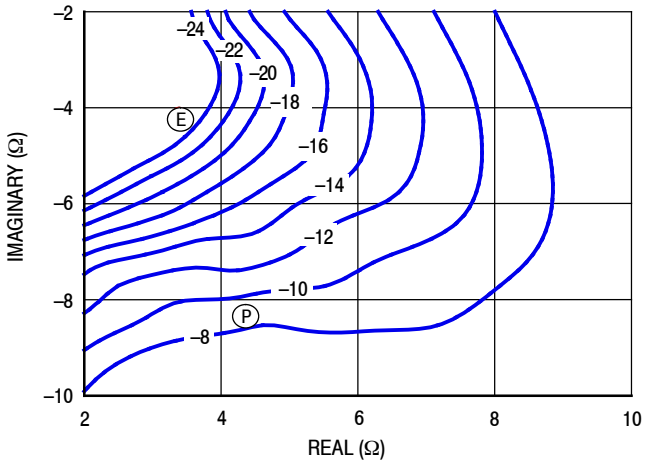



**Figure 11. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

## P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

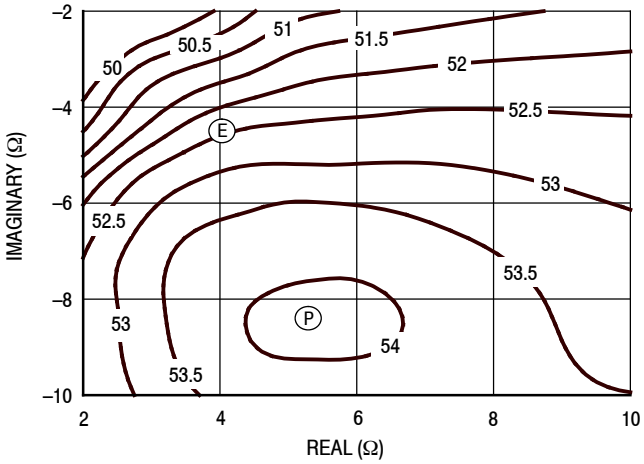



**Figure 12. P3dB Load Pull Output Power Contours (dBm)**

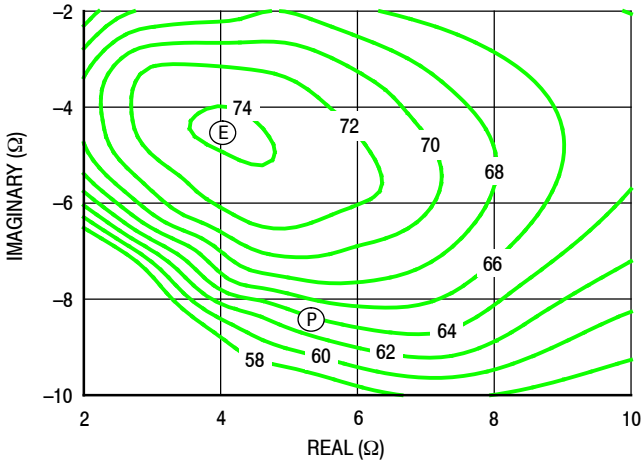



**Figure 13. P3dB Load Pull Efficiency Contours (%)**

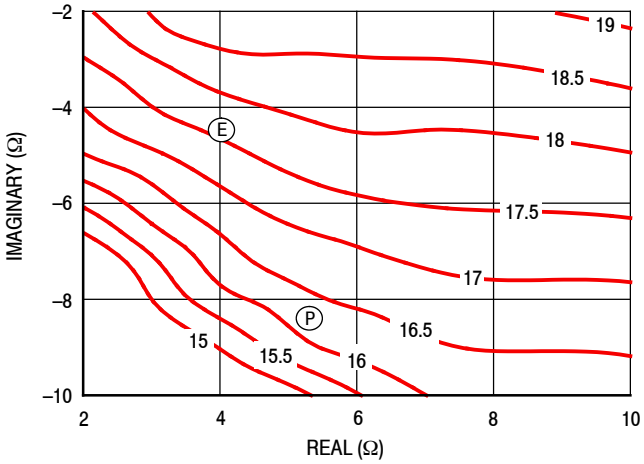



**Figure 14. P3dB Load Pull Gain Contours (dB)**

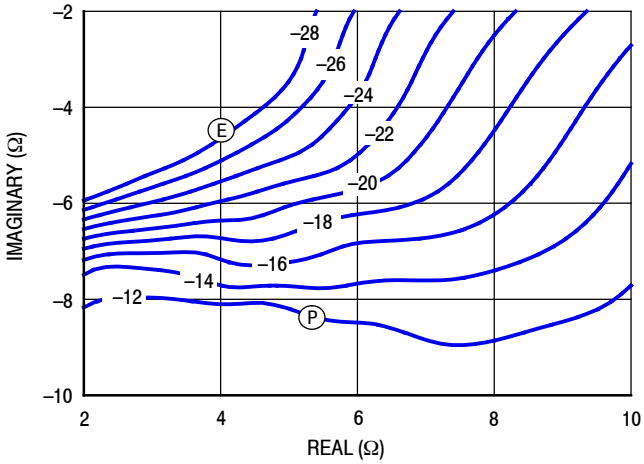



**Figure 15. P3dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

**Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 48 Vdc, $V_{GSB}$ = 3.1 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Output Power P1dB $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
|---|---|---|---|---|---|---|---|---|
| 1805 | 1.66 – j6.38 | 1.51 + j6.91 | 1.79 – j4.63 | 17.7 | 54.8 | 302 | 54.5 | –13 |
| 1840 | 2.64 – j7.07 | 2.11 + j7.34 | 2.06 – j4.97 | 17.8 | 54.7 | 297 | 54.3 | –13 |
| 1880 | 2.30 – j7.54 | 2.13 + j7.92 | 2.01 – j5.25 | 17.8 | 54.6 | 292 | 53.2 | –13 |

| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Output Power P3dB $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
|---|---|---|---|---|---|---|---|---|
| 1805 | 1.66 – j6.38 | 1.37 + j6.95 | 2.61 – j5.42 | 16.0 | 56.0 | 398 | 58.7 | –13 |
| 1840 | 2.64 – j7.07 | 2.02 + j7.47 | 2.86 – j5.78 | 15.9 | 55.8 | 378 | 56.4 | –13 |
| 1880 | 2.30 – j7.54 | 2.02 + j8.07 | 2.87 – j5.92 | 16.1 | 55.6 | 365 | 56.8 | –13 |

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

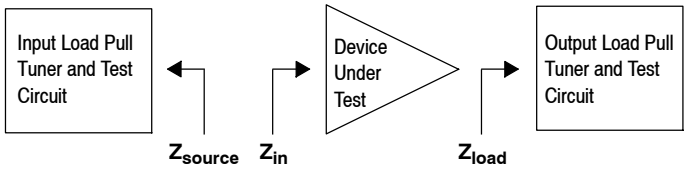
**Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 48 Vdc, $V_{GSB}$ = 3.1 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Drain Efficiency P1dB $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
|---|---|---|---|---|---|---|---|---|
| 1805 | 1.66 – j6.38 | 1.46 + j7.24 | 1.79 – j3.09 | 19.3 | 53.1 | 203 | 63.1 | –25 |
| 1840 | 2.64 – j7.07 | 2.04 + j7.76 | 2.02 – j3.16 | 19.3 | 53.0 | 200 | 63.8 | –25 |
| 1880 | 2.30 – j7.54 | 2.06 + j8.33 | 2.04 – j3.54 | 19.5 | 53.1 | 203 | 62.0 | –24 |

| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | Max Drain Efficiency P3dB $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
|---|---|---|---|---|---|---|---|---|
| 1805 | 1.66 – j6.38 | 1.38 + j7.43 | 2.15 – j2.96 | 17.7 | 53.9 | 247 | 69.4 | –32 |
| 1840 | 2.64 – j7.07 | 1.93 + j8.02 | 2.37 – j3.17 | 17.6 | 54.1 | 256 | 68.9 | –30 |
| 1880 | 2.30 – j7.54 | 2.01 + j8.60 | 2.52 – j3.41 | 17.9 | 54.0 | 250 | 67.1 | –30 |

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



## P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

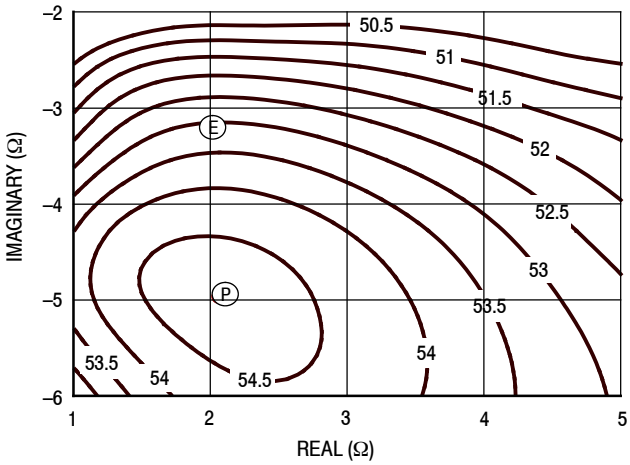



**Figure 16. P1dB Load Pull Output Power Contours (dBm)**

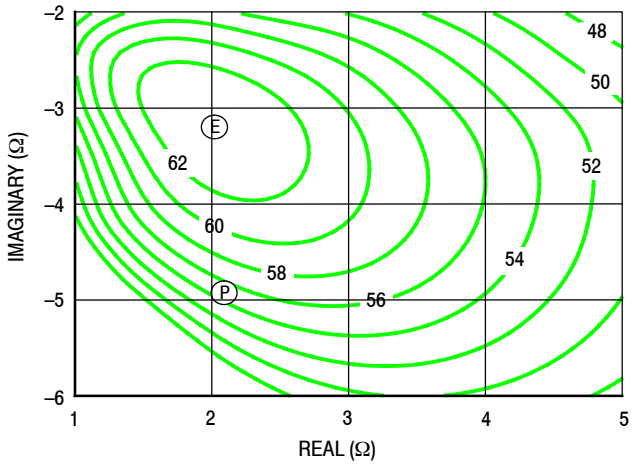



**Figure 17. P1dB Load Pull Efficiency Contours (%)**

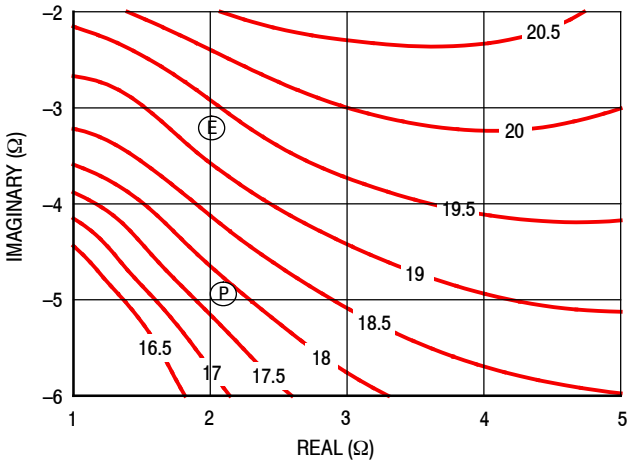



**Figure 18. P1dB Load Pull Gain Contours (dB)**

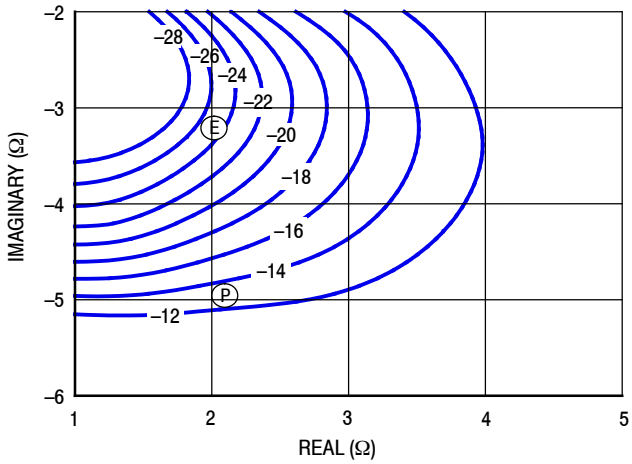



**Figure 19. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

## P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

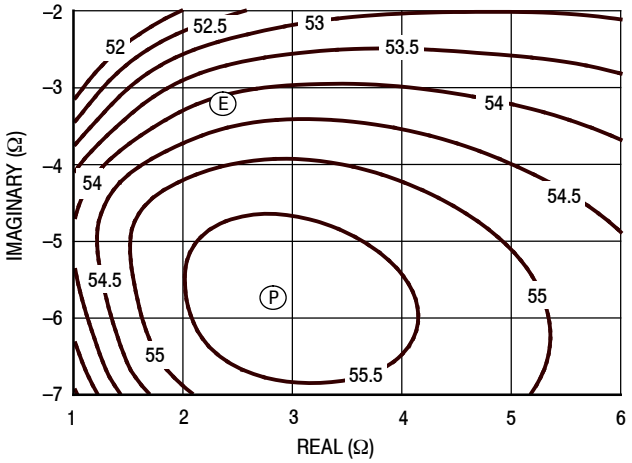



**Figure 20. P3dB Load Pull Output Power Contours (dBm)**

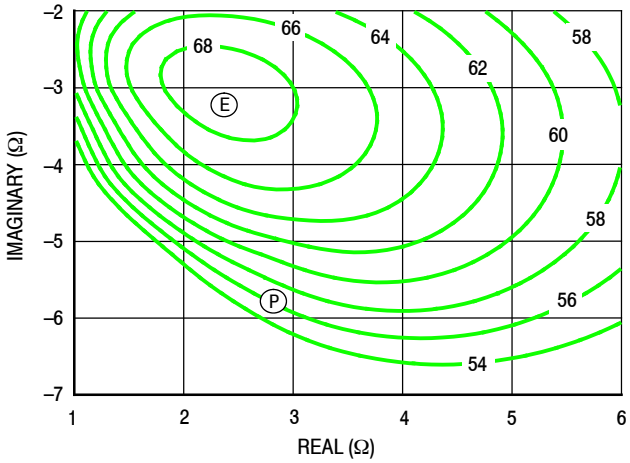



**Figure 21. P3dB Load Pull Efficiency Contours (%)**

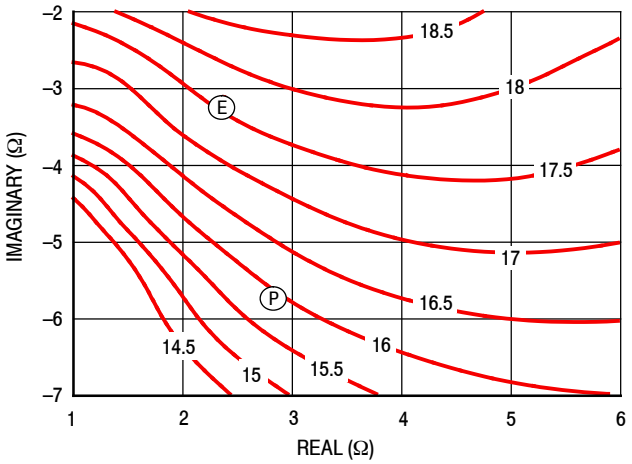



**Figure 22. P3dB Load Pull Gain Contours (dB)**

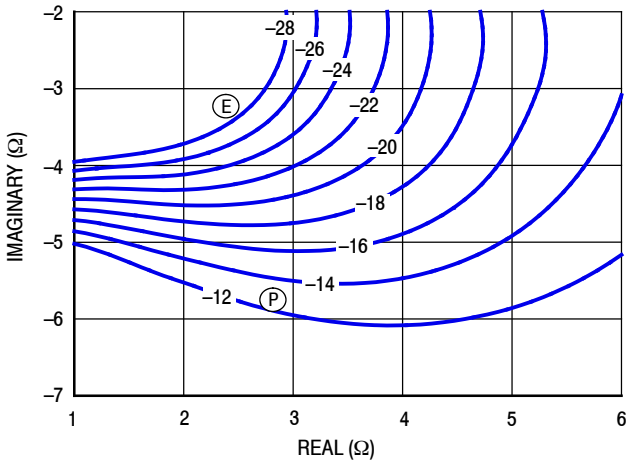



**Figure 23. P3dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

## P3dB LOAD PULL PERFORMANCE, CARRIER — 1800–2200 MHz

**Table 11. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQA}$ = 250 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Output Power | | | | |
|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | $\eta_D$ (%) | AM/PM (°) |
| 1800 | 2.56 – j6.80 | 2.60 + j6.70 | 5.40 – j8.08 | 16.2 | 54.2 | 65.1 | –11 |
| 1840 | 3.20 – j7.30 | 3.00 + j7.10 | 5.30 – j8.38 | 16.2 | 54.1 | 63.9 | –12 |
| 1880 | 3.90 – j7.70 | 3.50 + j7.40 | 5.88 – j9.20 | 16.2 | 54.0 | 62.5 | –12 |
| 1930 | 3.90 – j7.70 | 4.10 + j7.78 | 6.00 – j9.40 | 16.4 | 54.0 | 63.2 | –13 |
| 1990 | 5.60 – j7.11 | 5.30 + j7.70 | 6.60 – j9.80 | 16.6 | 54.0 | 64.0 | –13 |
| 2110 | 7.80 – j5.70 | 7.10 + j5.70 | 6.50 – j10.8 | 16.5 | 53.9 | 64.2 | –15 |
| 2200 | 7.50 – j1.70 | 6.30 + j2.90 | 7.04 – j12.0 | 16.2 | 53.8 | 59.4 | –15 |

(1) Load impedance for optimum P3dB power.

$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$ = Impedance as measured from gate contact to ground.

$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

**Table 12. Carrier Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQA}$ = 250 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

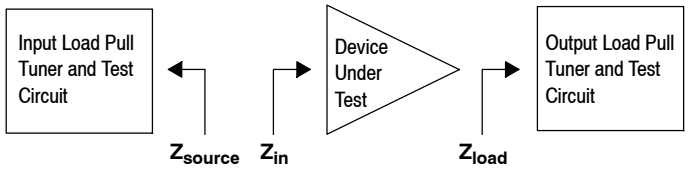
| | | | Max Drain Efficiency | | | | |
|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | $\eta_D$ (%) | AM/PM (°) |
| 1800 | 2.56 – j6.80 | 2.20 + j7.20 | 3.93 – j4.40 | 17.5 | 52.6 | 75.4 | –29 |
| 1840 | 3.20 – j7.30 | 2.60 + j7.70 | 4.00 – j4.50 | 17.6 | 52.4 | 74.3 | –29 |
| 1880 | 3.90 – j7.70 | 3.30 + j8.10 | 4.50 – j5.00 | 17.7 | 52.5 | 72.2 | –27 |
| 1930 | 3.90 – j7.70 | 3.90 + j8.70 | 4.30 – j5.30 | 17.7 | 52.4 | 71.7 | –29 |
| 1990 | 5.60 – j7.11 | 5.38 + j8.80 | 4.46 – j5.90 | 17.8 | 52.4 | 72.7 | –27 |
| 2110 | 7.80 – j5.70 | 8.20 + j6.00 | 5.10 – j7.40 | 17.7 | 53.0 | 72.9 | –26 |
| 2200 | 7.50 – j1.70 | 6.80 + j2.30 | 5.60 – j8.40 | 17.5 | 53.0 | 68.5 | –24 |

(1) Load impedance for optimum P3dB efficiency.

$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$ = Impedance as measured from gate contact to ground.

$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



## P3dB LOAD PULL PERFORMANCE, PEAKING — 1800–2200 MHz

**Table 13. Peaking Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQB}$ = 350 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Output Power | | | | |
|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | $\eta_D$ (%) | AM/PM (°) |
| 1800 | 2.56 – j6.80 | 2.20 + j6.30 | 2.90 – j5.90 | 15.6 | 55.7 | 62.9 | –7 |
| 1880 | 2.80 – j6.90 | 2.83 + j7.00 | 2.90 – j6.10 | 16.1 | 55.5 | 62.8 | –9 |
| 1930 | 3.00 – j7.16 | 3.50 + j7.00 | 3.53 – j7.50 | 15.7 | 55.5 | 57.1 | –7 |
| 1990 | 4.50 – j7.10 | 4.20 + j6.90 | 3.10 – j6.93 | 16.2 | 55.6 | 61.4 | –9 |
| 2110 | 4.80 – j4.70 | 4.50 + j4.80 | 3.00 – j7.60 | 16.5 | 55.7 | 61.3 | –10 |
| 2200 | 4.20 – j3.00 | 3.01 + j3.70 | 3.10 – j8.20 | 16.5 | 55.6 | 59.6 | –12 |

(1) Load impedance for optimum P3dB power.

$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$ = Impedance as measured from gate contact to ground.

$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

**Table 14. Peaking Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 48 Vdc, $I_{DQB}$ = 350 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

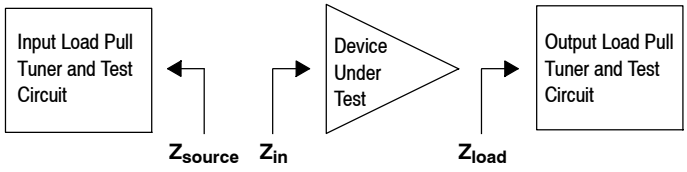
| | | | Max Drain Efficiency | | | | |
|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | $\eta_D$ (%) | AM/PM (°) |
| 1800 | 2.56 – j6.80 | 1.99 + j6.80 | 2.30 – j3.50 | 17.2 | 54.1 | 73.7 | –26 |
| 1880 | 2.80 – j6.90 | 2.80 + j7.60 | 2.40 – j4.20 | 17.5 | 54.1 | 70.3 | –26 |
| 1930 | 3.00 – j7.16 | 3.80 + j7.80 | 2.80 – j4.40 | 17.8 | 54.2 | 69.7 | –25 |
| 1990 | 4.50 – j7.10 | 4.90 + j7.50 | 2.40 – j4.60 | 17.9 | 54.1 | 70.7 | –27 |
| 2110 | 4.80 – j4.70 | 5.00 + j3.80 | 2.30 – j5.30 | 18.4 | 54.2 | 71.3 | –30 |
| 2200 | 4.20 – j3.00 | 2.60 + j3.30 | 2.60 – j6.10 | 18.5 | 54.5 | 68.8 | –28 |

(1) Load impedance for optimum P3dB efficiency.

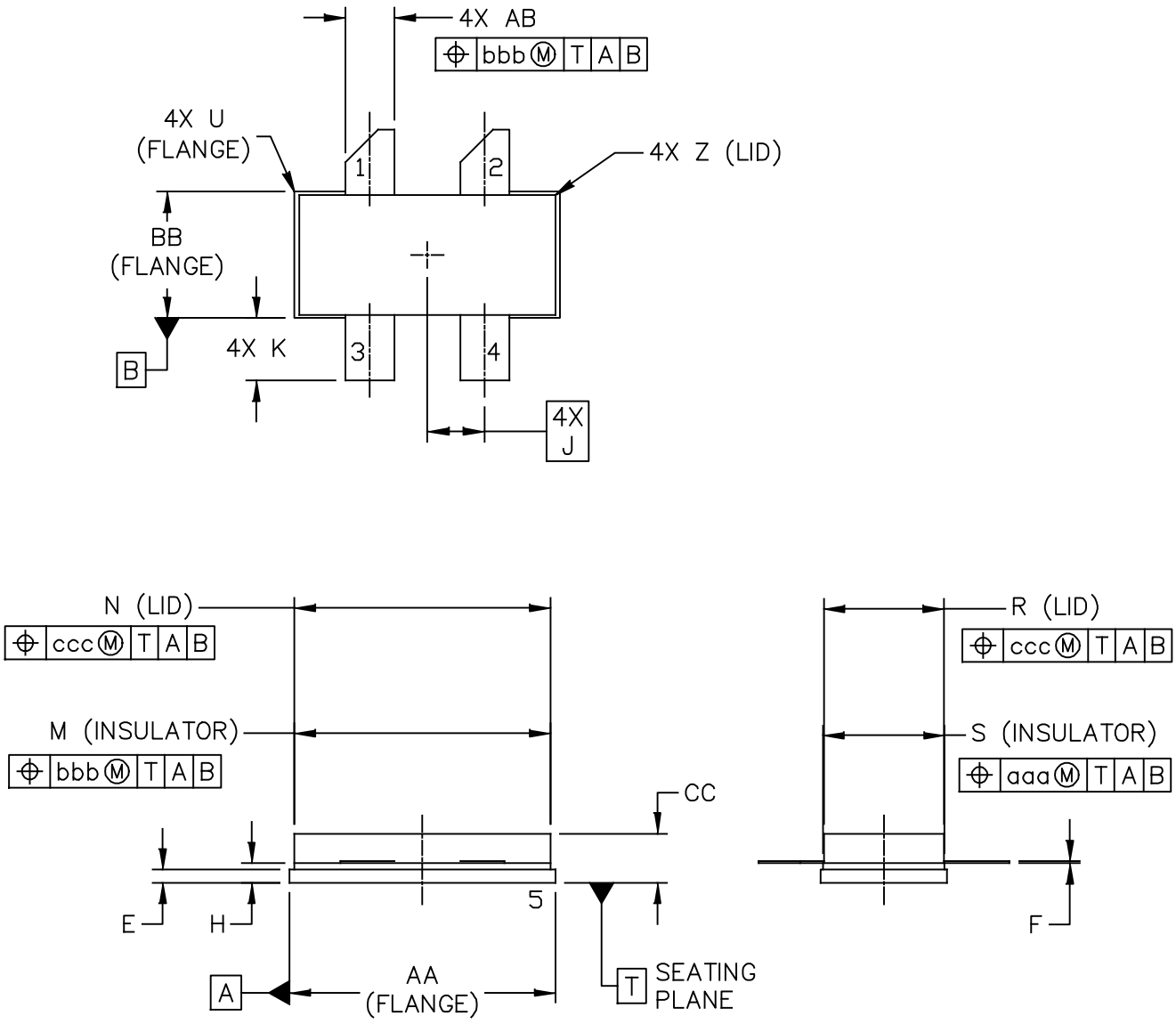
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$ = Impedance as measured from gate contact to ground.

$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



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| | SOT1826−1 | 01 AUG 2016 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM FLANGE TO CLEAR EPOXY FLOW OUT PARALLEL TO DATUM B.

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| AA | .805 | .815 | 20.45 | 20.70 | U | | .040 | | 1.02 |
| BB | .382 | .388 | 9.70 | 9.86 | Z | | .030 | | 0.76 |
| CC | .125 | .170 | 3.18 | 4.32 | AB | .145 | .155 | 3.68 – | 3.94 |
| E | .035 | .045 | 0.89 | 1.14 | | | | | |
| F | .003 | .006 | 0.08 | 0.15 | aaa | | .005 | | 0.127 |
| H | .057 | .067 | 1.45 | 1.70 | bbb | | .010 | | 0.254 |
| J | .175 BSC | | 4.44 BSC | | ccc | | .015 | | 0.381 |
| K | .170 | .210 | 4.32 | 5.33 | | | | | |
| M | .774 | .786 | 19.61 | 20.02 | | | | | |
| N | .772 | .788 | 19.61 | 20.02 | | | | | |
| R | .365 | .375 | 9.27 | 9.53 | | | | | |
| S | .365 | .375 | 9.27 | 9.52 | | | | | |

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## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

**Application Notes**

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Software**

- .s2p File

**Development Tools**

- Printed Circuit Boards

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | May 2017 | • Initial release of data sheet |
| 1 | Aug. 2020 | • Changed upper frequency range from 1880 MHz to 2200 MHz to highlight part performance up to 2200 MHz, p. 1<br>• Biasing sequence note: updated to reflect latest biasing sequence recommendations, p. 3<br>• Tables 11–14, Load Pull Performance: added Carrier Side and Peaking Side load pull performance tables showing P3dB performance across the 1800–2200 MHz band, pp. 13–14 |

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