A3G26D055N

Airfast RF Power GaN Amplifier

Rev. 3 — 18 October 2023 Product data sheet



1 General description

This 8 W symmetrical Doherty RF power GaN amplifier is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 100 to 2690 MHz.

This part is characterized and performance is guaranteed for applications operating in the 100 to 2690 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2 Features and benefits

- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity analog or digital linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

3 Typical performance

Table 1. 2600 MHz — Typical Doherty single-carrier W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQA} = 40 mA, V_{GSB} = –4.9 Vdc, P_{out} = 8 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2515 MHz	18.0	52.1	8.3	–27.4
2595 MHz	18.2	53.5	8.2	–28.2
2675 MHz	18.0	54.1	8.1	–30.1

[1] All data measured with device soldered to NXP reference circuit.

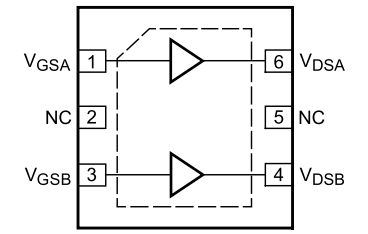
Table 2. 700 MHz — Typical Class AB Side A (top side) W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQA} = 40 mA, P_{out} = 5.6 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	P3dB (dBm)	ACPR (dBc)
750 MHz	20.0	41.7	7.0	44.5	–34.4
780 MHz	19.7	41.1	7.0	44.5	–34.3
810 MHz	19.2	40.6	7.0	44.5	–36.6

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information



(Top view)

Note: Exposed backside of the package is the source terminal for the device.

aaa-044825

Figure 1. Pin configuration

5 Ordering information

Table 3. Ordering information

Device	Tape and Reel Information	Package
A3G26D055NT4	T4 Suffix = 2,500 Units, 16 mm Tape Width, 13-inch Reel	DFN 7 × 6.5

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6 Product marking



Figure 2. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

7 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Gate-Source Voltage	V_{GS}	–8, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	10	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

8 Recommended operating conditions

Table 6. Recommended operating conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

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9 Thermal characteristics

Table 7. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 123°C, P_D = 8.3 W	$R_{\theta JC}$ (IR)	3.7[1]	°C/W
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature 95°C, P_D = 8.3 W	$R_{\theta CHC}$ (FEA)	8.5[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –11.1 and B = 8366.

10 ESD protection characteristics

Table 8. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1B
Charge Device Model (per JS-002-2014)	C3

11 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

12 Electrical characteristics

12.1 DC characteristics

12.1.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off characteristics[1]					
Off-State Drain Leakage	$I_{D(BR)}$				mAdc
(V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Carrier		—	—	3.0	
(V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Peaking		—	—	3.0	

[1] Each side of device measured separately.

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12.1.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
On characteristics — Side A, carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 3 mAdc)	$V_{GS(th)}$	–3.5	–2.7	–2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 40 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	–2.8	–2.5	–2.3	Vdc
Gate-Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –12 Vdc)	I_{GSS}	–3.0	—	—	mAdc
On characteristics — Side B, peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 3 mAdc)	$V_{GS(th)}$	–3.5	–2.7	–2.3	Vdc
Gate-Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –12 Vdc)	I_{GSS}	–3.0	—	—	mAdc

12.2 Functional tests

Table 12. Functional tests

(In NXP Doherty Production ATE[1] Test Fixture, T_A = 25°C unless otherwise noted, 50 ohm system)[2] V_{DD} = 48 Vdc, I_{DQA} = 40 mA, V_{GSB} = –5 Vdc, P_{out} = 5 W Avg., f = 2500 MHz, 1-tone CW.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	11.5	13.9	17.0	dB
Drain Efficiency	η_D	32.0	36.2	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	P_{sat}	37.5	40.0	—	dBm

[1] ATE is a socketed test environment.
[2] Internally matched part.

12.3 Wideband ruggedness

Table 13. Wideband ruggedness

(In NXP Doherty Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1] I_{DQA} = 40 mA, V_{GSB} = –5 Vdc, f = 2595 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Symbol	Min	Typ	Max	Unit
ISBW of 400 MHz at 55 Vdc, 17.4 W Avg. Modulated Output Power (3 dB Input Overdrive from 7.6 W Avg. Modulated Output Power)	No Device Degradation				

[1] All data measured with device soldered to NXP reference circuit.

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12.4 Typical performance

Table 14. Typical performance

(In NXP Doherty Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1] V_{DD} = 48 Vdc, I_{DQA} = 40 mA, V_{GSB} = –5 Vdc, 2515–2675 MHz Bandwidth.

Characteristic	Symbol	Min	Typ	Max	Unit
Fast CW, 27 ms sweep					
Saturated Power	P_{sat}	—	55	—	W
AM/PM (Maximum value measured at saturated power across the 2515–2675 MHz bandwidth)	Φ	—	–2.5	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (–40°C to +85°C)	ΔP_{sat}	—	0.010	—	dB/°C
Single-carrier W-CDMA, unclipped					
Gain Flatness in 160 MHz Bandwidth @ P_{out} = 8 W Avg.	G_F	—	0.8	—	dB
2-tone CW					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	200	—	MHz

[1] All data measured with device soldered to NXP reference circuit.

Correct biasing sequence for GaN depletion mode amplifiers in a Doherty configuration

Bias ON the device

1. Set gate voltage V_{GSA} and V_{GSB} to –5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to –5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.

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13 Package information

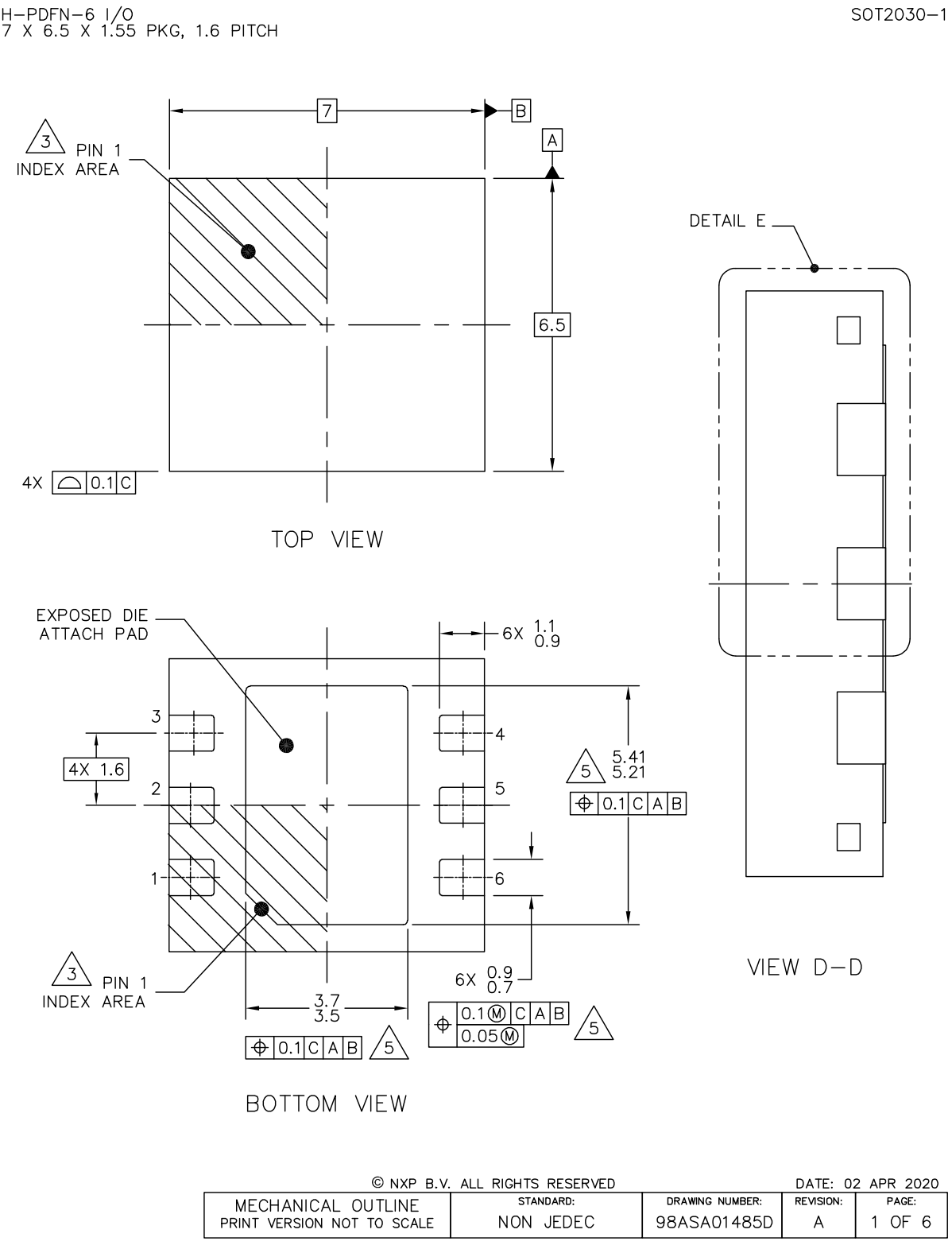


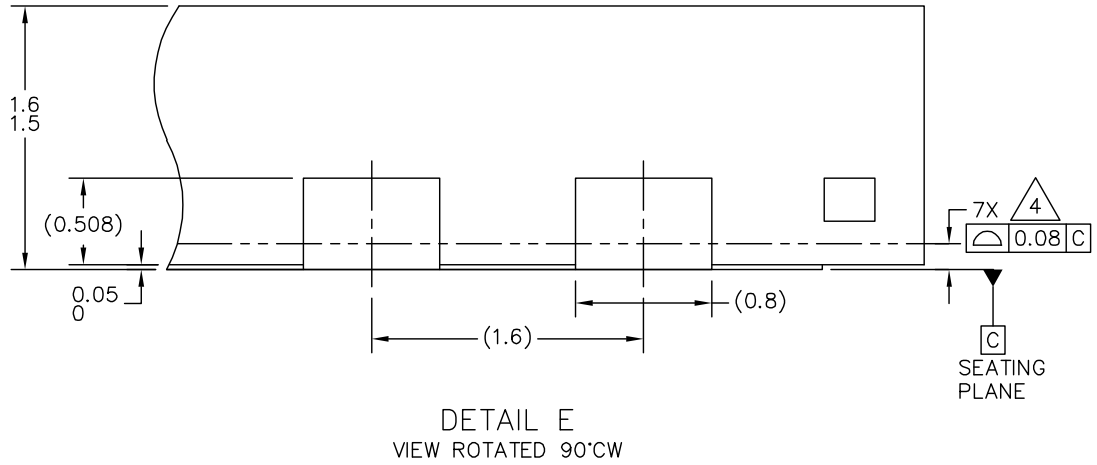
Figure 3. Package outline (DFN 7 mm × 6.5 mm) — top view, bottom view, detail E

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H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1



DETAIL E
VIEW ROTATED 90°CW

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Figure 4. Package outline (DFN 7 mm × 6.5 mm) — detail E, rotated

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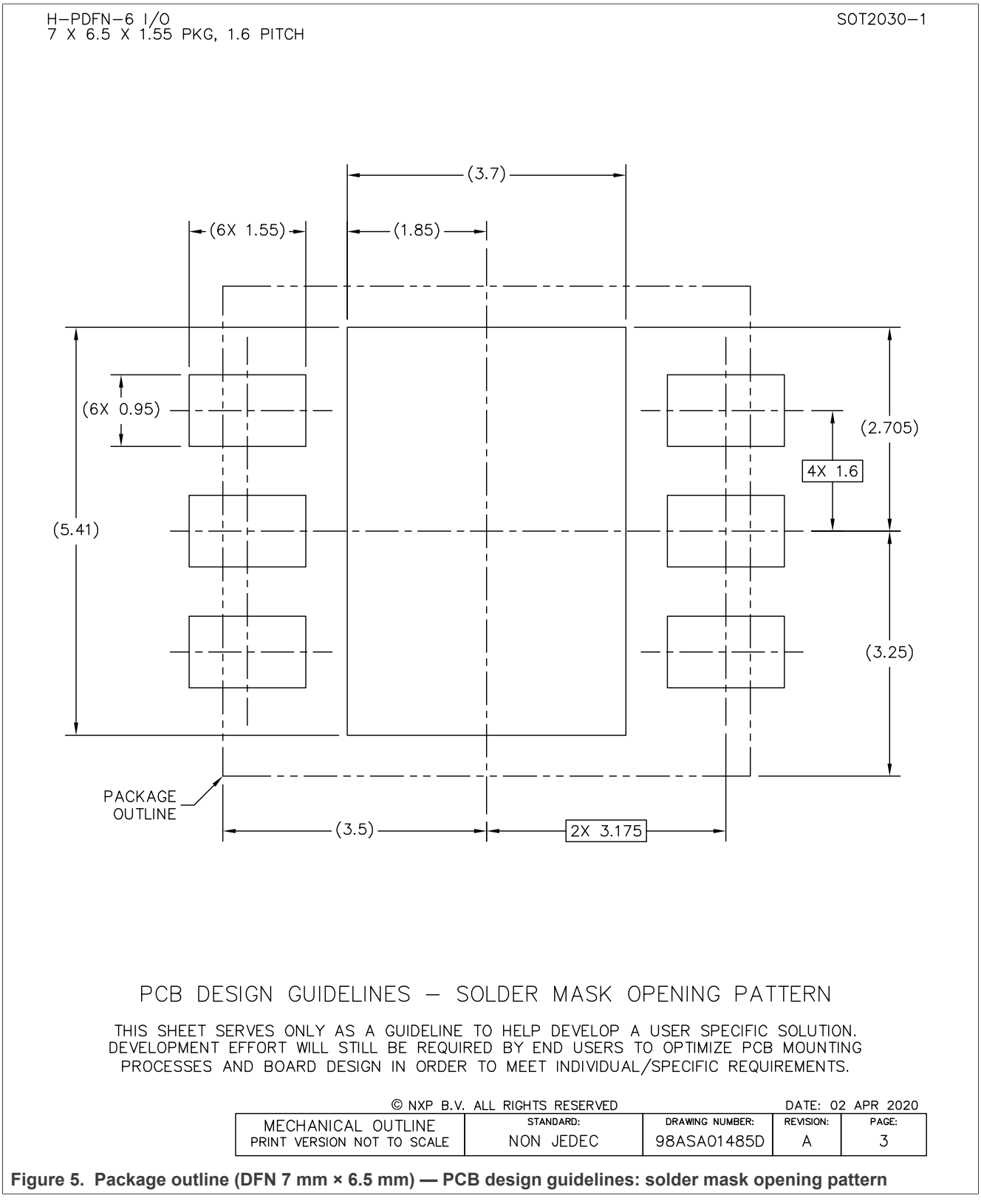


Figure 5. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: solder mask opening pattern

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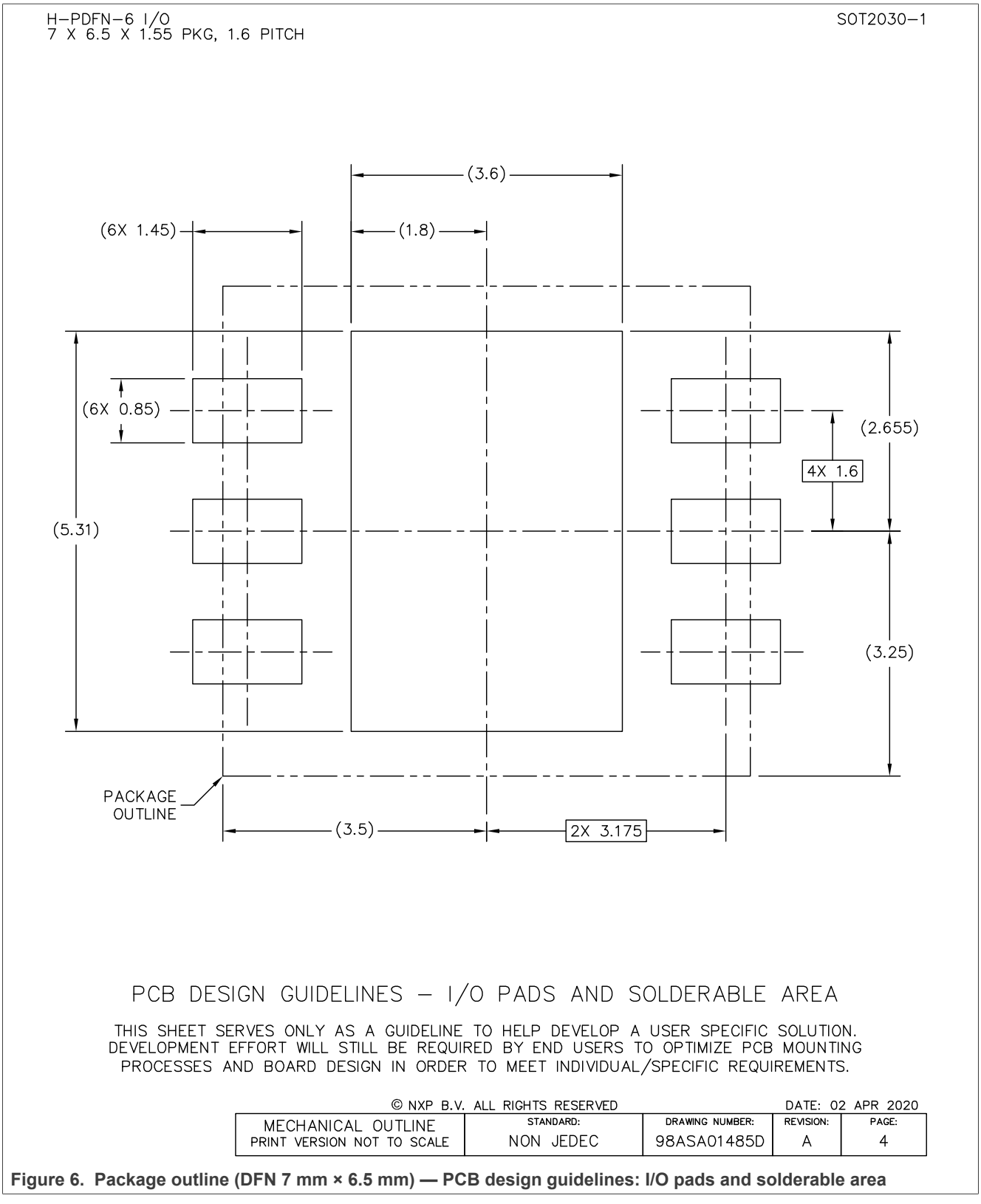


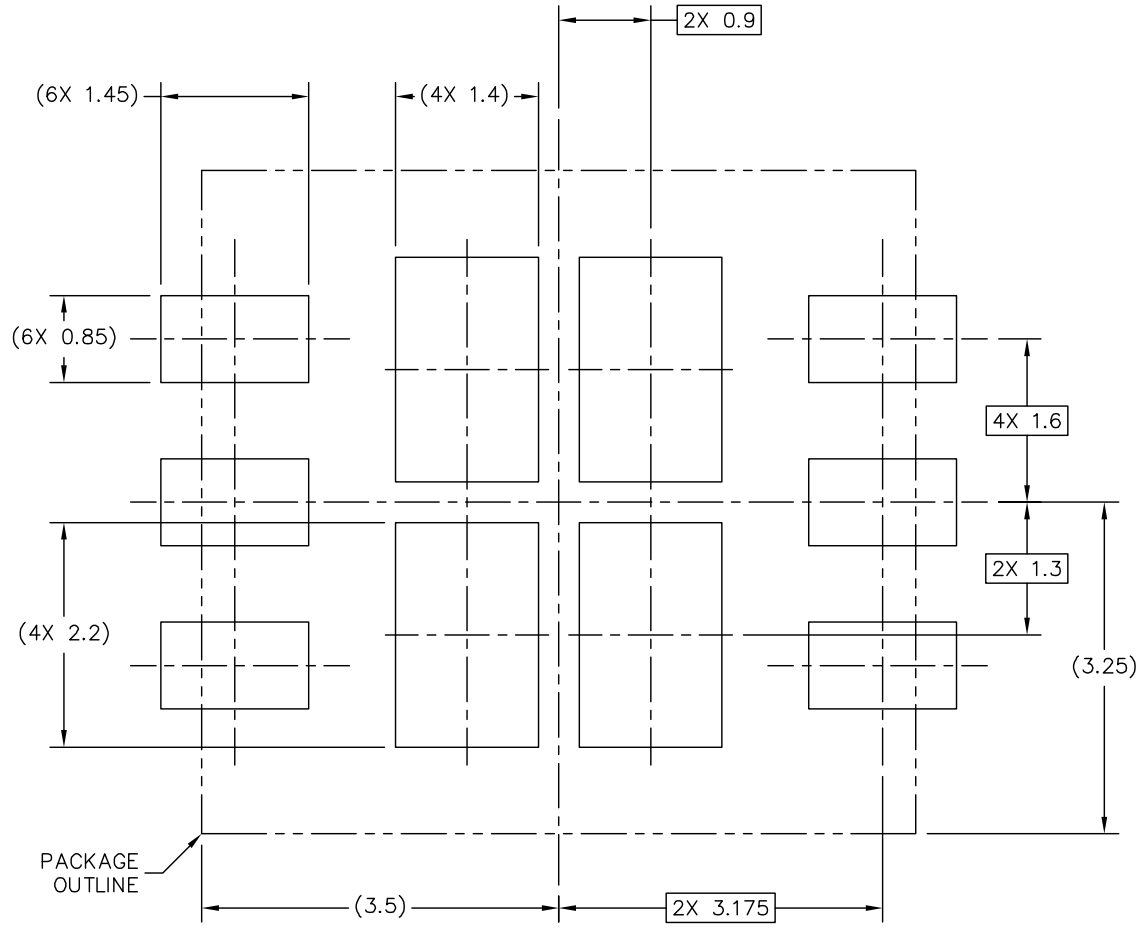
Figure 6. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: I/O pads and solderable area

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7 X 6.5 X 1.55 PKG, 1.6 PITCH

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STENCIL THICKNESS 0.125 OR 0.15

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Figure 7. Package outline (DFN 7 mm × 6.5 mm) — PCB design guidelines: solder paste stencil

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H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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NOTES:

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4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
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Figure 8. Package outline (DFN 7 mm × 6.5 mm) — notes

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14 Product documentation and software

Refer to the following resources to aid your design process.

Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

15 Revision history

The following table summarizes revisions to this document.

Table 15. Revision history

Revision	Date	Description
0	10 December 2020	• Initial release of data sheet
1	14 January 2021	• Table 1, Maximum Ratings: updated operating voltage for complete data sheet standardization, p. 2 • Table 2, Recommended Operating Conditions: added to data sheet, p. 2
2	1 March 2021	• Updated frequency band of operation for this device to 100–2690 MHz, p. 1
3	18 October 2023	• Figure 2, Product Marking: added, p. 3 • Table 4, Product Marking Trace Code: added, p. 3 • Table 12, Functional Tests: updated output power test condition, p. 5 • General updates made to align data sheet to current standard

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16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Document identifier: A3G26D055N

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