Document Number: A3T18H360W23S
Rev. 1, 06/2017

# RF Power LDMOS Transistor

## N–Channel Enhancement–Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1880 MHz.

**1800 MHz**

- Typical Doherty Single–Carrier W–CDMA Performance: $V_{DD}$ = 28 Vdc, $I_{DQA}$ = 700 mA, $V_{GSB}$ = 0.6 Vdc, $P_{out}$ = 63 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

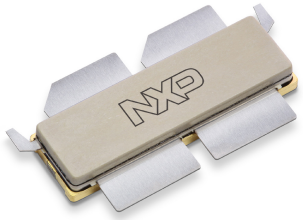
| Frequency | $G_{ps}$ (dB) | $\eta_D$ (%) | Output PAR (dB) | ACPR (dBc) |
|---|---|---|---|---|
| 1805 MHz | 16.3 | 52.8 | 7.7 | –30.3 |
| 1840 MHz | 16.6 | 52.3 | 7.6 | –31.7 |
| 1880 MHz | 16.6 | 51.6 | 7.5 | –32.8 |

**Features**

- Advanced high performance in–package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

**A3T18H360W23SR6**

**1805–1880 MHz, 63 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR**



**ACP–1230S–4L2S**

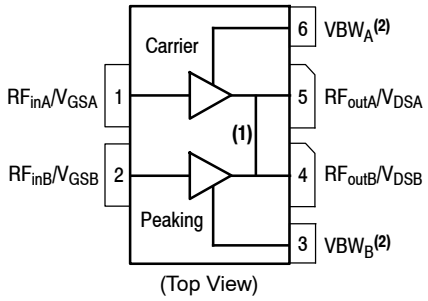



**Figure 1. Pin Connections**

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device can operate with $V_{DD}$ current supplied through pin 3 and pin 6.

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**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | –0.5, +65 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | –6.0, +10 | Vdc |
| Operating Voltage | $V_{DD}$ | 32, +0 | Vdc |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature Range | $T_C$ | –40 to +150 | °C |
| Operating Junction Temperature Range (1,2) | $T_J$ | –40 to +225 | °C |
| CW Operation @ $T_C$ = 25°C when DC current is fed through pin 3 and pin 6<br>Derate above 25°C | CW | 104<br>0.48 | W<br>W/°C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value (2,3) | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>Case Temperature 74°C, 63 W Avg., W-CDMA, 28 Vdc, $I_{DQA}$ = 700 mA, $V_{GSB}$ = 0.6 Vdc, 1840 MHz | $R_{\theta JC}$ | 0.22 | °C/W |

**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 2 |
| Charge Device Model (per JESD22-C101) | C3 |

**Table 4. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics (4)** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 65 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 32 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 5 | μAdc |
| Gate-Source Leakage Current ($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | μAdc |
| **On Characteristics - Side A, Carrier** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 120 μAdc) | $V_{GS(th)}$ | 1.4 | 1.8 | 2.3 | Vdc |
| Gate Quiescent Voltage ($V_{DD}$ = 28 Vdc, $I_{DA}$ = 700 mAdc, Measured in Functional Test) | $V_{GSA(Q)}$ | 2.3 | 2.7 | 3.1 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 1.2 Adc) | $V_{DS(on)}$ | 0.1 | 0.15 | 0.3 | Vdc |
| **On Characteristics - Side B, Peaking** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 240 μAdc) | $V_{GS(th)}$ | 0.8 | 1.2 | 1.6 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 2.4 Adc) | $V_{DS(on)}$ | 0.1 | 0.15 | 0.3 | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

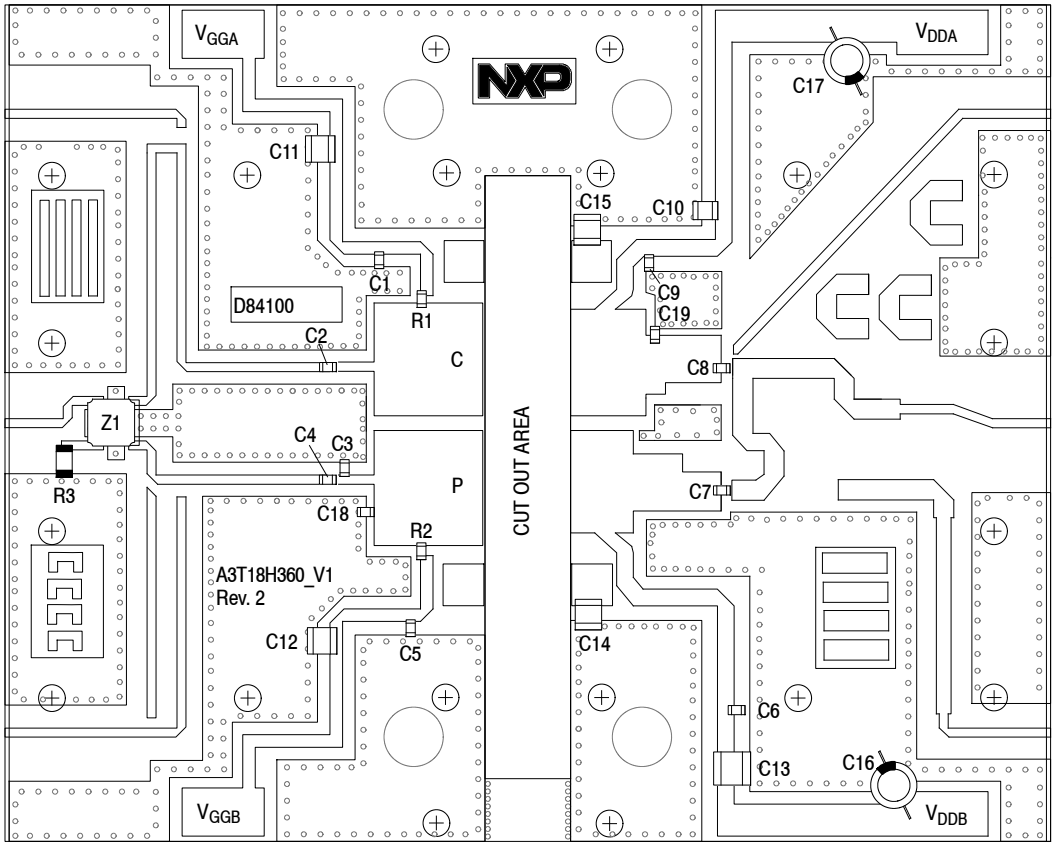
**Table 4. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Functional Tests** (1,2,3) (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQA}$ = 700 mA, $V_{GSB}$ = 0.6 Vdc, $P_{out}$ = 63 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. | | | | | |
| Power Gain | $G_{ps}$ | 16.0 | 16.6 | 19.0 | dB |
| Drain Efficiency | $\eta_D$ | 49.0 | 51.6 | — | % |
| $P_{out}$ @ 3 dB Compression Point, CW | P3dB | 54.0 | 54.7 | — | dBm |
| Adjacent Channel Power Ratio | ACPR | — | –32.8 | –29.0 | dBc |
| **Load Mismatch** (3) (In NXP Doherty Test Fixture, 50 ohm system) $I_{DQA}$ = 700 mA, $V_{GSB}$ = 0.6 Vdc, f = 1840 MHz, 12 μsec(on), 10% Duty Cycle | | | | | |
| VSWR 10:1 at 32 Vdc, 372 W Pulsed CW Output Power (3 dB Input Overdrive from 199 W Pulsed CW Rated Power) | No Device Degradation | | | | |
| **Typical Performance** (3) (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD}$ = 28 Vdc, $I_{DQA}$ = 700 mA, $V_{GSB}$ = 0.6 Vdc, 1805–1880 MHz Bandwidth | | | | | |
| $P_{out}$ @ 3 dB Compression Point (4) | P3dB | — | 375 | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth) | Φ | — | –23 | — | ° |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | 130 | — | MHz |
| Gain Flatness in 75 MHz Bandwidth @ $P_{out}$ = 63 W Avg. | $G_F$ | — | 0.3 | — | dB |
| Gain Variation over Temperature (–30°C to +85°C) | ΔG | — | 0.003 | — | dB/°C |
| Output Power Variation over Temperature (–30°C to +85°C) | ΔP1dB | — | 0.04 | — | dB/°C |

**Table 5. Ordering Information**

| Device | Tape and Reel Information | Package |
|---|---|---|
| A3T18H360W23SR6 | R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel | ACP-1230S-4L2S |

1. $V_{DDA}$ and $V_{DDB}$ must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = $P_{avg}$ + 7.0 dB where $P_{avg}$ is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.




Note: $V_{DDA}$ and $V_{DDB}$ must be tied together and powered by a single DC power supply.

**Figure 2. A3T18H360W23SR6 Test Circuit Component Layout**

**Table 6. A3T18H360W23SR6 Test Circuit Component Designations and Values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C5, C6, C9 | 20 pF Chip Capacitor | GQM2195C2E200GB12D | Murata |
| C2, C4 | 12 pF Chip Capacitor | GQM2195C2E120FB12D | Murata |
| C3, C18, C19 | 0.6 pF Chip Capacitor | GQM2195C2ER60BB12D | Murata |
| C7, C8 | 5 pF Chip Capacitor | GQM2195C2E5R0BB12D | Murata |
| C10 | 2.2 μF Chip Capacitor | HMK432B7225KM-T | Taiyo Yuden |
| C11, C12, C13, C14, C15 | 15 μF Chip Capacitor | C5750X7S2A156M230KB | TDK |
| C16, C17 | 220 μF, 100 V Electrolytic Capacitor | MCGPR100V227M16X26-RH | Multicomp |
| R1, R2 | 2.2 Ω, 1/8 W Chip Resistor | CRCW08052R20JNEA | Vishay |
| R3 | 50 Ω, 8 W Termination Chip Resistor | C8A50Z4A | Anaren |
| Z1 | 1700-2000 MHz Band, 90°, 5 dB Directional Coupler | X3C19P1-05S | Anaren |
| PCB | Rogers RO4350B, 0.020″, $\varepsilon_r$ = 3.66 | D84100 | MTL |

## TYPICAL CHARACTERISTICS — 1805–1880 MHz

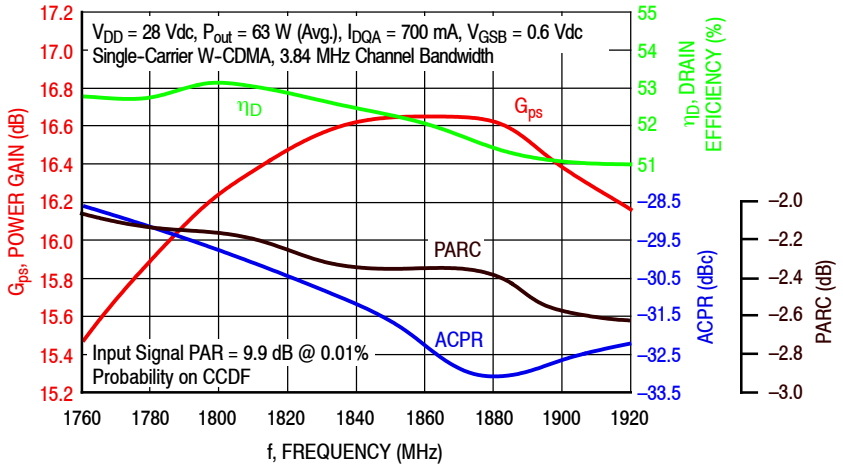



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out}$ = 63 Watts Avg.**

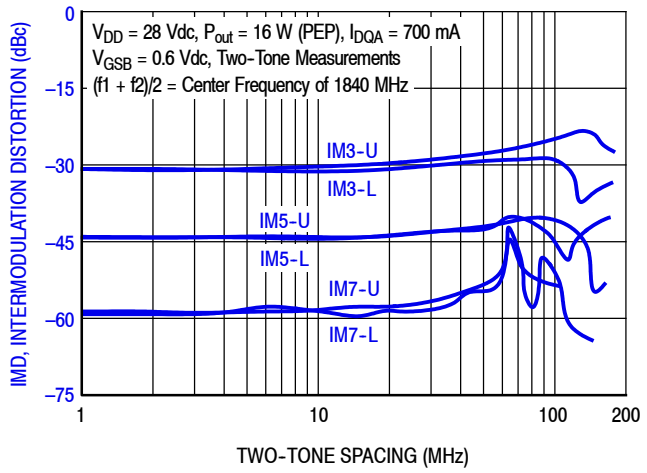



**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

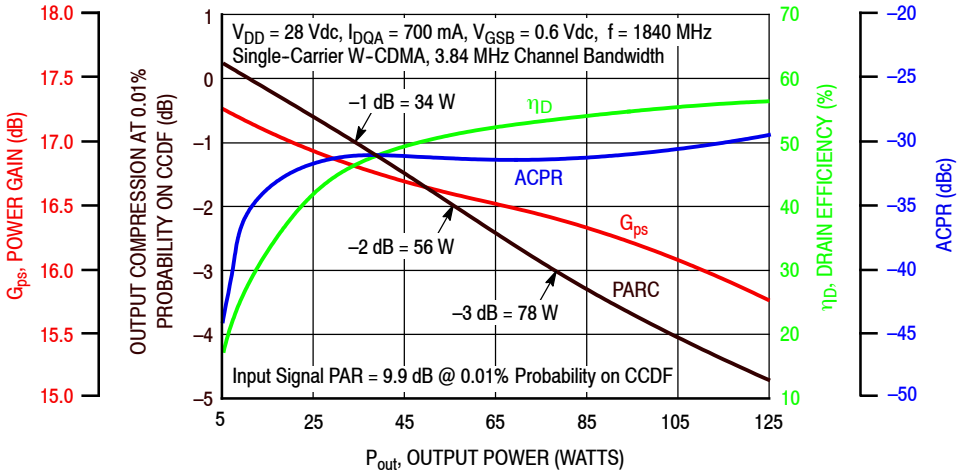



**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

## TYPICAL CHARACTERISTICS — 1805–1880 MHz

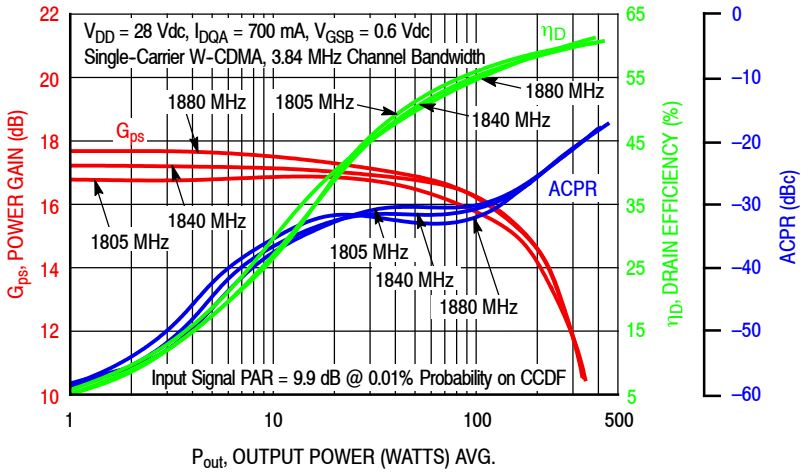



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

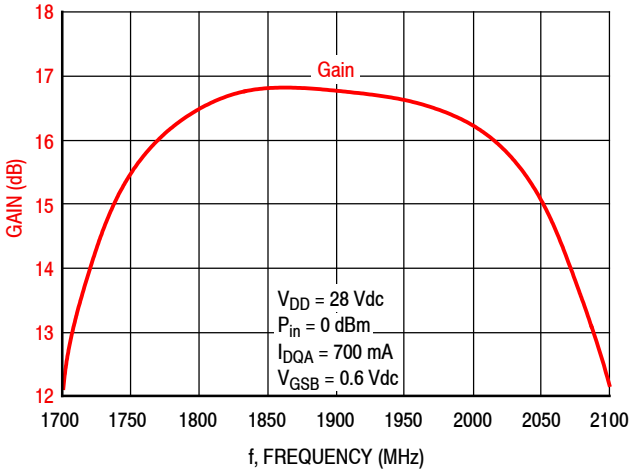



**Figure 7. Broadband Frequency Response**

**Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 28 Vdc, $I_{DQA}$ = 726 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 0.99 – j5.03 | 1.16 + j5.13 | 1.70 – j3.99 | 17.9 | 51.7 | 148 | 58.8 | –11 |
| 1840 | 1.08 – j5.40 | 1.33 + j5.44 | 1.63 – j4.13 | 17.7 | 51.7 | 148 | 57.7 | –12 |
| 1880 | 1.31 – j5.86 | 1.62 + j5.86 | 1.61 – j4.34 | 17.7 | 51.5 | 141 | 55.9 | –12 |

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 0.99 – j5.03 | 1.02 + j5.28 | 1.67 – j4.35 | 15.7 | 52.5 | 177 | 59.9 | –17 |
| 1840 | 1.08 – j5.40 | 1.18 + j5.64 | 1.65 – j4.43 | 15.6 | 52.4 | 175 | 59.2 | –18 |
| 1880 | 1.31 – j5.86 | 1.44 + j6.13 | 1.67 – j4.66 | 15.6 | 52.2 | 168 | 57.5 | –18 |

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

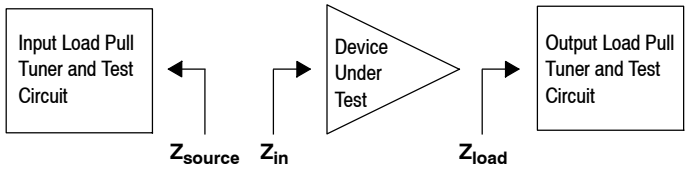
**Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 28 Vdc, $I_{DQA}$ = 726 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 0.99 – j5.03 | 1.07 + j5.07 | 3.12 – j2.79 | 20.2 | 50.2 | 105 | 67.6 | –14 |
| 1840 | 1.08 – j5.40 | 1.27 + j5.38 | 2.96 – j3.21 | 20.0 | 50.3 | 108 | 66.1 | –14 |
| 1880 | 1.31 – j5.86 | 1.50 + j5.77 | 2.44 – j2.83 | 19.7 | 50.1 | 101 | 63.2 | –15 |

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 0.99 – j5.03 | 0.94 + j5.23 | 3.49 – j2.86 | 18.5 | 50.8 | 120 | 70.6 | –23 |
| 1840 | 1.08 – j5.40 | 1.09 + j5.57 | 3.35 – j2.88 | 18.4 | 50.8 | 120 | 70.3 | –24 |
| 1880 | 1.31 – j5.86 | 1.31 + j6.04 | 3.22 – j2.88 | 18.4 | 50.7 | 117 | 69.1 | –23 |

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



## P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

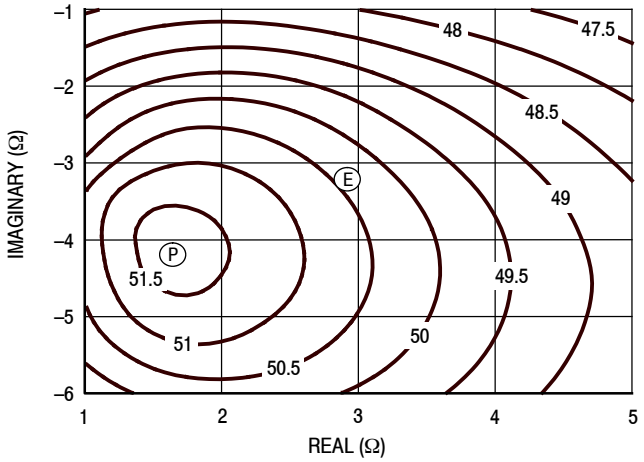



**Figure 8. P1dB Load Pull Output Power Contours (dBm)**

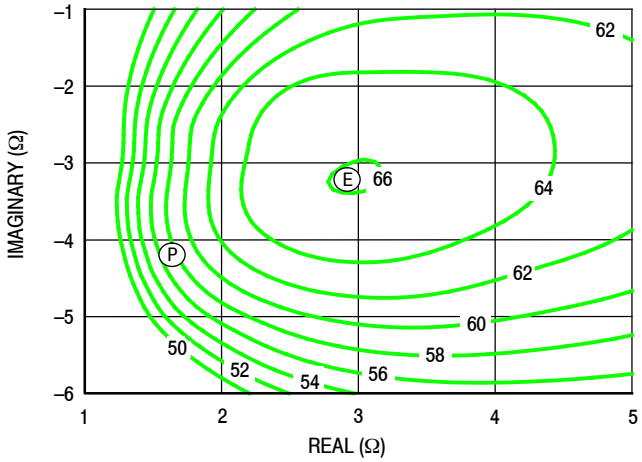



**Figure 9. P1dB Load Pull Efficiency Contours (%)**

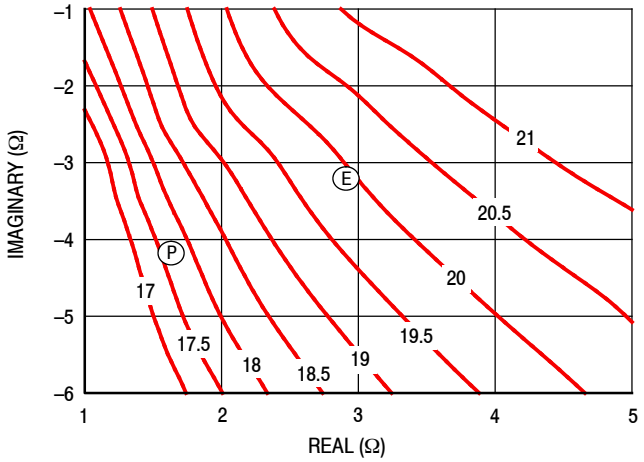



**Figure 10. P1dB Load Pull Gain Contours (dB)**

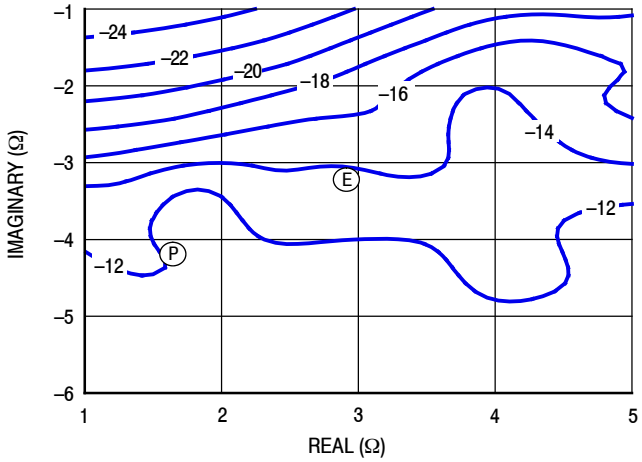



**Figure 11. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

## P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

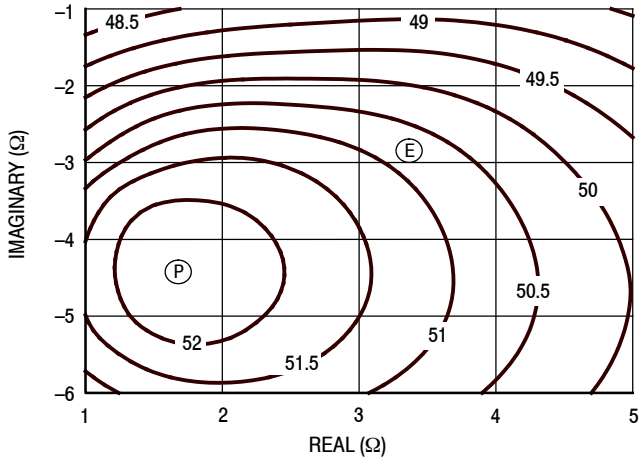



**Figure 12. P3dB Load Pull Output Power Contours (dBm)**

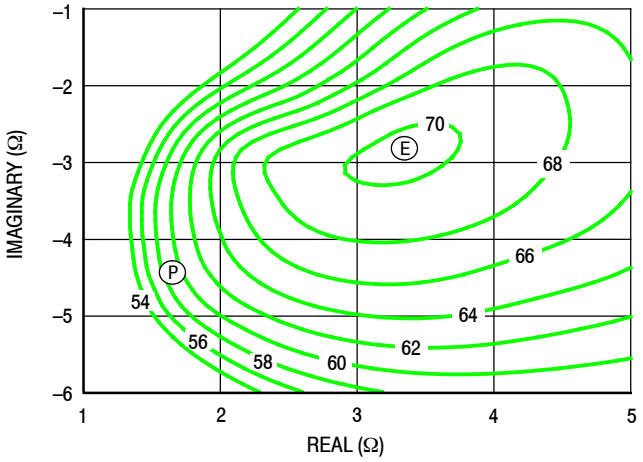



**Figure 13. P3dB Load Pull Efficiency Contours (%)**

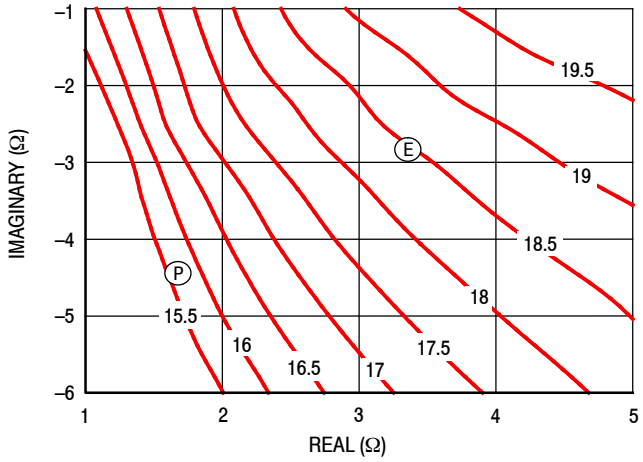



**Figure 14. P3dB Load Pull Gain Contours (dB)**

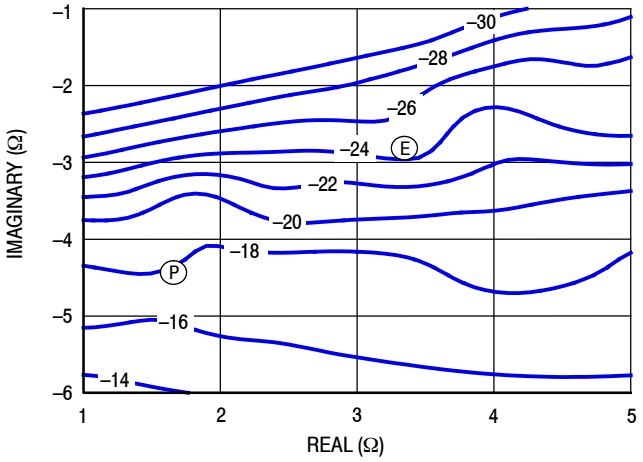



**Figure 15. P3dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

**Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning**

$V_{DD}$ = 28 Vdc, $V_{GSB}$ = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 1.11 – j4.67 | 1.06 + j4.94 | 2.06 – j4.24 | 15.6 | 54.9 | 310 | 58.8 | –31 |
| 1840 | 1.29 – j5.10 | 1.34 + j5.39 | 2.16 – j4.38 | 15.7 | 54.9 | 309 | 59.2 | –33 |
| 1880 | 1.74 – j5.74 | 1.81 + j6.07 | 2.23 – j4.45 | 15.8 | 54.9 | 308 | 59.4 | –34 |

| | | | Max Output Power | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 1.11 – j4.67 | 1.05 + j5.16 | 2.16 – j4.63 | 13.4 | 55.6 | 367 | 60.2 | –39 |
| 1840 | 1.29 – j5.10 | 1.35 + j5.68 | 2.23 – j4.65 | 13.5 | 55.7 | 369 | 60.9 | –41 |
| 1880 | 1.74 – j5.74 | 1.87 + j6.48 | 2.38 – j4.82 | 13.5 | 55.6 | 362 | 60.3 | –42 |

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.

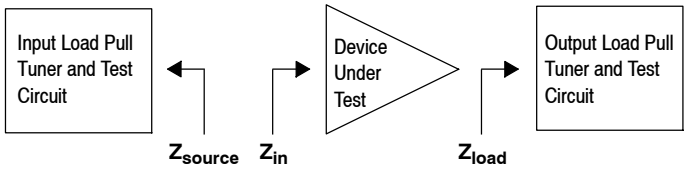
**Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD}$ = 28 Vdc, $V_{GSB}$ = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (1) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 1.11 – j4.67 | 0.89 + j4.82 | 4.60 – j1.84 | 17.1 | 53.0 | 199 | 71.0 | –35 |
| 1840 | 1.29 – j5.10 | 1.13 + j5.25 | 3.97 – j1.98 | 17.2 | 53.3 | 213 | 71.9 | –37 |
| 1880 | 1.74 – j5.74 | 1.54 + j5.89 | 3.49 – j2.09 | 17.1 | 53.4 | 217 | 71.9 | –38 |

| | | | Max Drain Efficiency | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P3dB | | | | | |
| f (MHz) | $Z_{source}$ (Ω) | $Z_{in}$ (Ω) | $Z_{load}$ (2) (Ω) | Gain (dB) | (dBm) | (W) | $\eta_D$ (%) | AM/PM (°) |
| 1805 | 1.11 – j4.67 | 0.93 + j5.09 | 4.75 – j2.97 | 14.9 | 54.1 | 258 | 69.7 | –43 |
| 1840 | 1.29 – j5.10 | 1.19 + j5.58 | 4.34 – j2.64 | 15.0 | 54.2 | 262 | 70.5 | –45 |
| 1880 | 1.74 – j5.74 | 1.65 + j6.34 | 4.06 – j2.49 | 14.9 | 54.1 | 258 | 70.1 | –47 |

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
$Z_{source}$ = Measured impedance presented to the input of the device at the package reference plane.
$Z_{in}$ = Impedance as measured from gate contact to ground.
$Z_{load}$ = Measured impedance presented to the output of the device at the package reference plane.



## P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

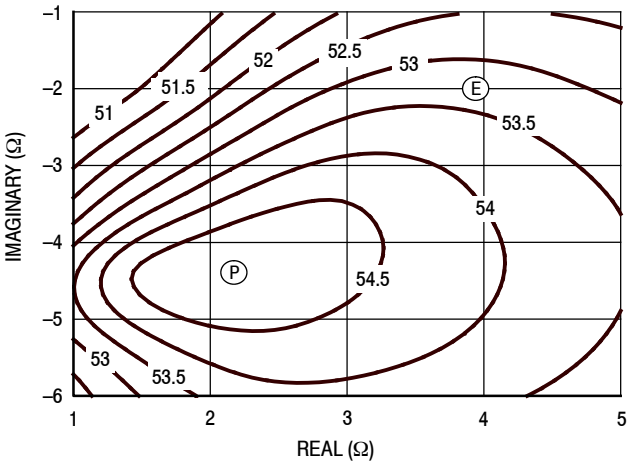



**Figure 16. P1dB Load Pull Output Power Contours (dBm)**

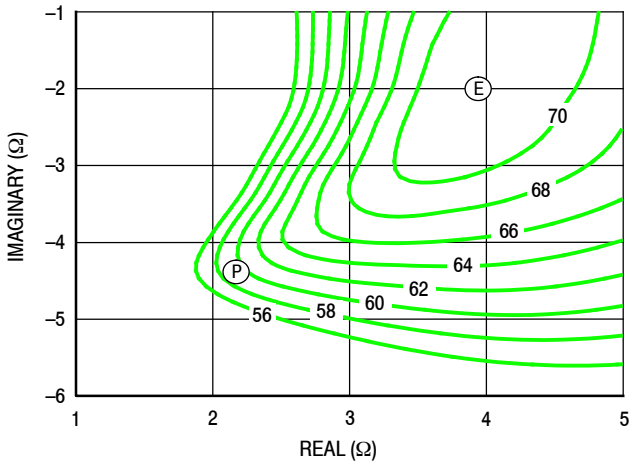



**Figure 17. P1dB Load Pull Efficiency Contours (%)**

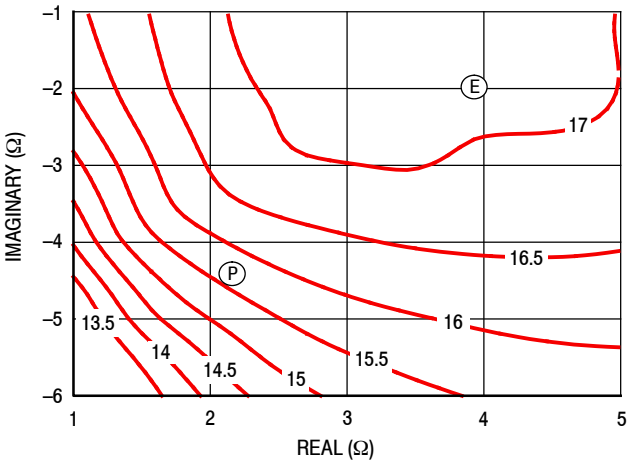



**Figure 18. P1dB Load Pull Gain Contours (dB)**

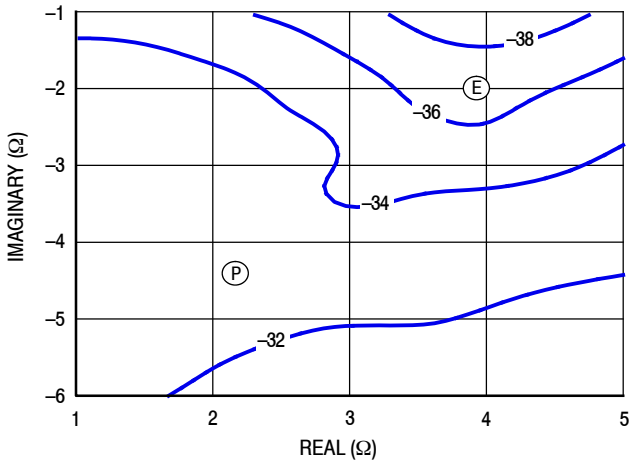



**Figure 19. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

## P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

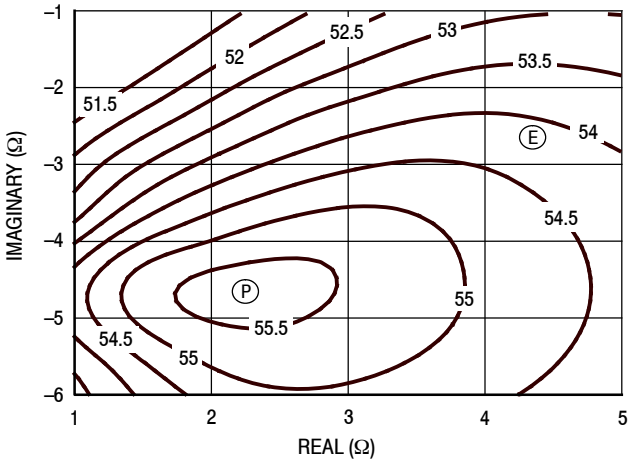



**Figure 20. P3dB Load Pull Output Power Contours (dBm)**

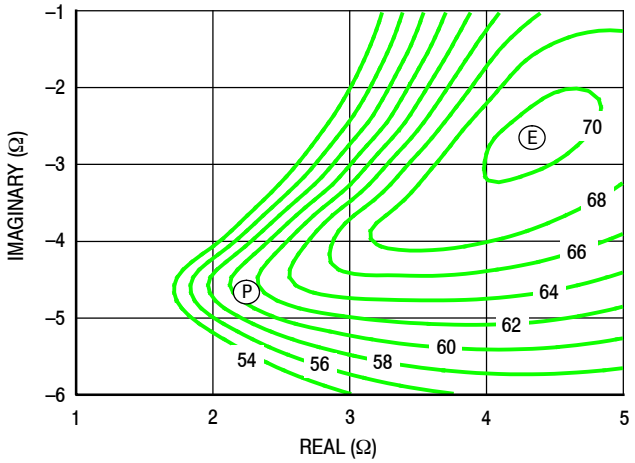



**Figure 21. P3dB Load Pull Efficiency Contours (%)**

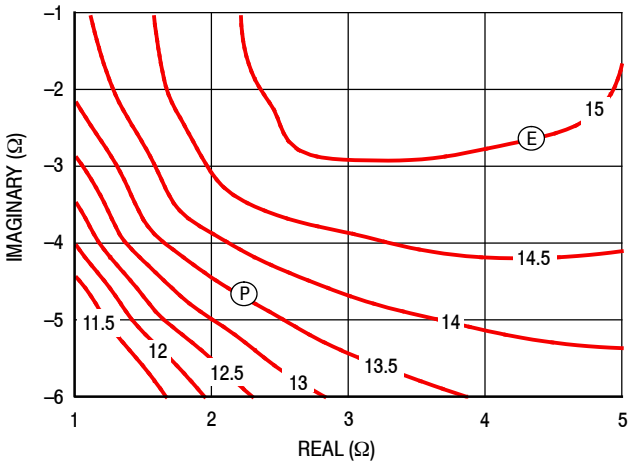



**Figure 22. P3dB Load Pull Gain Contours (dB)**

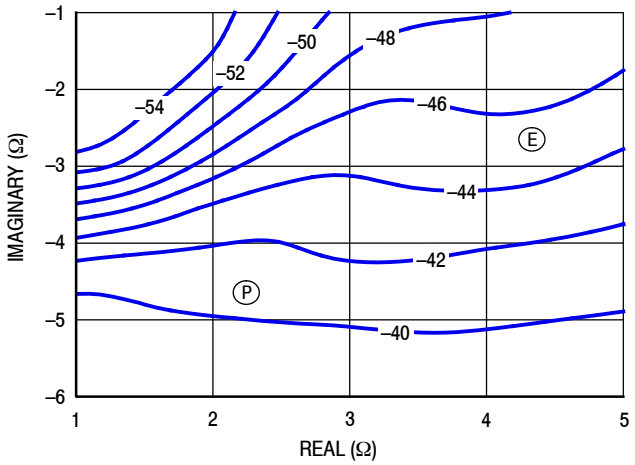



**Figure 23. P3dB Load Pull AM/PM Contours (°)**

**NOTE:** Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

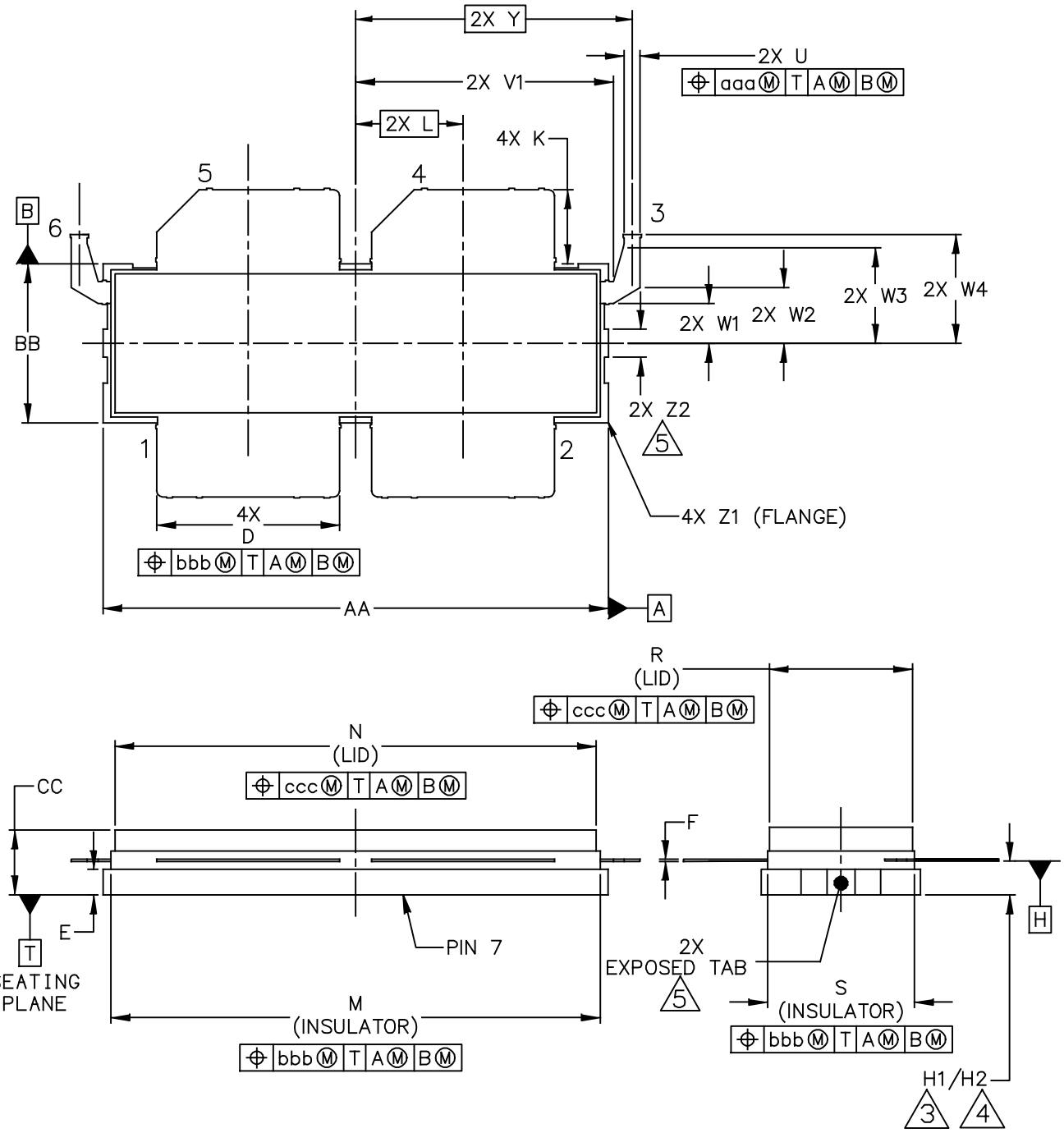
Gain

Drain Efficiency

Linearity

Output Power

## PACKAGE DIMENSIONS




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|---|---|---|
| TITLE: ACP–1230S–4L2S | DOCUMENT NO: 98ASA00974D | REV: A |
| | STANDARD: NON–JEDEC | |
| | SOT1800–4 | 21 JUN 2017 |

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.

7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. DATUM A AND B TO BE DETERMINED AT DATUM T.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|---|---|---|---|---|
| AA | 1.265 | 1.275 | 32.13 | 32.39 | S | .365 | .375 | 9.27 | 9.53 |
| BB | .395 | .405 | 10.03 | 10.29 | U | .035 | .045 | 0.89 | 1.14 |
| CC | .160 | .190 | 4.06 | 4.83 | V1 | .640 | .655 | 16.26 | 16.64 |
| D | .455 | .465 | 11.56 | 11.81 | W1 | .105 | .115 | 2.67 | 2.92 |
| E | .062 | .069 | 1.57 | 1.75 | W2 | .135 | .145 | 3.43 | 3.68 |
| F | .004 | .007 | 0.10 | 0.18 | W3 | .245 | .255 | 6.22 | 6.48 |
| H1 | .082 | .090 | 2.08 | 2.29 | W4 | .265 | .281 | 6.73 | 7.14 |
| H2 | .078 | .094 | 1.98 | 2.39 | Y | 0.695 BSC | | 17.65 BSC | |
| K | .175 | .195 | 4.45 | 4.95 | Z1 | R.000 | R.040 | R0.00 | R1.02 |
| L | 0.270 BSC | | 6.86 BSC | | Z2 | .060 | .100 | 1.52 | 2.54 |
| M | 1.219 | 1.241 | 30.96 | 31.52 | aaa | .015 | | 0.38 | |
| N | 1.218 | 1.242 | 30.94 | 31.55 | bbb | .010 | | 0.25 | |
| R | .365 | .375 | 9.27 | 9.53 | ccc | .020 | | 0.51 | |

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STANDARD: NON–JEDEC

SOT1800–4 21 JUN 2017

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

**Application Notes**

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**

- Electromigration MTTF Calculator
- .s2p File

**Development Tools**

- Printed Circuit Boards

**To Download Resources Specific to a Given Part Number:**

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | May 2017 | • Initial release of data sheet |
| 1 | June 2017 | • Table 6, Test Circuit Component Designations and Values: corrected C18 and C19 value and part number to 0.6 pF, GQM2195C2ER60BB12D, p. 4<br>• Package Outline: replaced 98ASA00974D, Rev. O with Rev. A, pp. 13, 14. Corrected dimension E. |

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