A5G26S004N

Airfast RF Power GaN Transistor

Rev. 5 — 18 October 2023 Product data sheet



1 General description

This 24 dBm RF power GaN transistor is designed for cellular base station applications covering the frequency range of 2300 to 2690 MHz.

2 Features and benefits

- High terminal impedances for optimal broadband performance
- Designed for low complexity linearization systems
- Universal broadband driver
- Optimized for massive MIMO active antenna systems for 5G base stations

3 Typical performance

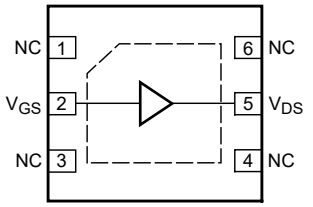
Table 1. 2600 MHz — Typical single-carrier W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQ} = 10 mA, P_{out} = 24 dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2515 MHz	18.7	18.8	10.2	–39.6
2595 MHz	19.6	20.5	9.8	–42.0
2675 MHz	18.9	20.6	9.7	–44.7

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information



(Top view)

Note: Exposed backside of the package is the source terminal for the transistor.

aaa-042956

Figure 1. Pin configuration

5 Ordering information

Table 2. Ordering information

Device	Tape and Reel Information	Package
A5G26S004NT6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	DFN 4.5 × 4

6 Product marking



aaa-044549

Figure 2. Product marking

Table 3. Product marking trace code

Identifier	Description
A	Assembly location
L	Wafer lot indicator
YW	Date code
Z	Assembly lot

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7 Limiting values

Table 4. Limiting values

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Gate-Source Voltage	V_{GS}	–16, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current @ T_C = 25°C	I_{GMAX}	0.74	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

8 Recommended operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

9 Thermal characteristics

Table 6. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 115°C, P_D = 1.1 W	$R_{\theta JC}$ (IR)	9.5[1]	°C/W
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature 115°C, P_D = 1.1 W	$R_{\theta CHC}$ (FEA)	32[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = –11.1 and *B* = 8366.

10 ESD protection characteristics

Table 7. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1A
Charge Device Model (per JS-002-2014)	C3

11 Moisture sensitivity level

Table 8. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

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12 Electrical characteristics

12.1 DC characteristics

12.1.1 DC characteristics — off characteristics

Table 9. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off characteristics					
Off-State Drain Leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	0.74	mAdc

12.1.2 DC characteristics — on characteristics

Table 10. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
On characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 0.74 mAdc)	$V_{GS(th)}$	–4.9	–2.6	–1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 10 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	–2.9	–2.5	–2.0	Vdc
Gate-Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –12 Vdc)	I_{GSS}	–0.74	—	—	mAdc

12.2 Functional tests

Table 11. Functional tests

(In NXP Production ATE[1] Test Fixture, T_A = 25°C unless otherwise noted, 50 ohm system)[2] V_{DD} = 48 Vdc, I_{DQ} = 10 mA, P_{out} = 24 dBm Avg., f = 2690 MHz, 1-tone CW.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	18.0	20.9	24.0	dB
Drain Efficiency	η_D	20.0	22.4	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	P_{sat}	35.0	37.4	—	dBm

[1] ATE is a socketed test environment.
[2] Internally matched part.

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12.3 Wideband ruggedness

Table 12. Wideband ruggedness

(In NXP Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1] I_{DQ} = 10 mA, f = 2595 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Symbol	Min	Typ	Max	Unit
ISBW of 400 MHz at 55 Vdc, 0.64 W Avg. Modulated Output Power (3 dB Input Overdrive from 0.3 W Avg. Modulated Output Power)	No Device Degradation				

[1] All data measured with device soldered to NXP reference circuit.

12.4 Typical performance

Table 13. Typical performance

(In NXP Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1] V_{DD} = 48 Vdc, I_{DQ} = 10 mA, 2515–2675 MHz Bandwidth.

Characteristic	Symbol	Min	Typ	Max	Unit
Fast CW, 27 ms sweep					
Saturated Power	P_{sat}	—	4.0	—	W
AM/PM (Maximum value measured at saturated power across the 2515–2675 MHz bandwidth)	Φ	—	–16	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (–40°C to +85°C)	ΔP_{sat}	—	0.002	—	dB/°C
Single-carrier W-CDMA, unclipped					
Gain Flatness in 160 MHz Bandwidth @ P_{out} = 24 dBm Avg.	G_F	—	0.9	—	dB
2-tone CW					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	250	—	MHz

[1] All data measured with device soldered to NXP reference circuit.

Correct biasing sequence for GaN depletion mode transistors

Turning the device ON

1. Set V_{GS} to the pinch-off voltage, typically –5 V.
2. Turn on V_{DS} to nominal supply voltage (+48 V).
3. Increase V_{GS} until I_{DS} current is attained.
4. Apply RF input power to desired level.

Turning the device OFF

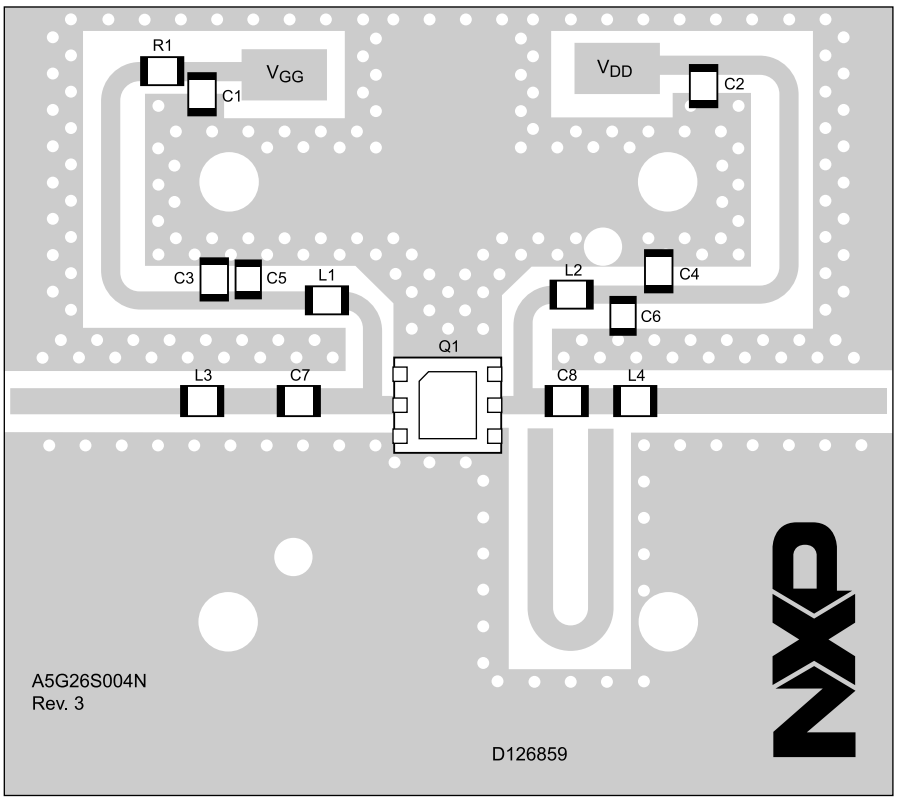
1. Turn RF power off.
2. Reduce V_{GS} down to the pinch-off voltage, typically –5 V.
3. Adjust drain voltage V_{DS} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Turn off V_{GS}.

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13 Component layout and parts list

13.1 Component layout



Note: All data measured with device soldered to NXP reference circuit.

aaa-039741

Figure 3. A5G26S004N reference circuit component layout

13.2 Component designations and values

Table 14. A5G26S004N reference circuit component designations and values

Part	Description	Part Number	Manufacturer
C1, C2	2.2 µF Chip Capacitor	GRM32ER72A225KA35L	Murata
C3, C4	1 µF Chip Capacitor	GRM31MR71H105KA88L	Murata
C5, C6, C7, C8	8.2 pF Chip Capacitor	GQM2195C2E8R2BB12D	Murata
L1	3.9 nH Chip Inductor	0603HP-3N9XJLW	Coilcraft
L2, L3	1.6 nH Chip Inductor	0603HP-1N6XJLW	Coilcraft
L4	4.7 nH Chip Inductor	0603HP-4N7XJLW	Coilcraft
Q1	RF Power GaN Transistor	A5G26S004N	NXP
R1	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D126859	MTL

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14 Package information

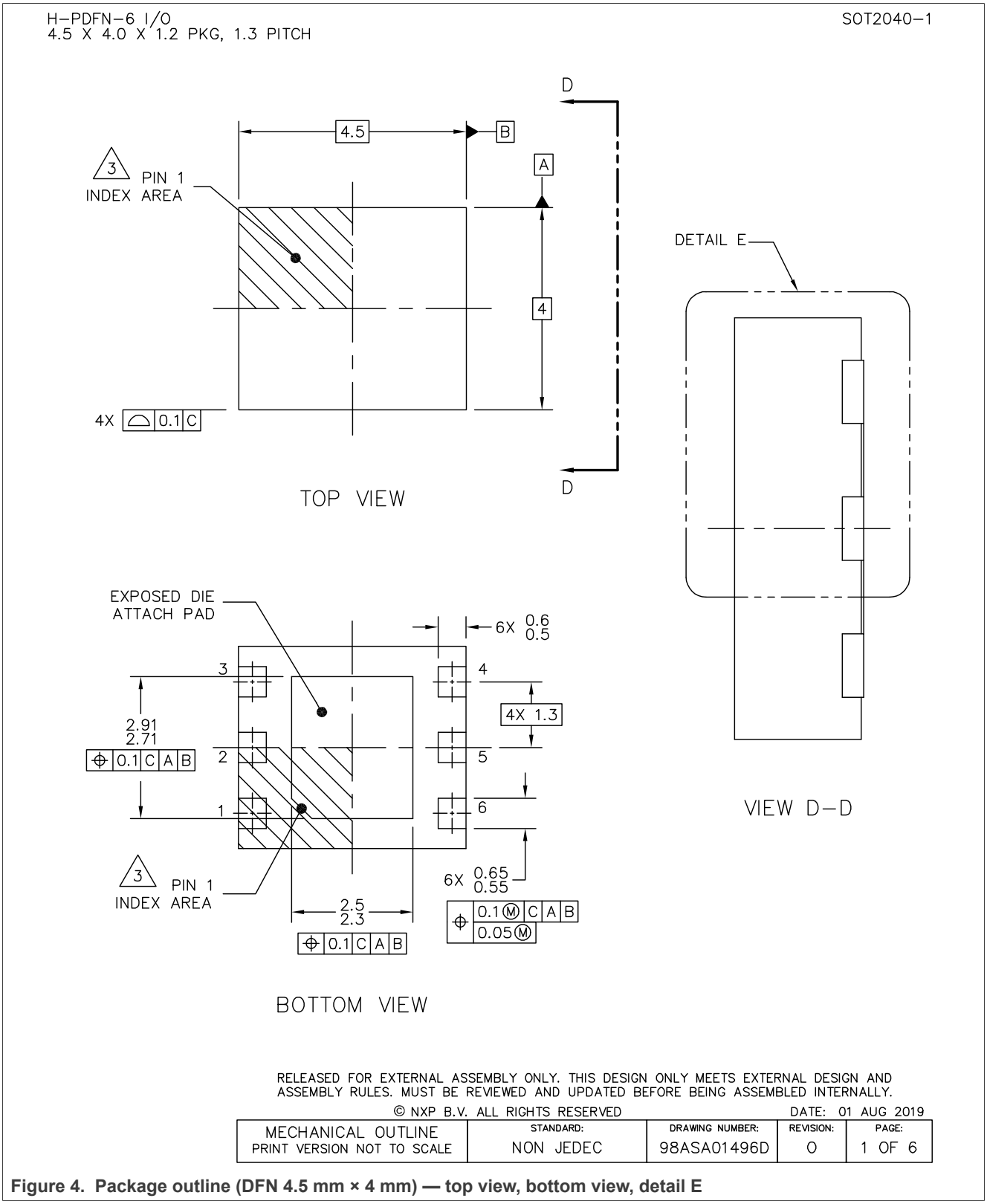


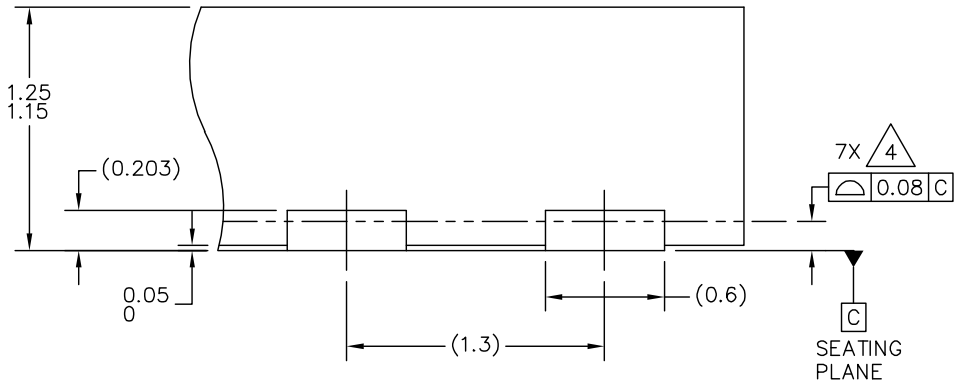
Figure 4. Package outline (DFN 4.5 mm × 4 mm) — top view, bottom view, detail E

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H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



DETAIL E
VIEW ROTATED 90°CW

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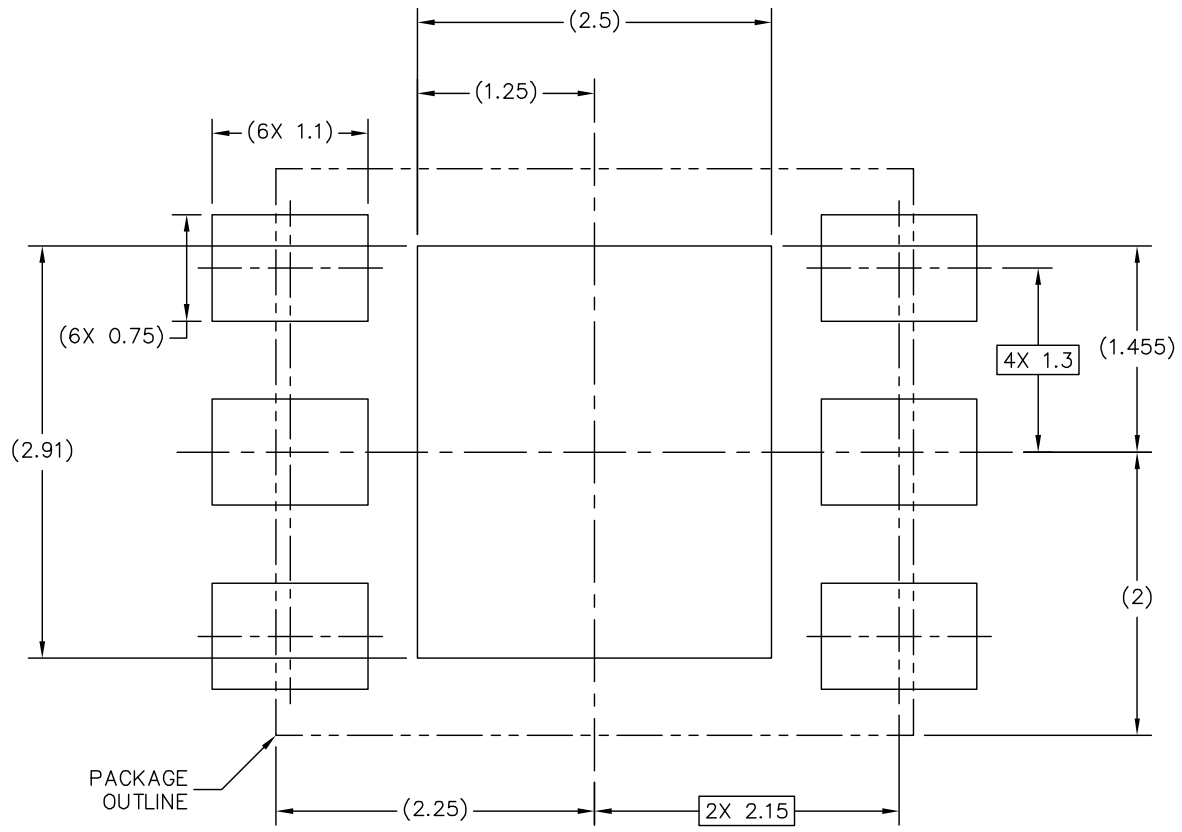
Figure 5. Package outline (DFN 4.5 mm × 4 mm) — detail E, rotated

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4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

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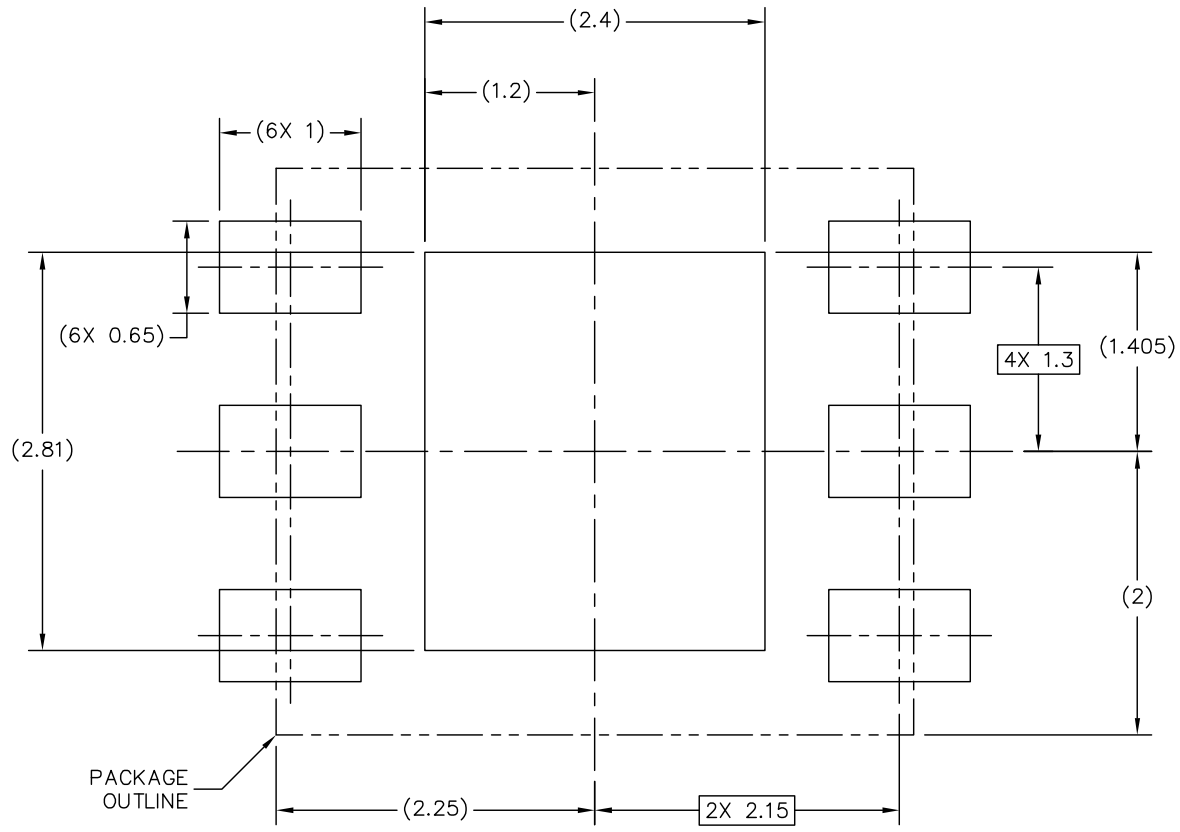
Figure 6. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: solder mask opening pattern

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Figure 7. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: I/O pads and solderable area

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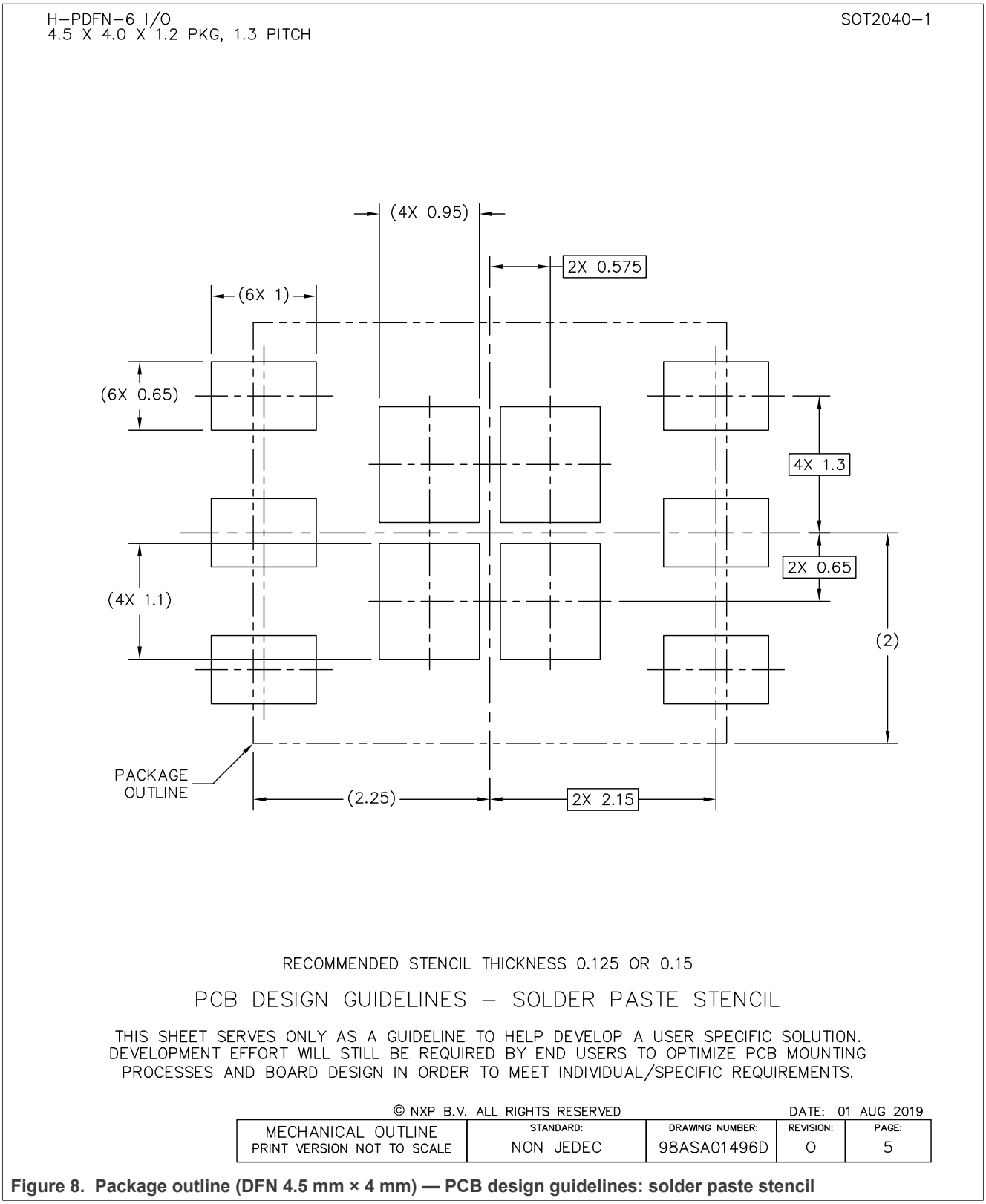


Figure 8. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: solder paste stencil

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4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
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Figure 9. Package outline (DFN 4.5 mm × 4 mm) — notes

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15 Product documentation, software and tools

Refer to the following resources to aid your design process.

Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development tools

- Printed Circuit Boards

16 Revision history

The following table summarizes revisions to this document.

Table 15. Revision history

Revision	Date	Description
0	15 December 2020	• Initial release of data sheet
1	15 January 2021	• Table 1, Maximum Ratings: updated operating voltage for complete data sheet standardization, p. 2 • Table 2, Recommended Operating Conditions: added to data sheet, p. 2
2	21 January 2022	• Table 6, DC On Characteristics, $V_{GS(th)}$: Min, Typ and Max values updated to match production test values, p. 2
3	30 November 2022	• Table 1, Maximum Ratings: Gate-Source Voltage: updated –8, 0 to –16, 0 Vdc, p. 2 • Table 4, ESD Protection Characteristics, Human Body Model: updated to reflect test data, p. 2 • General updates made to align data sheet to current standard
4	17 April 2023	• Updated frequency band of operation for this device to 2300–2690 MHz, p. 1 • Table 9, Product Marking Trace Code: added, p. 5 • General updates made to align data sheet to current standard
5	18 October 2023	• Table 11, Functional Tests: updated output power test condition, p. 4 • General updates made to align data sheet to current standard

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Date of release: 18 October 2023
Document identifier: A5G26S004N

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Parça koduyla arama

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www.entegreci.com

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

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