ALPHA & OMEGA SEMICONDUCTOR

AOT27S60L/AOB27S60L/AOTF27S60L/AOTF27S60

600V 27A αMOS™ Power Transistor

General Description

The AOT27S60L & AOB27S60L & AOTF27S60L & AOTF27S60 have been fabricated using the advanced αMOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications.
By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS} @ $T_{j,max}$	700V
I_{DM}	110A
$R_{DS(ON),max}$	0.16Ω
$Q_{g,typ}$	26nC
E_{oss} @ 400V	6µJ

100% UIS Tested
100% R_g Tested

RoHS Compliant

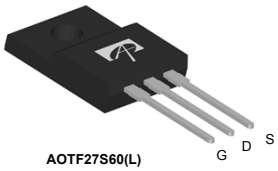
Top View

TO-220



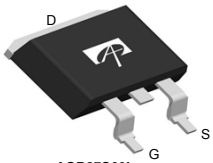
AOT27S60L

TO-220F(3kVAC;1s)

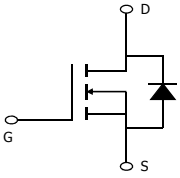


AOTF27S60(L)

TO-263
D²PAK



AOB27S60L



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	AOT27S60L/AOB27S60L	AOTF27S60	AOTF27S60L	Units
Drain-Source Voltage		V_{DS}	600			V
Gate-Source Voltage		V_{GS}	±30			V
Continuous Drain Current	T_C=25°C	I_D	27	27*	27*	A
	T_C=100°C		17	17*	17*	
Pulsed Drain Current [C]		I_{DM}	110			
Avalanche Current [C]		I_{AR}	7.5			A
Repetitive avalanche energy [C]		E_{AR}	110			mJ
Single pulsed avalanche energy [G]		E_{AS}	480			mJ
Power Dissipation [B]	T_C=25°C	P_D	357	50	40	W
	Derate above 25°C		2.9	0.4	0.3	W/ °C
MOSFET dv/dt ruggedness		dv/dt	100			V/ns
Peak diode recovery dv/dt [H]			20			
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150			°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds [J]		T_L	300			°C

Thermal Characteristics

Parameter	Symbol	AOT27S60L/AOB27S60L	AOTF27S60	AOTF27S60L	Units
Maximum Junction-to-Ambient [A,D]	$R_{\theta JA}$	65	65	65	°C/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	0.5	--	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.35	2.5	3.1	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C	600	-	-	V
		I_D=250µA, V_{GS}=0V, T_J=150°C	650	700	-	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=600V, V_{GS}=0V	-	-	1	µA
		V_{DS}=480V, T_J=150°C	-	10	-	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=5V,I_D=250µA	2.5	3.3	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=13.5A, T_J=25°C	-	0.14	0.16	Ω
		V_{GS}=10V, I_D=13.5A, T_J=150°C	-	0.38	0.44	Ω
V_{SD}	Diode Forward Voltage	I_S=13.5A,V_{GS}=0V, T_J=25°C	-	0.85	-	V
I_S	Maximum Body-Diode Continuous Current		-	-	27	A
I_{SM}	Maximum Body-Diode Pulsed Current		-	-	110	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	-	1294	-	pF
C_{oss}	Output Capacitance		-	80	-	pF
$C_{o(er)}$	Effective output capacitance, energy related [H]	V_{GS}=0V, V_{DS}=0 to 480V, f=1MHz	-	69	-	pF
$C_{o(tr)}$	Effective output capacitance, time related [I]		-	221	-	pF
C_{rss}	Reverse Transfer Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	-	2.3	-	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.4	4.7	6.7	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=480V, I_D=13.5A	-	26	-	nC
Q_{gs}	Gate Source Charge		-	6.2	-	nC
Q_{gd}	Gate Drain Charge		-	8.8	-	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=400V, I_D=13.5A, R_G=25Ω	-	31	-	ns
t_r	Turn-On Rise Time		-	33	-	ns
$t_{D(off)}$	Turn-Off DelayTime		-	99	-	ns
t_f	Turn-Off Fall Time		-	34	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=13.5A,dI/dt=100A/µs,V_{DS}=400V	-	440	-	ns
I_{rm}	Peak Reverse Recovery Current	I_F=13.5A,dI/dt=100A/µs,V_{DS}=400V	-	28	-	A
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=13.5A,dI/dt=100A/µs,V_{DS}=400V	-	7.5	-	µC

A. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A=25° C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C, Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. L=60mH, I_{AS}=4A, V_{DD}=150V, Starting T_J=25° C
H. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.
I. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.
J. Wavesoldering only allowed at leads.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

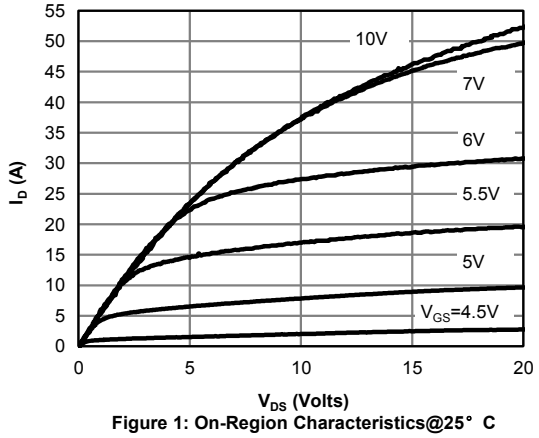


Figure 1: On-Region Characteristics@25° C

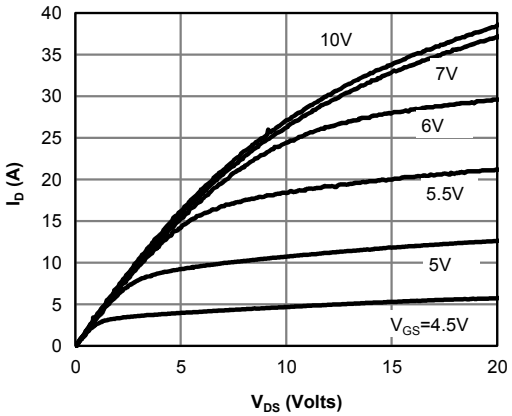


Figure 2: On-Region Characteristics@125° C

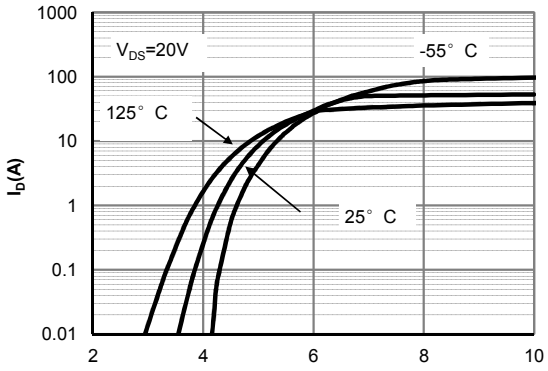


Figure 3: Transfer Characteristics

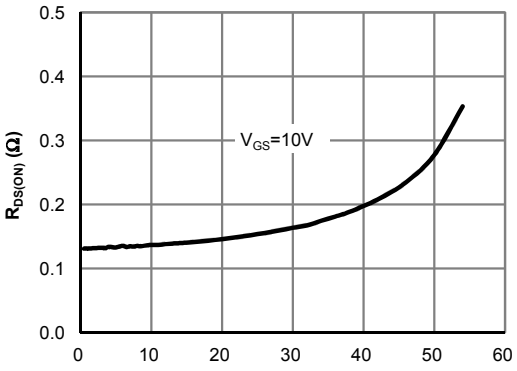


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

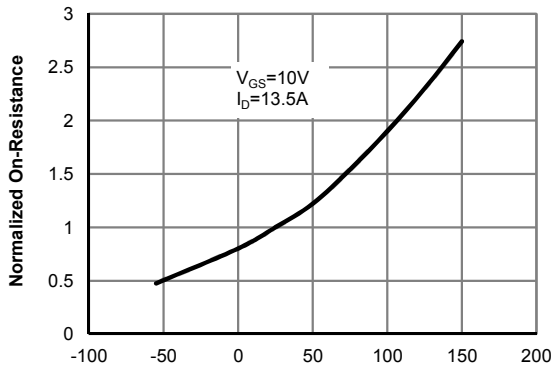


Figure 5: On-Resistance vs. Junction Temperature

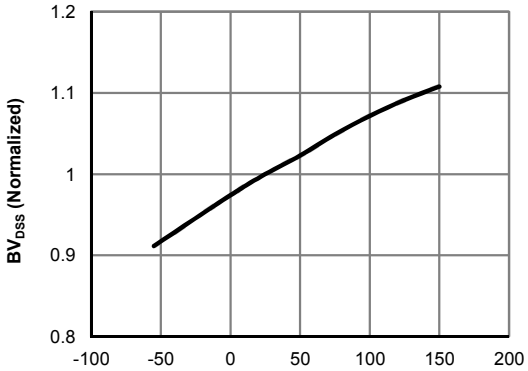


Figure 6: Break Down vs. Junction Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

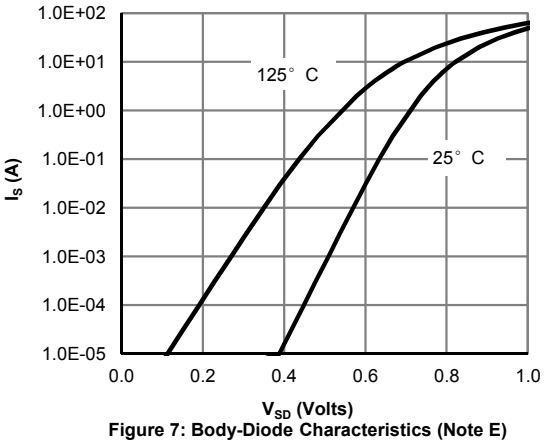


Figure 7: Body-Diode Characteristics (Note E)

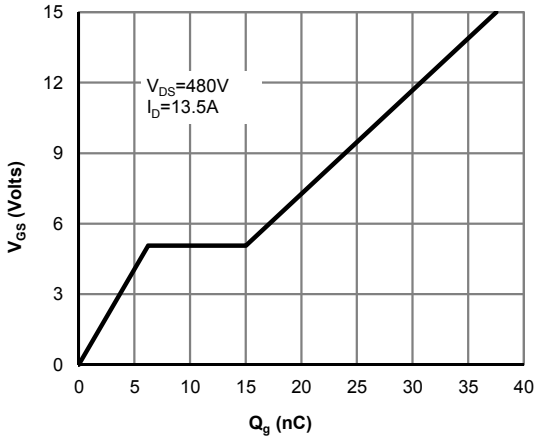


Figure 8: Gate-Charge Characteristics

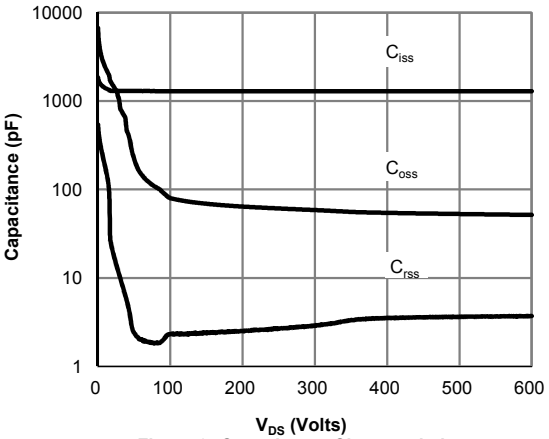


Figure 9: Capacitance Characteristics

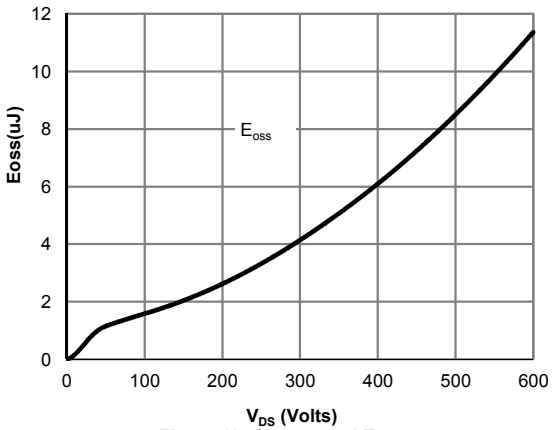


Figure 10: Coss stored Energy

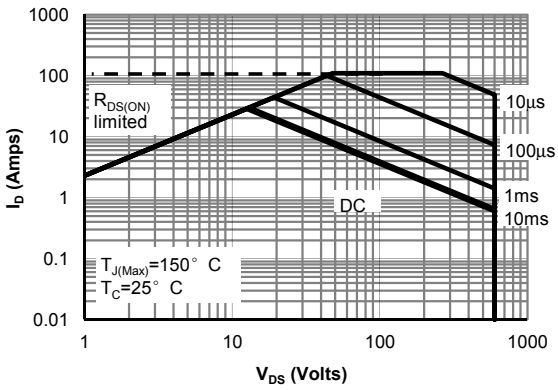


Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)27S60L (Note F)

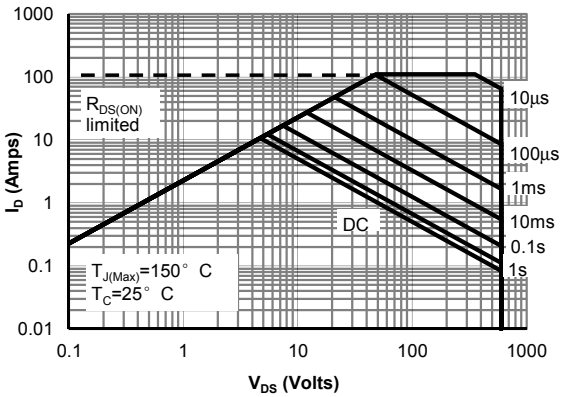


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF27S60(Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

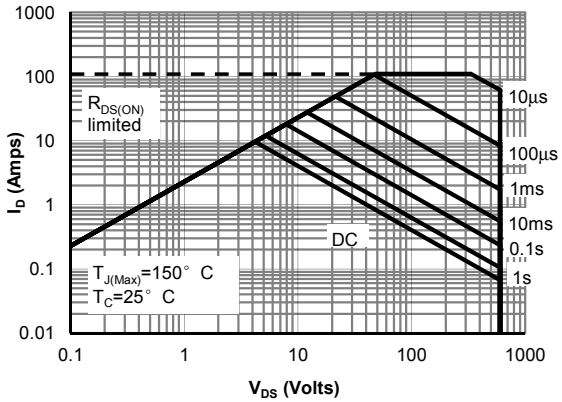


Figure 13: Maximum Forward Biased Safe Operating Area for AOTF27S60L(Note F)

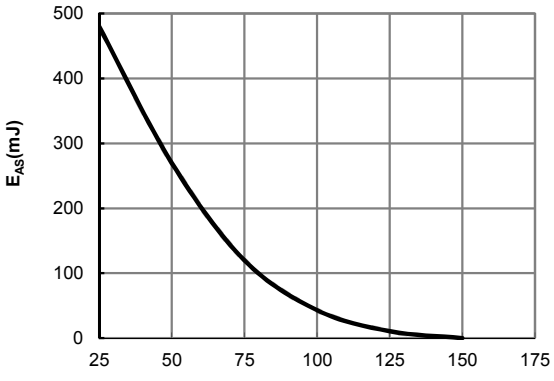


Figure 14: Avalanche energy

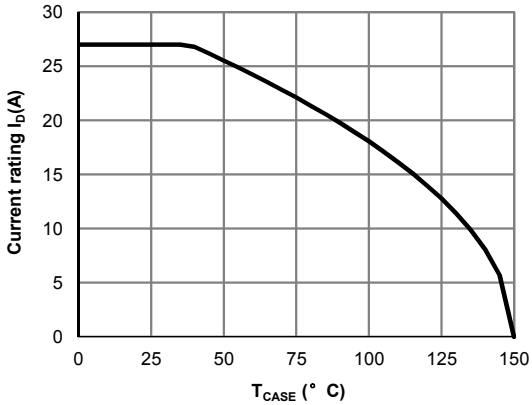


Figure 15: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

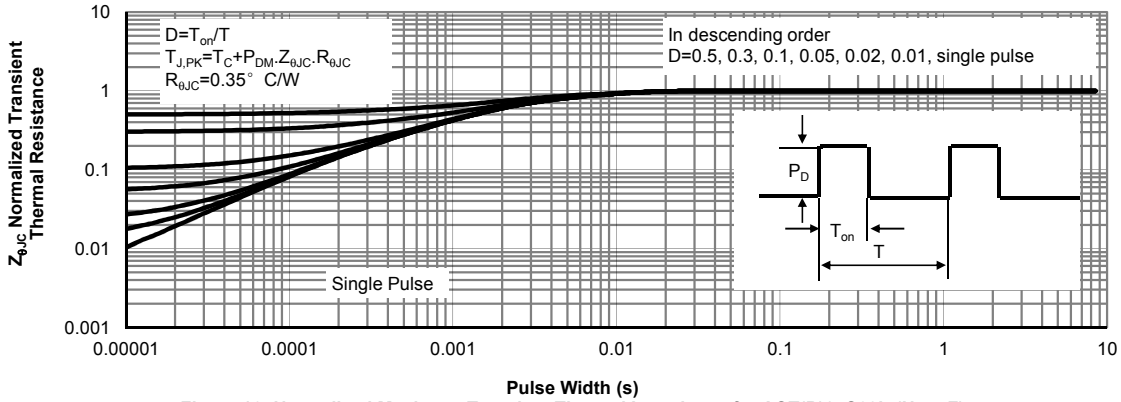


Figure 16: Normalized Maximum Transient Thermal Impedance for AOT(B)27S60L (Note F)

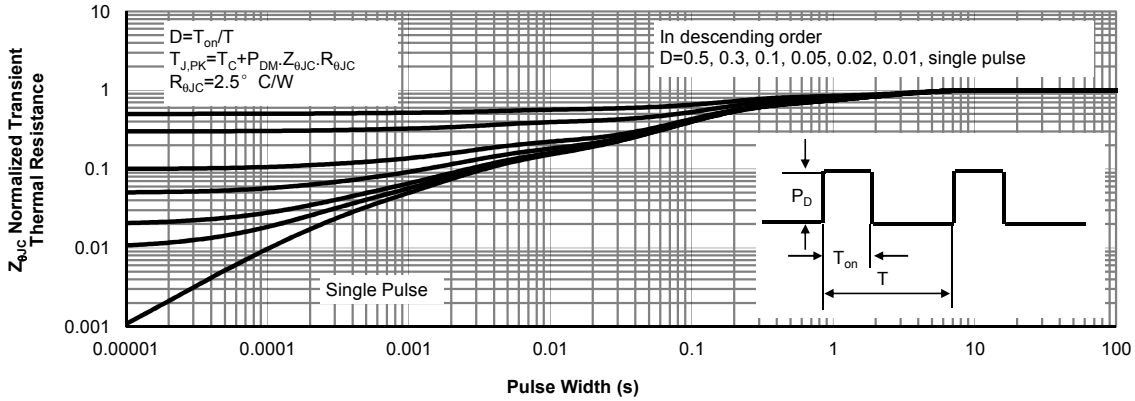


Figure 17: Normalized Maximum Transient Thermal Impedance for AOTF27S60 (Note F)

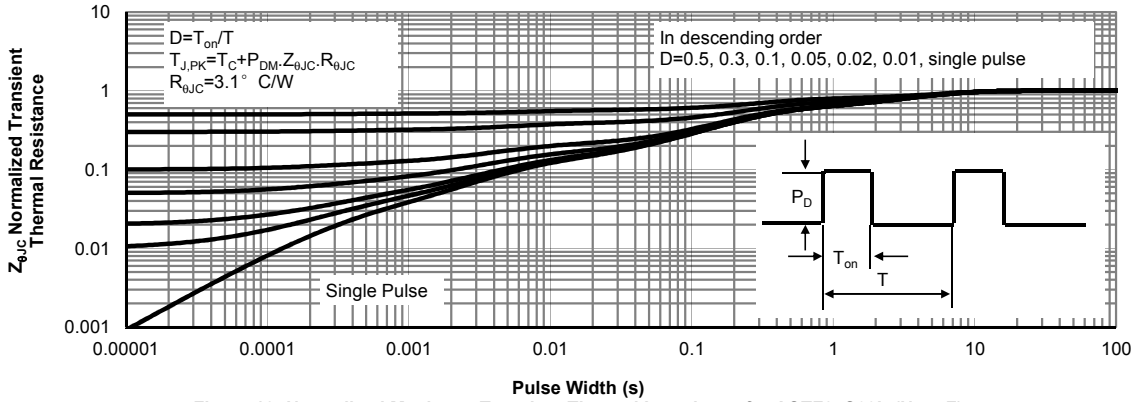
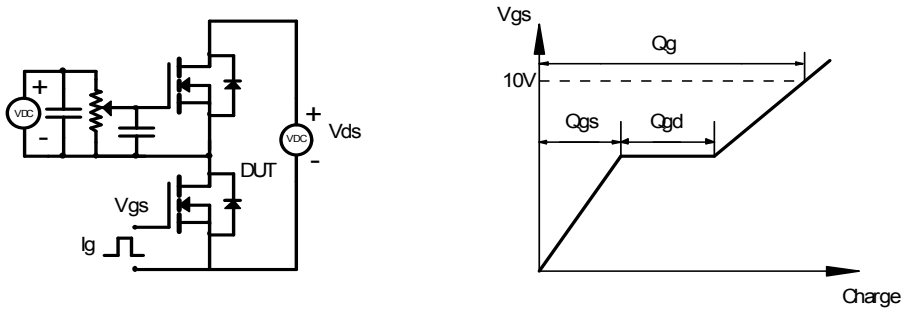
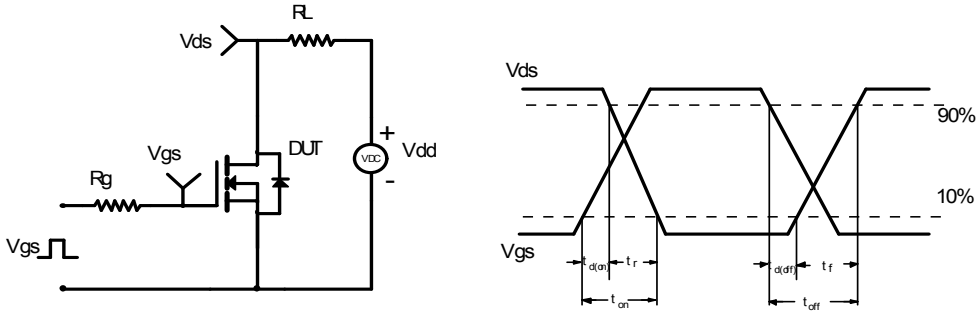


Figure 18: Normalized Maximum Transient Thermal Impedance for AOTF27S60L (Note F)

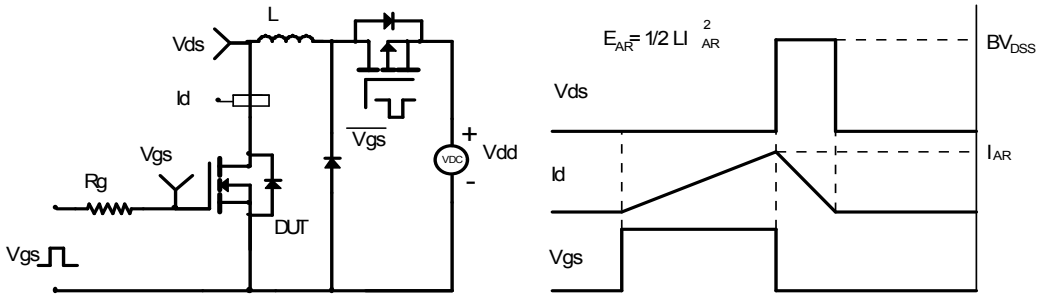
Gate Charge Test Circuit & Waveform



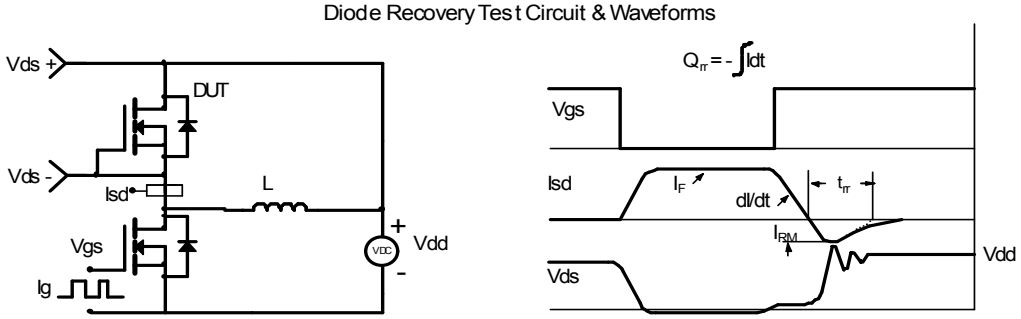
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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