ALPHA & OMEGA SEMICONDUCTOR

# AOB411L

## 60V P-Channel MOSFET

### General Description

The AOB411L combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

### Product Summary

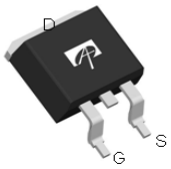
| | |
|---|---|
| $V_{DS}$ | -60V |
| $I_D$ (at $V_{GS}$=-10V) | -78A |
| $R_{DS(ON)}$ (at $V_{GS}$=-10V) | < 16.5mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=-4.5V) | < 22mΩ |

100% UIS Tested
100% $R_g$ Tested

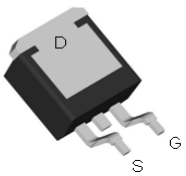
Green Product

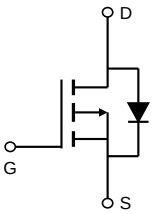
TO-263
D²PAK

Top View




Bottom View




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | -78 | A |
| | $T_C$=100°C | | -55 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -230 | |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | -8 | A |
| | $T_A$=70°C | | -6.5 | |
| Avalanche Current [C] | | $I_{AS}$, $I_{AR}$ | -77 | A |
| Avalanche energy L=0.1mH [C] | | $E_{AS}$, $E_{AR}$ | 296 | mJ |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 187 | W |
| | $T_C$=100°C | | 93 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 2.1 | W |
| | $T_A$=70°C | | 1.3 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 175 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 11 | 15 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 47 | 60 | °C/W |
| Maximum Junction-to-Case | Steady-State | $R_{\theta JC}$ | 0.6 | 0.8 | °C/W |

## Electrical Characteristics ($T_J$=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | -60 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-60V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=-250µA | -1.5 | -2 | -2.5 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-10V, $V_{DS}$=-5V | -230 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-10V, $I_D$=-20A | | 13.5 | 16.5 | mΩ |
| | | $T_J$=125°C | | 20.5 | 25 | |
| | | $V_{GS}$=-4.5V, $I_D$=-20A | | 17 | 22 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-20A | | 48 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | -0.7 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current [G] | | | | -105 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-30V, f=1MHz | 4260 | 5330 | 6400 | pF |
| $C_{oss}$ | Output Capacitance | | 335 | 483 | 630 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 140 | 234 | 330 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 1.4 | 2.8 | 4.2 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=-10V, $V_{DS}$=-30V, $I_D$=-20A | 65 | 83 | 100 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | 35 | 40 | 50 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 15 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 18 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-10V, $V_{DS}$=-30V, $R_L$=1.5Ω, $R_{GEN}$=3Ω | | 17.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 20 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 83.5 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 37 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-20A, dI/dt=500A/µs | 18 | 27 | 36 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-20A, dI/dt=500A/µs | 110 | 165 | 215 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. The maximum current limited by package.
H. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

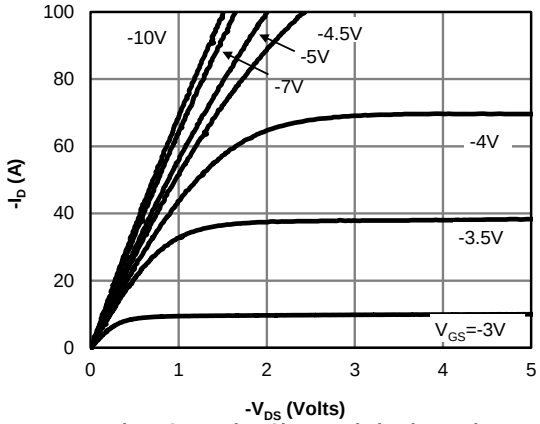



Fig 1: On-Region Characteristics (Note E)

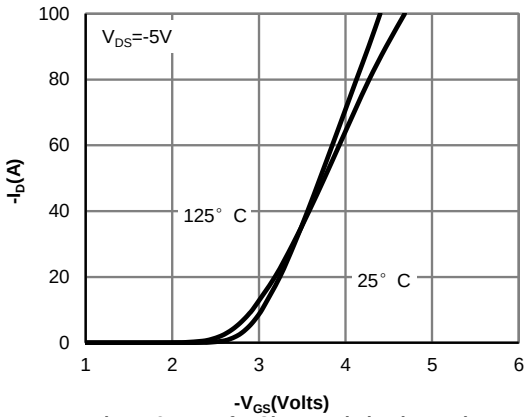



Figure 2: Transfer Characteristics (Note E)

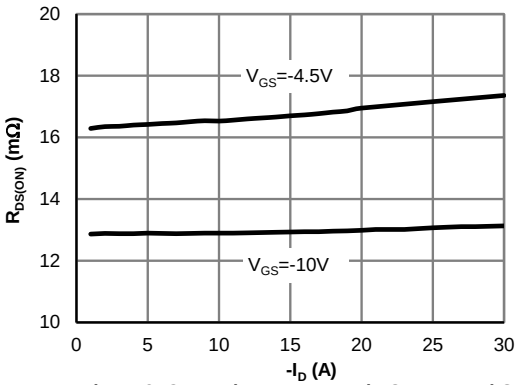



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

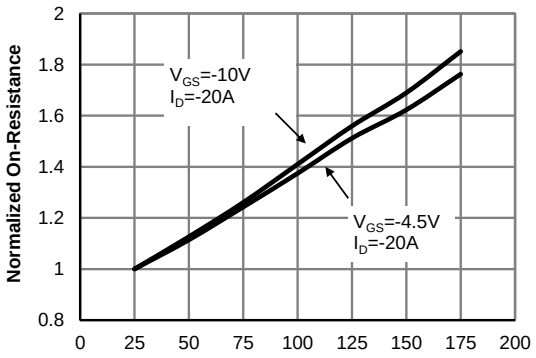



Figure 4: On-Resistance vs. Junction Temperature (Note E)

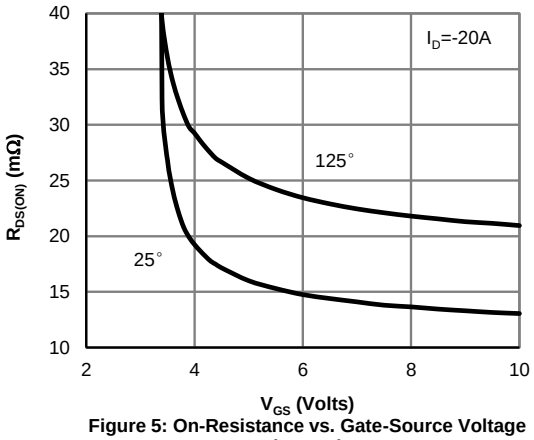



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

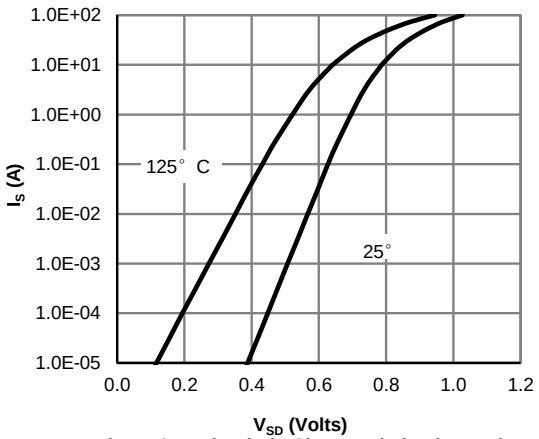



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

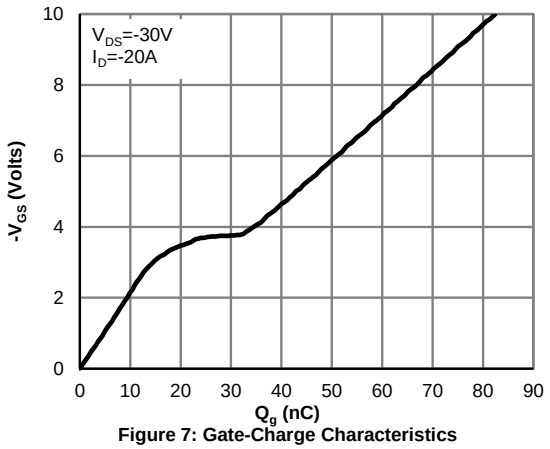



Figure 7: Gate-Charge Characteristics

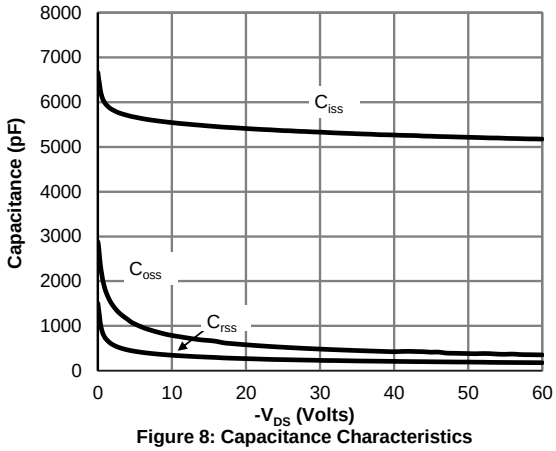



Figure 8: Capacitance Characteristics

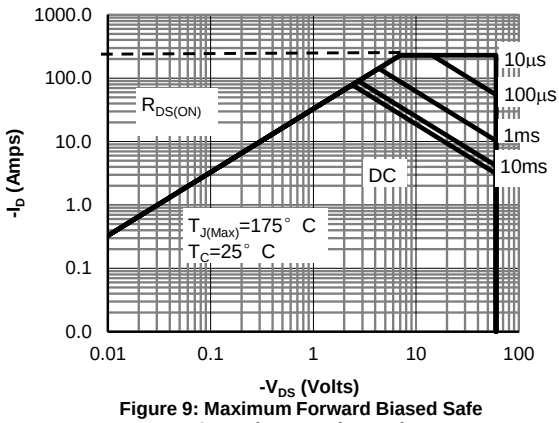



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

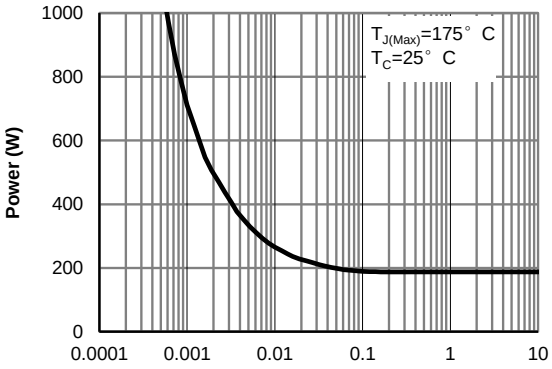



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

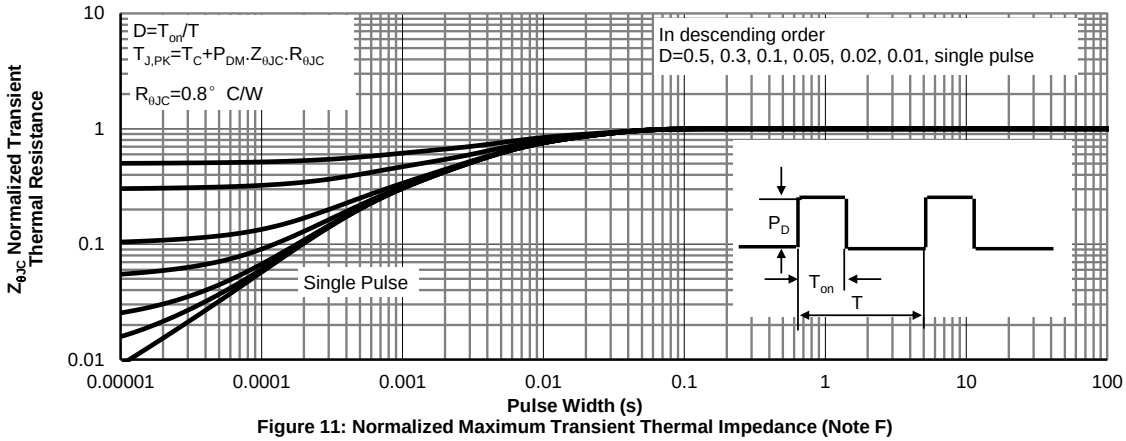



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

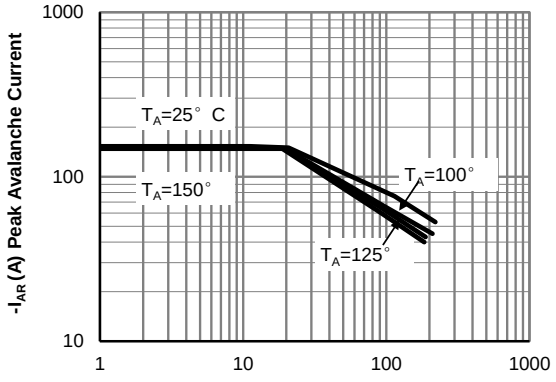



**Figure 12: Single Pulse Avalanche capability (Note C)**

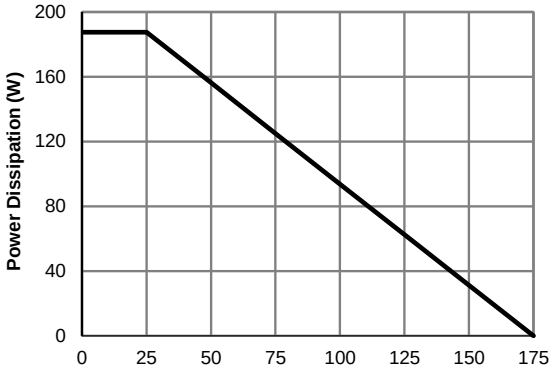



**Figure 13: Power De-rating (Note F)**

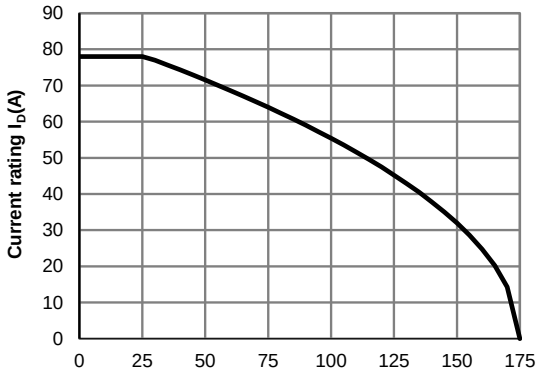



**Figure 14: Current De-rating (Note F)**

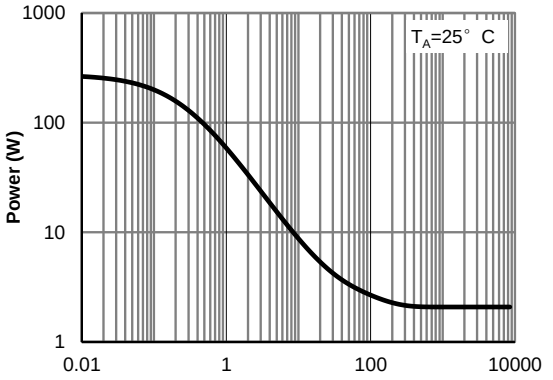



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

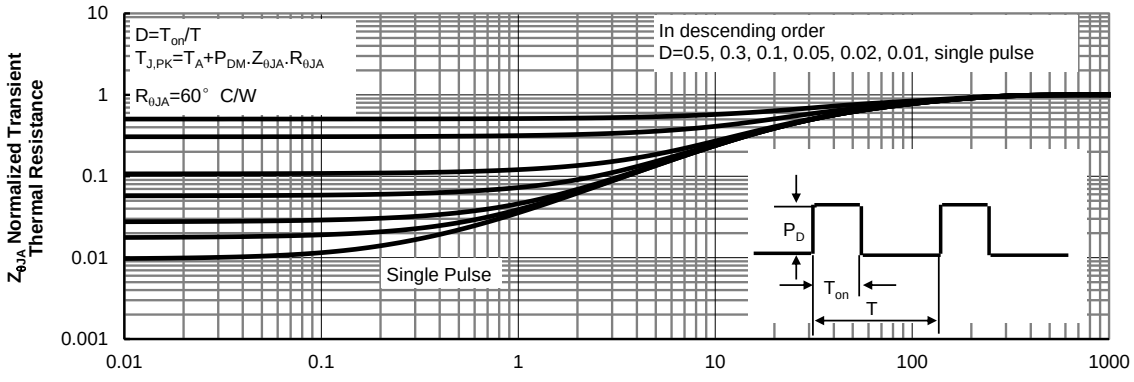
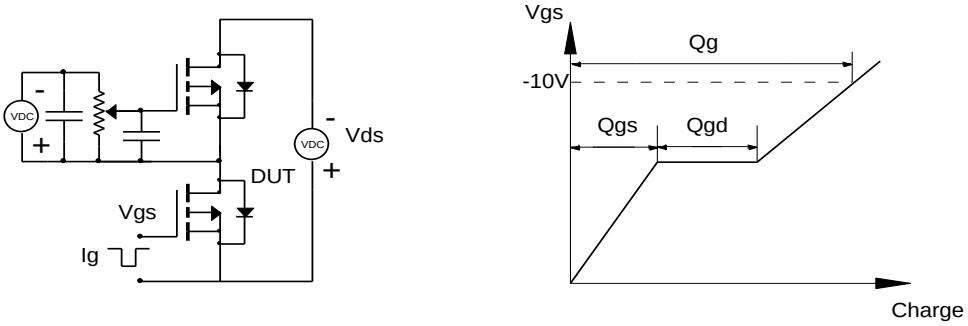
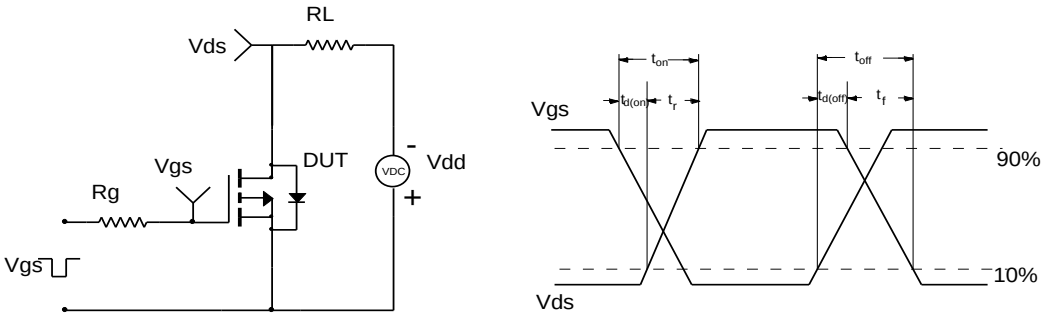



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

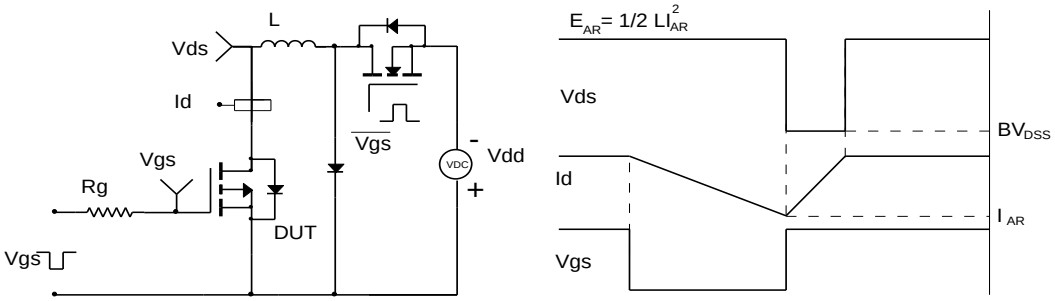
## Gate Charge Test Circuit & Waveform



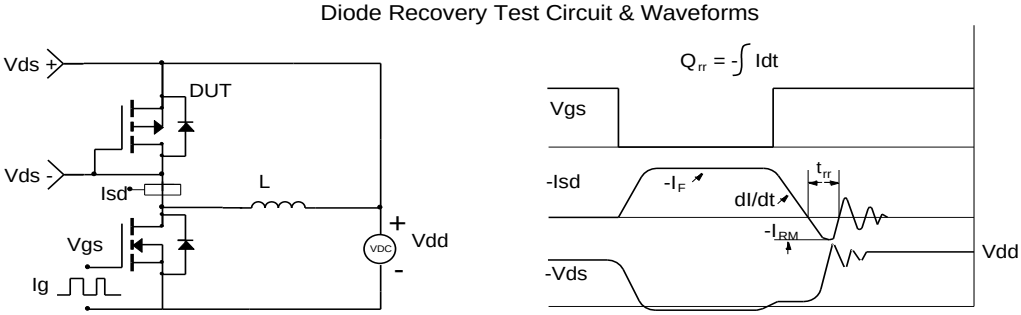

## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms



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