ALPHA & OMEGA SEMICONDUCTOR

AOB4184
40V N-Channel MOSFET

General Description

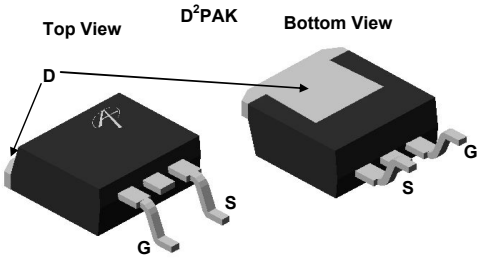
The AOB4184 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. With the excellent thermal resistance of the D^2PAK package, this device is well suited for high current load applications.

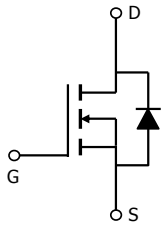
Features

V_{DS} (V) =40V
I_D = 50 A (V_{GS} = 10V)
$R_{DS(ON)}$ < 10 mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 13 mΩ (V_{GS} = 4.5V)

100% UIS Tested
100% Rg Tested

TO-263
D^2PAK





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	50	A
	T_C=100°C		40	
Pulsed Drain Current [C]		I_{DM}	120	
Continuous Drain Current [A]	T_C=25°C	I_{DSM}	12	
	T_C=70°C		10	
Avalanche Current [C]		I_{AS}, I_{AR}	35	A
Avalanche energy L=100uH [C]		E_{AS}, E_{AR}	61	mJ
Power Dissipation [B]	T_C=25°C	P_D	50	W
	T_C=100°C		25	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	11	17	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		42	50	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	2.4	3	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA		1.7	2.1	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			8.5	10	mΩ
			T_J=125°C		13.2	17	
		V_{GS}=4.5V, I_D=20A			10	13	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			100		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.72	1	V
I_S	Maximum Body-Diode Continuous Current[G]					30	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz		1250	1500	1800	pF
C_{oss}	Output Capacitance			165	215	280	pF
C_{rss}	Reverse Transfer Capacitance			95	135	190	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2	3.5	5	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=20A		22	27.2	35	nC
Q_g(4.5V)	Total Gate Charge			11	13.6	18	nC
Q_{gs}	Gate Source Charge			3.5	4.5	6	nC
Q_{gd}	Gate Drain Charge			4.5	6.4	9	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1Ω, R_{GEN}=3Ω			6.4		ns
t_r	Turn-On Rise Time				17.2		ns
$t_{D(off)}$	Turn-Off DelayTime				29.6		ns
t_f	Turn-Off Fall Time				16.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		15	19	25	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		48	59	78	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

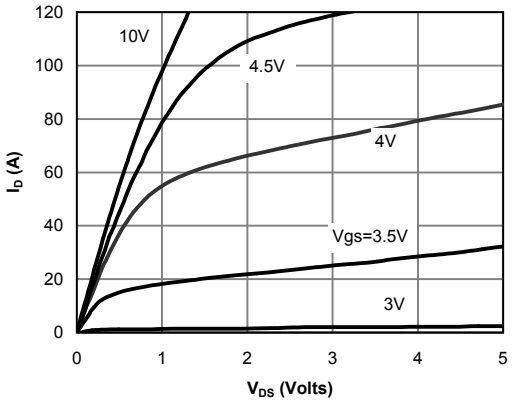


Figure 1: On-Region Characteristics

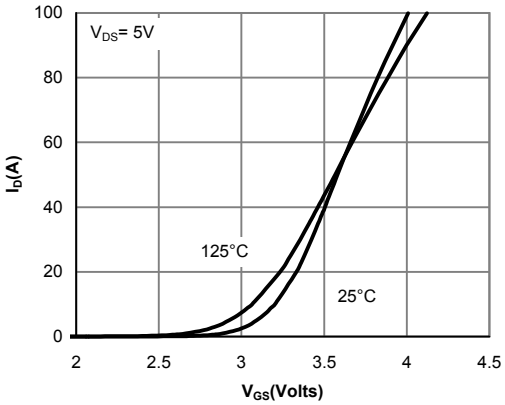


Figure 2: Transfer Characteristics

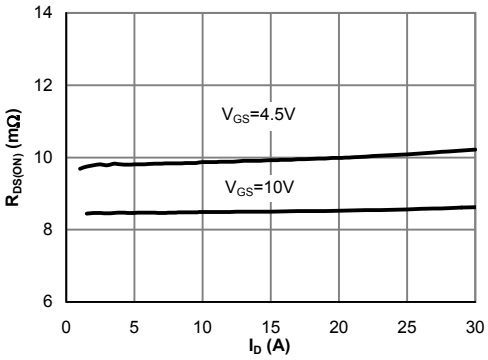


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

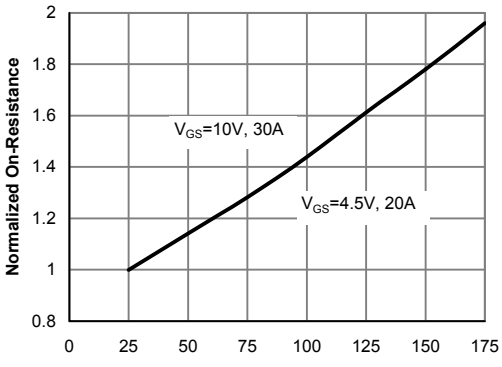


Figure 4: On-Resistance vs. Junction Temperature

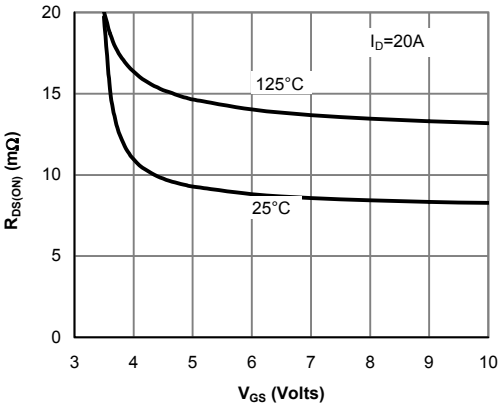


Figure 5: On-Resistance vs. Gate-Source Voltage

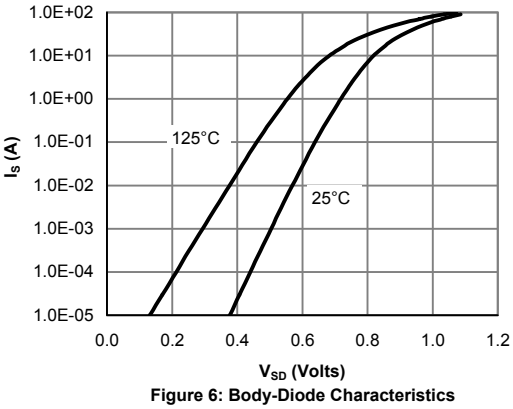


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

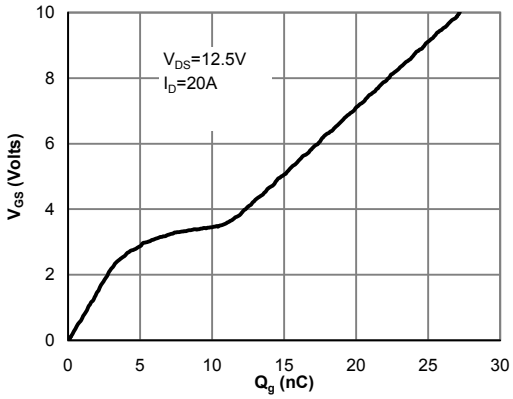


Figure 7: Gate-Charge Characteristics

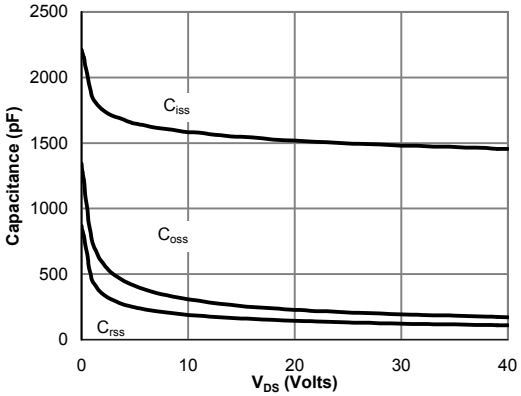


Figure 8: Capacitance Characteristics

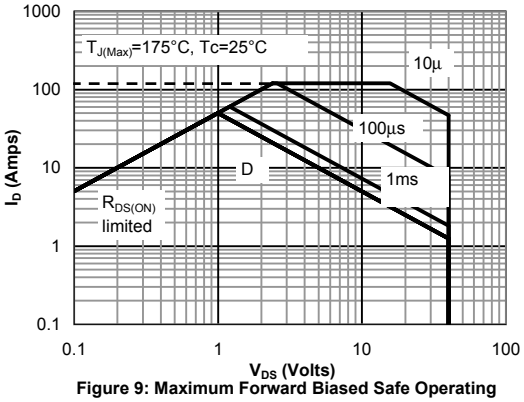


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

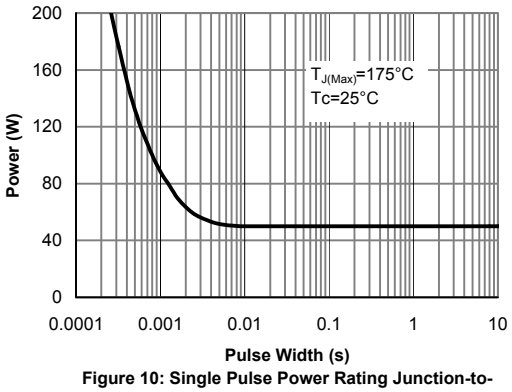


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

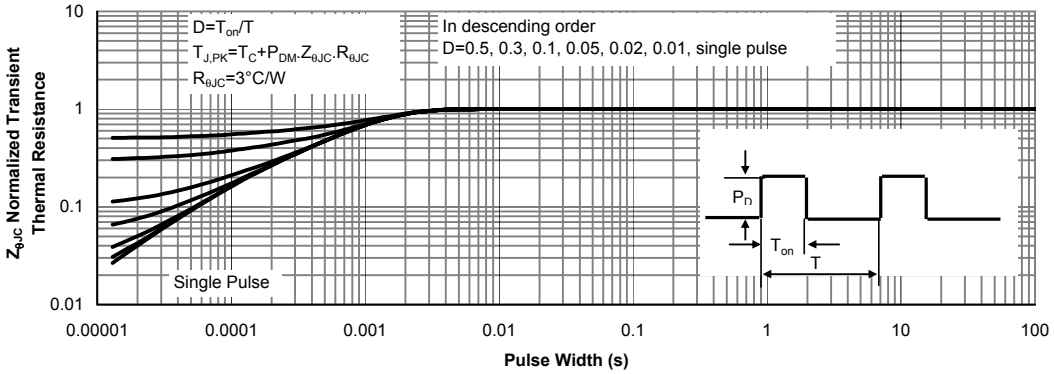


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

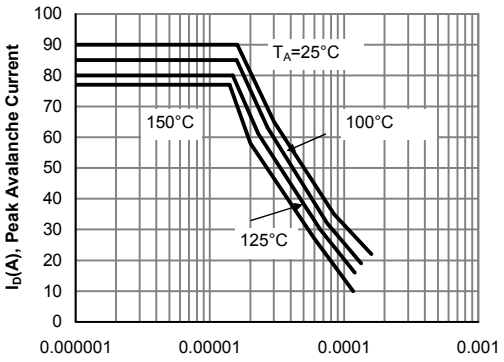


Figure 12: Single Pulse Avalanche capability

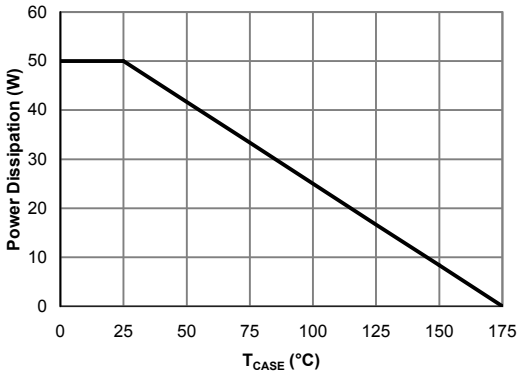


Figure 13: Power De-rating (Note F)

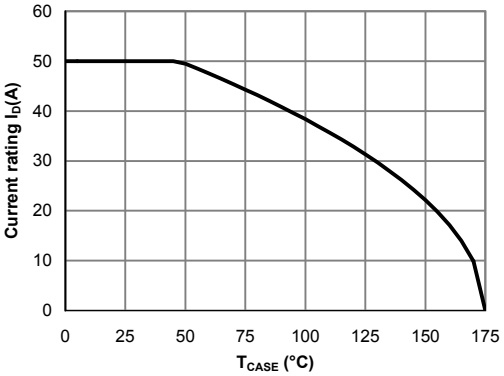


Figure 14: Current De-rating (Note F)

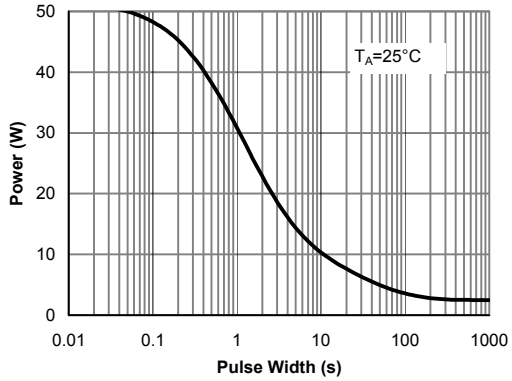


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

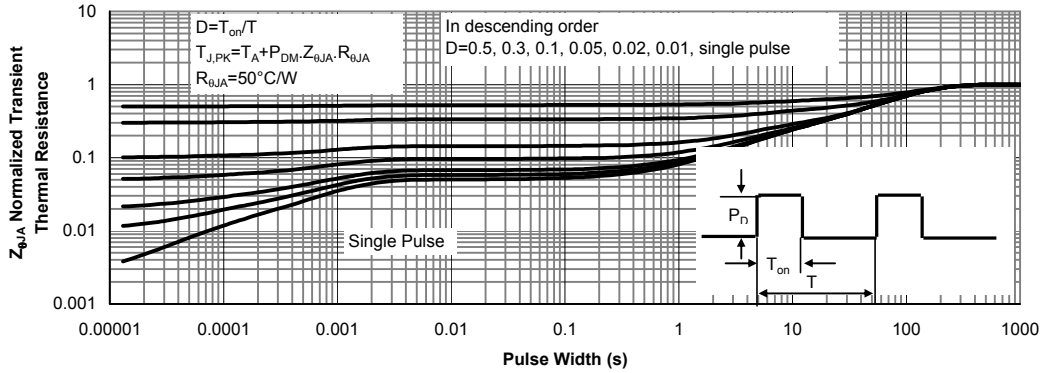
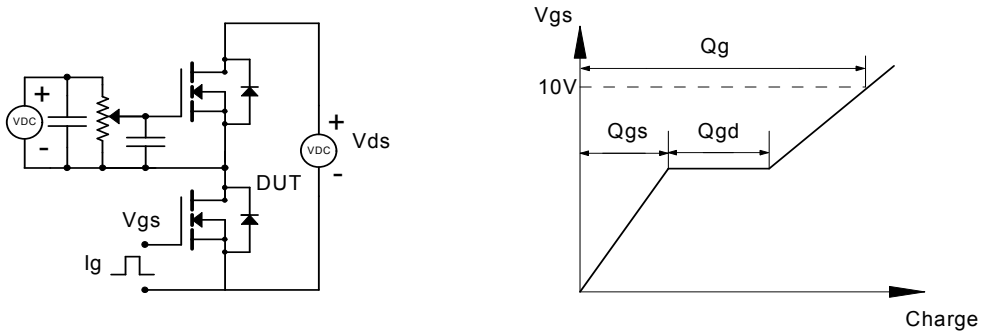
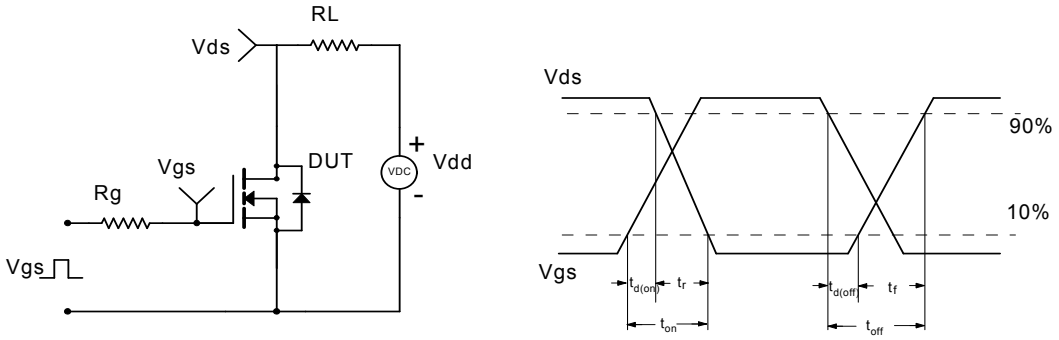


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

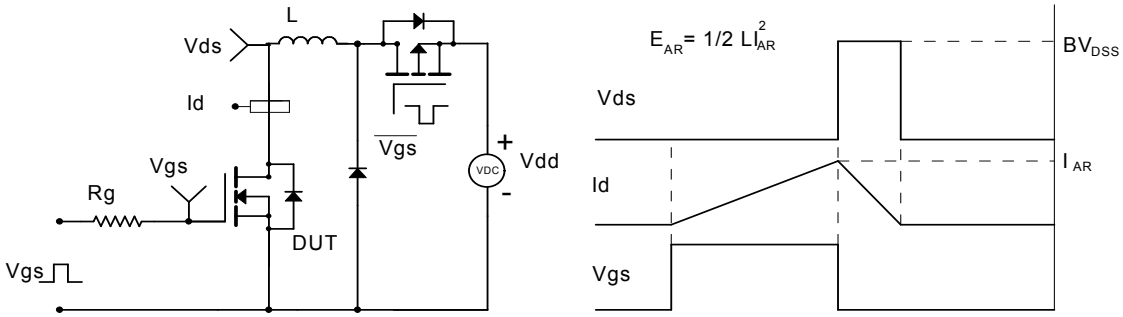
Gate Charge Test Circuit & Waveform



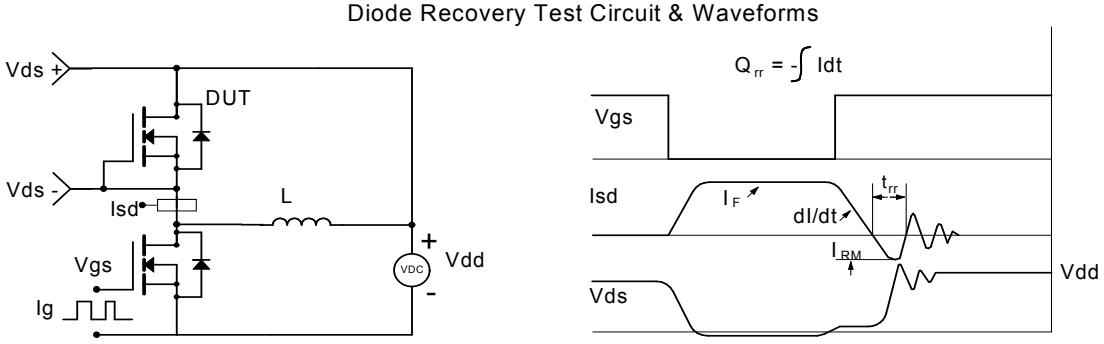
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