ALPHA & OMEGA SEMICONDUCTOR

AON2392

100V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Logic driven
- RoHS and Halogen-Free Compliant

Applications

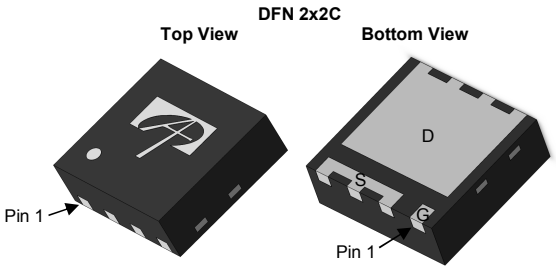
- Home Automation and IoT
- VOIP applications

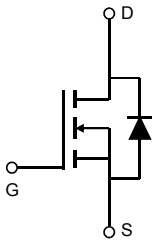
Product Summary

V_{DS}	100V
I_D (at V_{GS}=10V)	8A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 32mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 39mΩ

Green Product

DFN 2x2C





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON2392	DFN2x2C	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	8	A
	T_A=70°C		6	
Pulsed Drain Current [C]		I_{DM}	32	
Power Dissipation [B]	T_A=25°C	P_D	4.1	W
	T_A=70°C		2.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	25	30	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		45	55	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.4	1.85	2.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8A		26	32	mΩ
		T_J=125°C		46	57	
		V_{GS}=4.5V, I_D=6A		31	39	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz		840		pF
C_{oss}	Output Capacitance			64		pF
C_{rss}	Reverse Transfer Capacitance			4		pF
R_g	Gate resistance	f=1MHz		1.4		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=8A		12.8	25	nC
Q_g(4.5V)	Total Gate Charge			6.1	12	nC
Q_{gs}	Gate Source Charge			2.1		nC
Q_{gd}	Gate Drain Charge			1.8		nC
Q_{oss}	Output Charge	V_{GS}=0V, V_{DS}=50V		11		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=50V, R_L=5.85Ω, R_{GEN}=3Ω		7		ns
t_r	Turn-On Rise Time			8		ns
$t_{D(off)}$	Turn-Off DelayTime			24		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8A, di/dt=500A/µs		20		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8A, di/dt=500A/µs		70		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

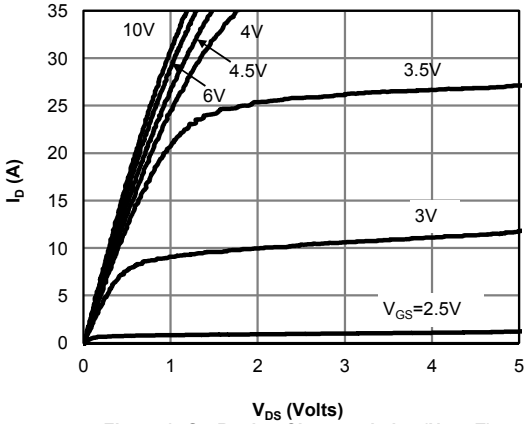


Figure 1: On-Region Characteristics (Note E)

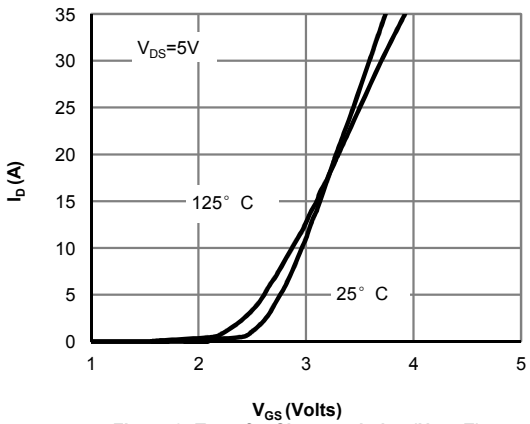


Figure 2: Transfer Characteristics (Note E)

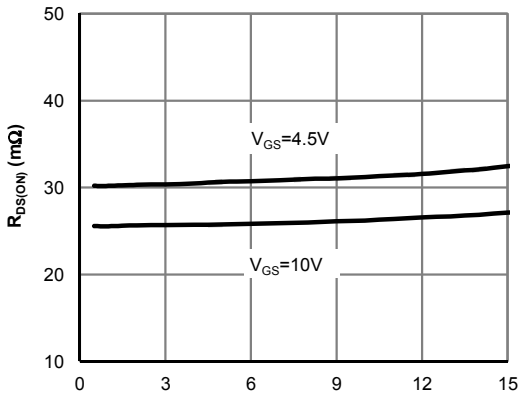


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

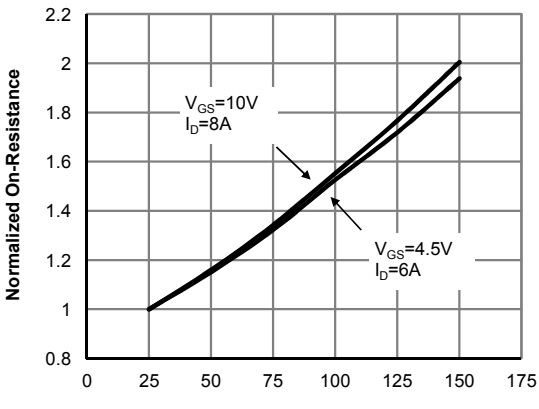


Figure 4: On-Resistance vs. Junction Temperature (Note E)

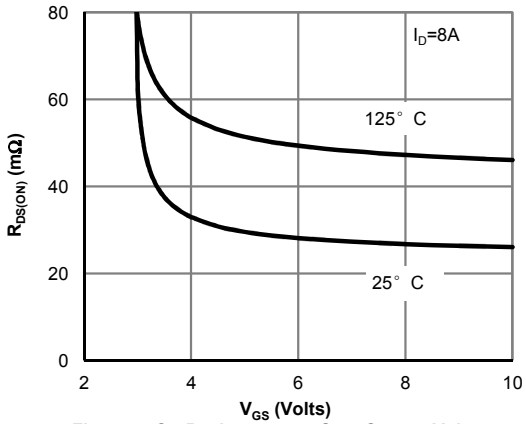


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

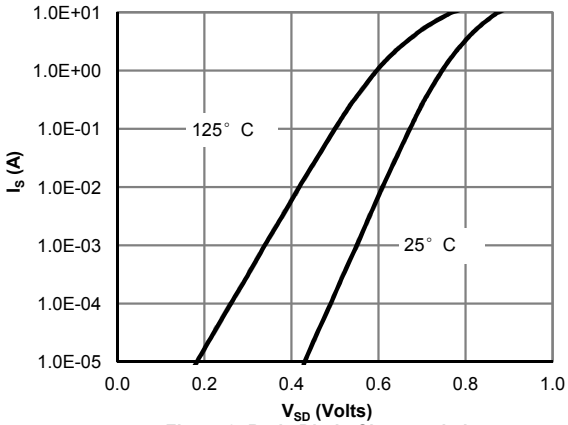


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

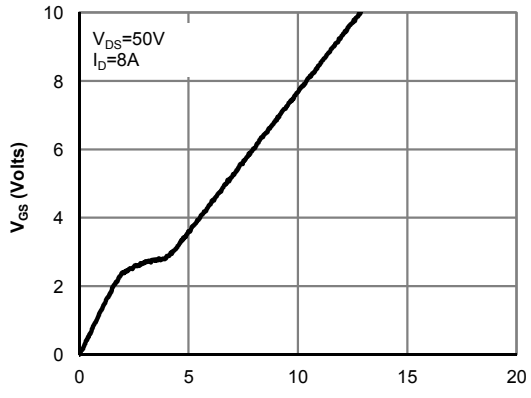


Figure 7: Gate-Charge Characteristics

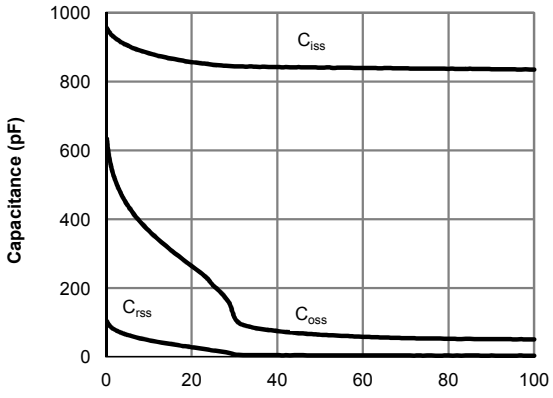


Figure 8: Capacitance Characteristics

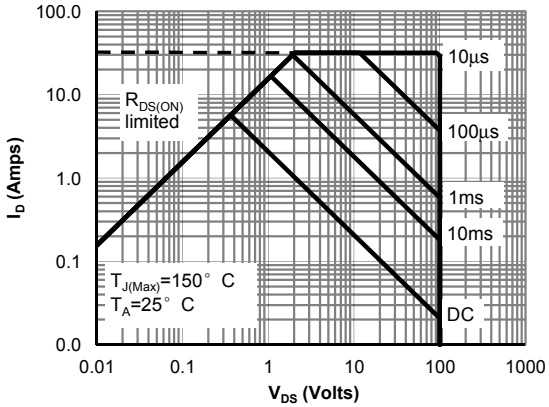


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

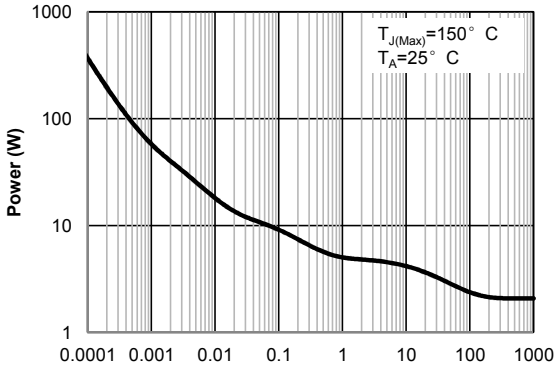


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

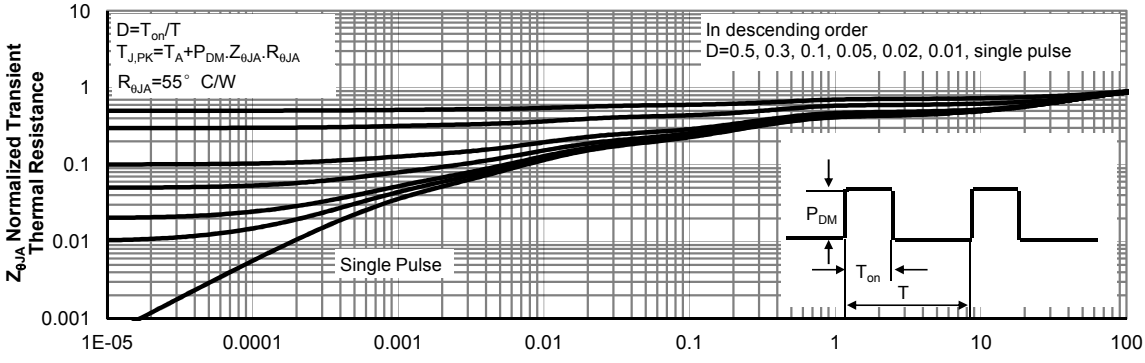


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

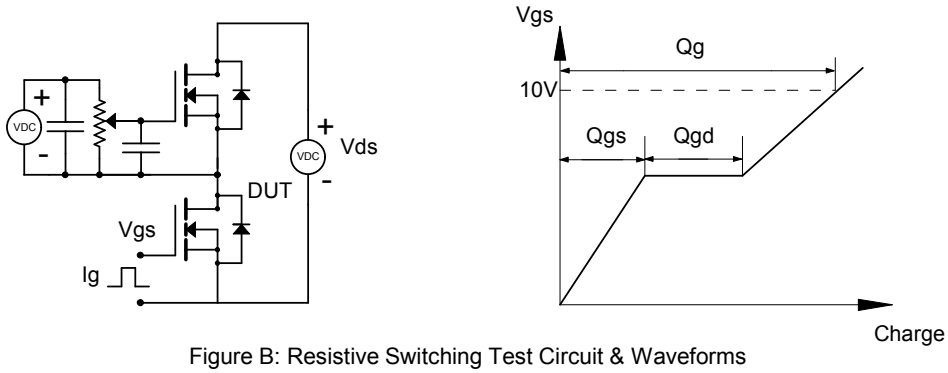


Figure B: Resistive Switching Test Circuit & Waveforms

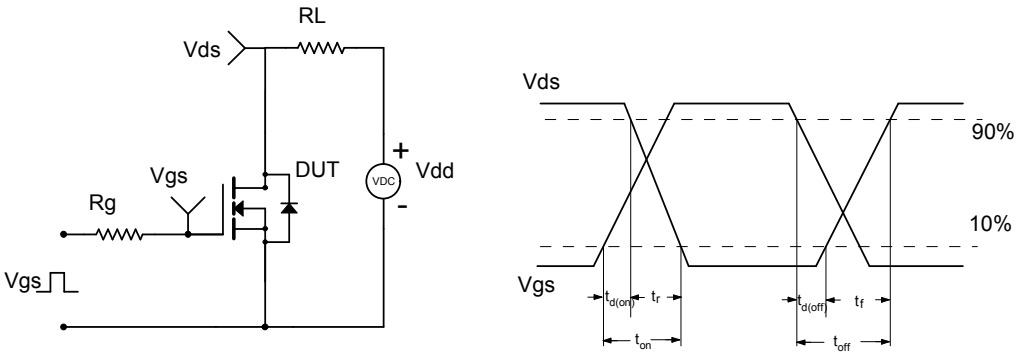


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

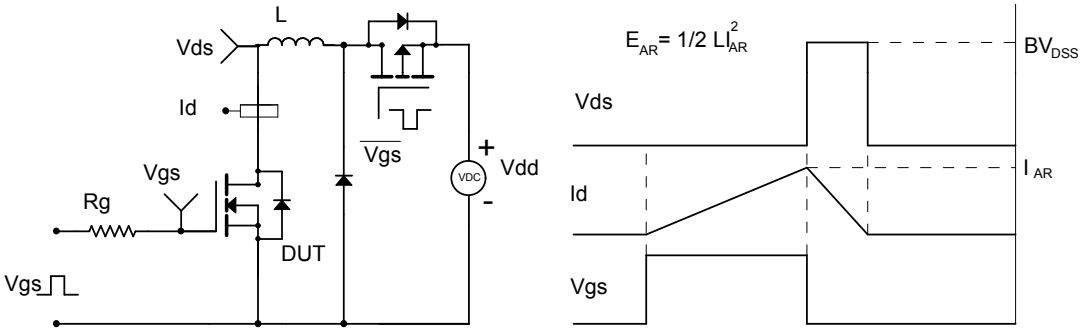
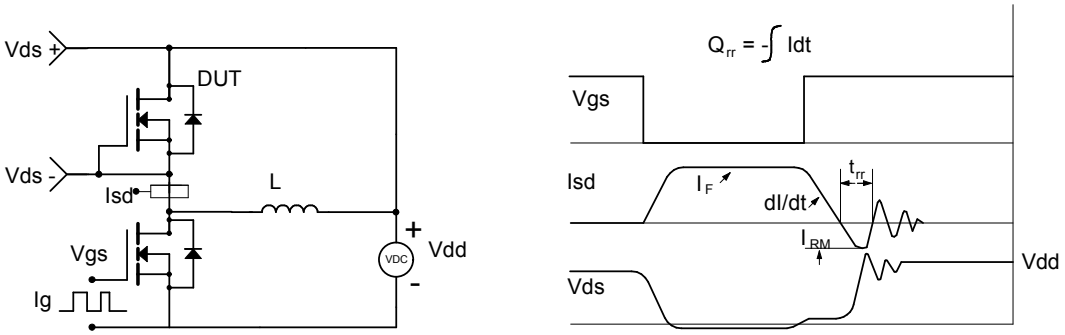


Figure D: Diode Recovery Test Circuit & Waveforms



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