Description

The AP7165 is a 600mA, adjustable output voltage, ultra-low dropout linear regulator. The device includes pass element, error amplifier, band-gap reference, current limit and thermal shutdown circuitry. The device is turned on when EN pin is set to logic high level. A Power-OK (POK) output is available for power sequence control.

The characteristics of the low dropout voltage and low quiescent current make it suitable for low to medium power applications, for example, laptop computers, audio and video applications, and battery powered devices. The typical quiescent current is approximately 125µA.

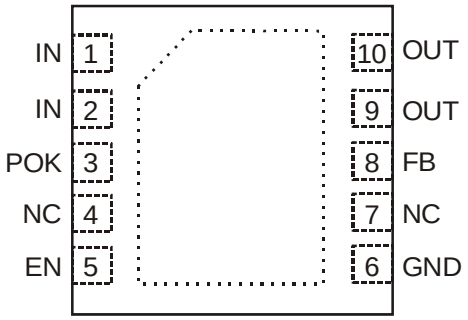
Built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions. The AP7165 are available in U-DFN3030-10 and SO-8EP packages.

Features

- Wide input voltage range: 2.2V – 5.5V
- 300mV very low dropout at 500mA load
- Very low quiescent current (I_Q): 125µA typical
- ± 2.5% total accuracy over line, load and temperature
- Adjustable output voltage range: 0.8V to 5.0V
- Very fast transient response
- High PSRR
- Accurate voltage regulation
- Current limiting and short circuit protection
- Thermal shutdown protection
- Stable with any type output capacitor ≥ 4.7µF
- Ambient temperature range -40ºC to +85°C
- U-DFN3030-10 and SO-8EP: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

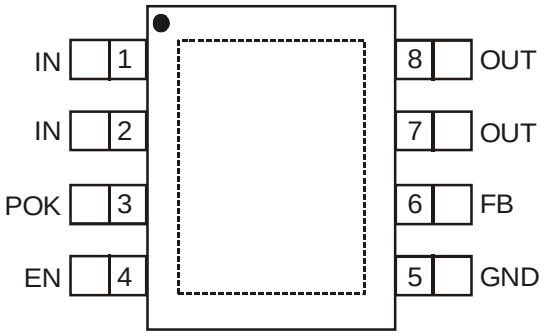
Pin Assignments

(Top View)



U-DFN3030-10

(Top View)



SO-8EP

Applications

- Servers and laptops
- Smart phone and PDA
- MP3/MP4
- Bluetooth headset
- Low and medium power applications
- FPGA and DSP core or I/O power

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

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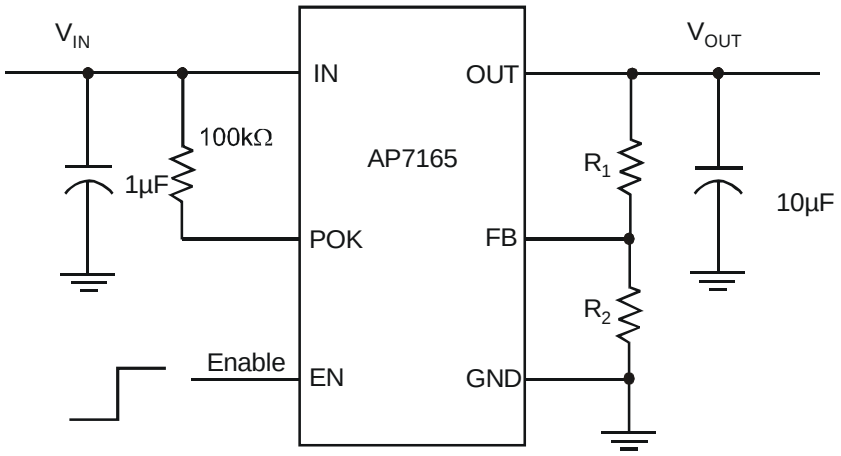
Typical Application Circuit



$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Pin Descriptions

Name	Pin #		Description
	U-DFN3030-10	SO-8EP	
IN	1, 2	1, 2	Voltage input pins, to be tied together externally. Bypass to ground through at least 1µF capacitor.
POK	3	3	Power-OK output, active-high open-drain.
EN	5	4	Enable input, active high.
GND	6	5	Ground.
FB	8	6	Output feedback.
OUT	9, 10	7, 8	Voltage output pins, to be tied together externally. Bypass to ground through at least 4.7µF ceramic capacitor.
NC	4, 7	NA	No connection.

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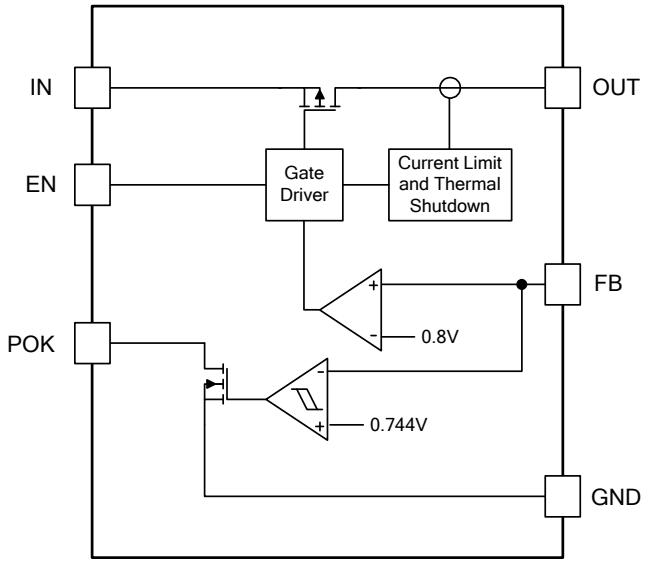
Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Ratings	Unit
ESD HBM	Human Body Model ESD Protection		4	KV
ESD MM	Machine Model ESD Protection		300	V
V_{IN}	Input Voltage		7	V
	OUT, FB, POK, EN Voltage		V_{IN} +0.3	V
	Continuous Load Current		Internal Limited	
T_{Jmax}	Maximum Junction Temperature		150	°C
T_{ST}	Storage Temperature Range		-65 ~ +150	°C
P_D	Power Dissipation	U-DFN3030-10 (Note 2, 4)	3.1	W
		SO-8EP (Note 2, 5)	4.0	W

Notes: 2. Ratings apply to ambient temperature at 25°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input voltage	2.2	5.5	V
I_{OUT}	Output Current	0	600	mA
T_A	Operating Ambient Temperature	-40	+85	°C

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Electrical Characteristics

(T_A = 25°C, V_{IN} = V_{OUT} +1V, C_{IN} = 1µF, C_{OUT} = 10µF, V_{EN} = V_{IN}, unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Input Quiescent Current	I_{OUT} = 0	—	125	170	µA
I_{SHDN}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0 (Note 3)	-1	0.01	+1	µA
V_{ROPOUT}	Dropout Voltage	$V_{OUT} \geq$ 1.5V, $I_{OU\,T}$ = 500mA		300	400	mV
V_{REF}	FB reference voltage			0.8		V
I_{FB}	FB leakage		—	0.01	1	µA
V_{OUT}	Output Voltage Total Accuracy	Over line, load and temperature	-2.5		+2.5	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}} / V_{OUT}$	Line Regulation	V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 1mA		0.015		%/V
ΔV_{OUT} / V_{OUT}	Load Regulation	I_{OUT} from 1mA to 500mA	-1.0		+1.0	%
t_{ST}	Start-up Time, from EN high to POK high	V_{EN} = 0V to 2.0V, I_{OUT} = 100mA, V_{IN} = 3.3V		170		µs
PSRR	Power Supply Rejection Ratio	1kHz, V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0mA		60		dB
I_{LIMIT}	Current limit	V_{OUT} = 1.8V, R_{OUT} = 0.5Ω	600	950		mA
I_{SHORT}	Short-circuit Current	V_{IN} = 3.3V, V_{OUT} < 0.2V		380		mA
V_{IL}	EN Input Logic Low Voltage				0.4	V
V_{IH}	EN Input Logic High Voltage		1.4			V
I_{EN}	EN Input leakage	V_{EN} = 0V or 5.5V	—	0.01	1	µA
V_{OL}	POK output low voltage	Force 2mA		100	200	mV
$V_{POK_TH_UP}$	Output voltage (rising) POK threshold	FB (or OUT for fixed version) rising	87%	92%	97%	V_{ref}
V_{POK_Hys}	Output voltage POK hysteresis			4%		V_{ref}
POK deglitch		V_{IN} = 3.3V, V_{OUT} = 1.2V		150		µs
I_{POK_LK}	POK leakage current	V_{POK} = 5.5V	—	0.01	1	µA
T_{SHDN}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown hysteresis			25		°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	U-DFN3030-10 (Note 4)		40		°C/W
		SO-8EP (Note 5)		27		°C/W
θ_{JC}	Thermal Resistance Junction-to- Case	U-DFN3030-10 (Note 4)		9		°C/W
		SO-8EP (Note 5)		4		°C/W

Notes:
3. POK pin must be disconnected from IN pin.
4. Test condition for U-DFN3030-10: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 6 vias to bottom layer 1.0"x1.5" ground plane.
5. Test condition for SO-8EP: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

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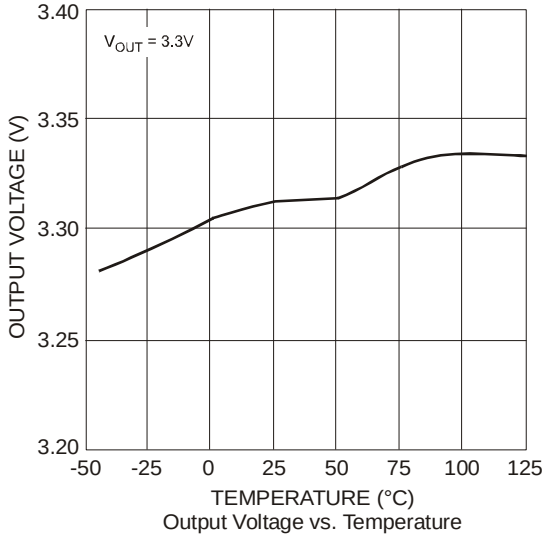
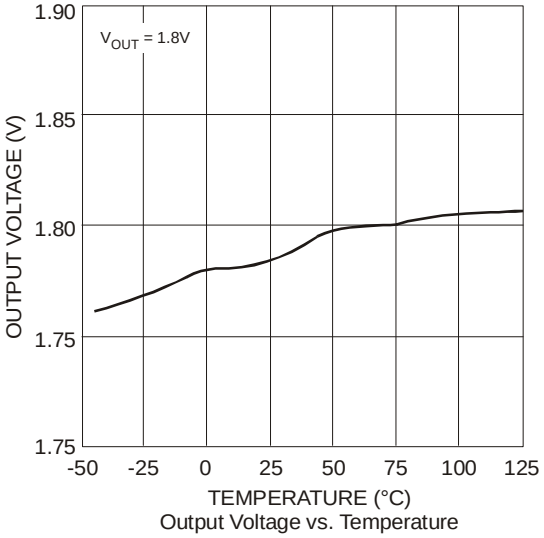
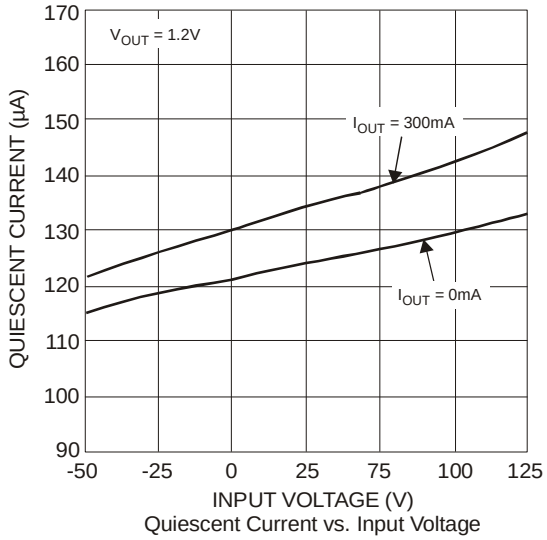
Typical Performance Characteristics



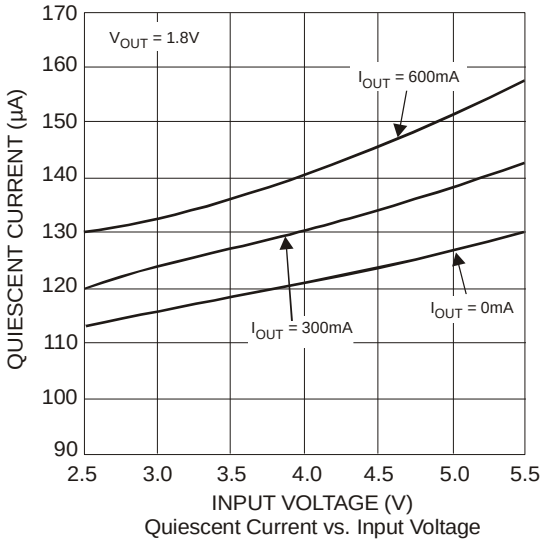
Output Voltage vs. Temperature



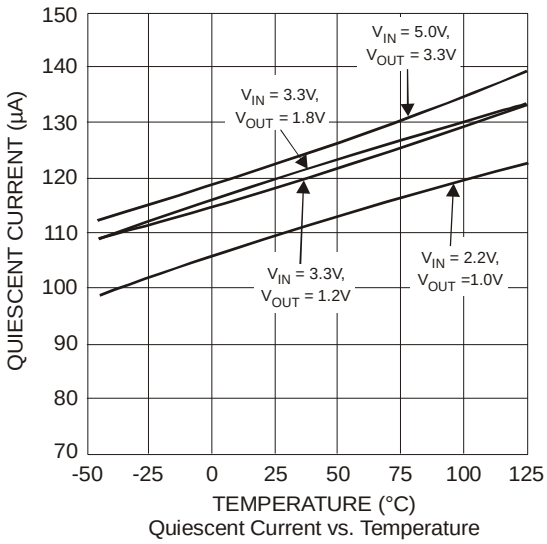
Output Voltage vs. Temperature



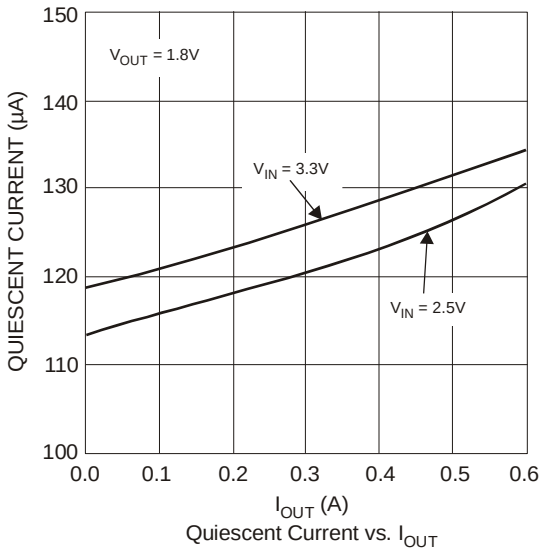
Quiescent Current vs. Input Voltage



Quiescent Current vs. Input Voltage



Quiescent Current vs. Temperature



Quiescent Current vs. I_{OUT}

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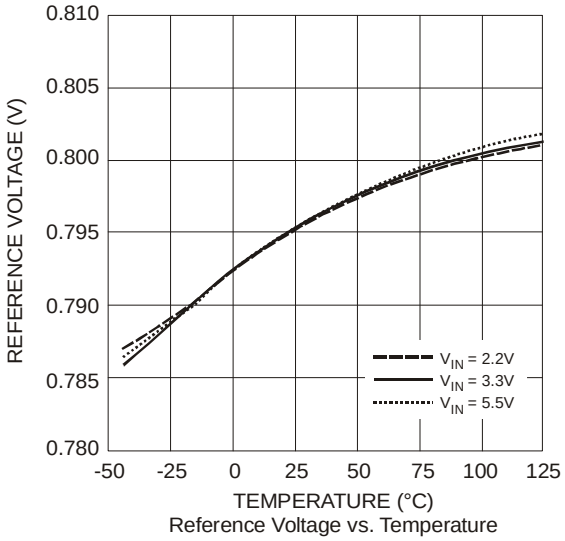
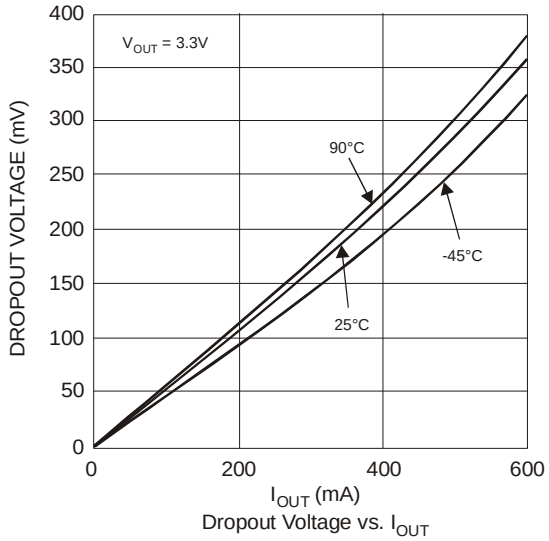
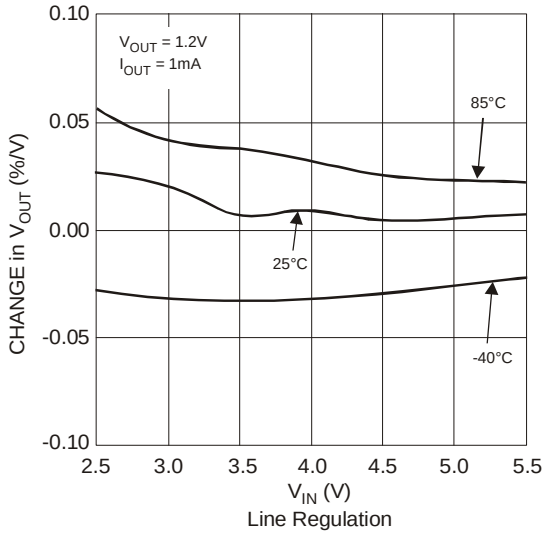
Typical Performance Characteristics (cont.)



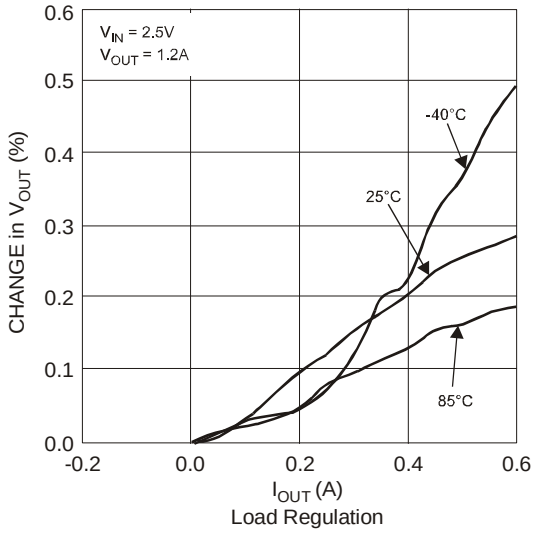
Reference Voltage vs. Temperature



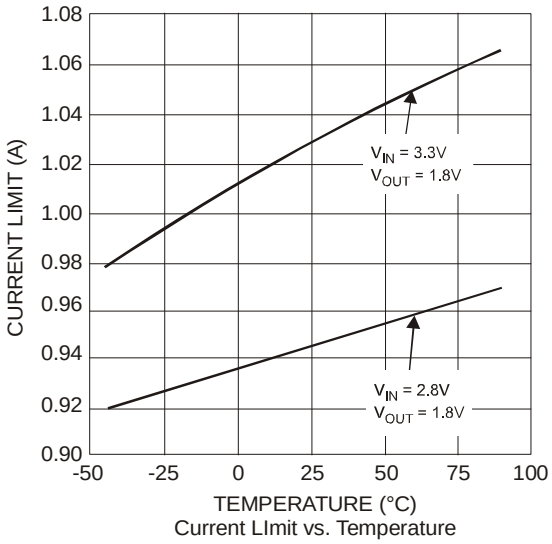
Dropout Voltage vs. I_{OUT}



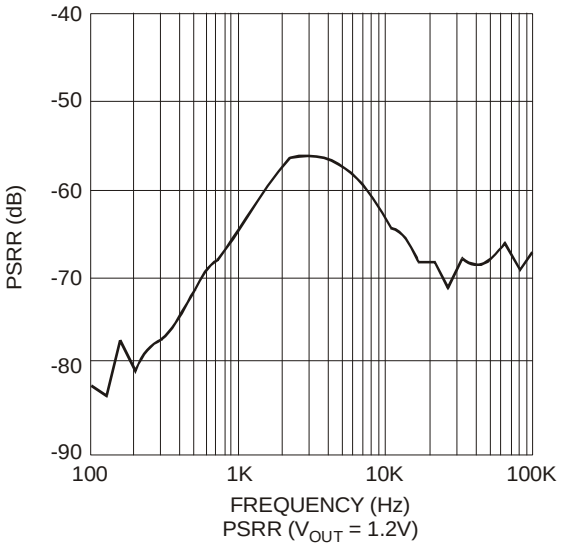
Line Regulation



Load Regulation



Current LImit vs. Temperature



PSRR (V_{OUT} = 1.2V)

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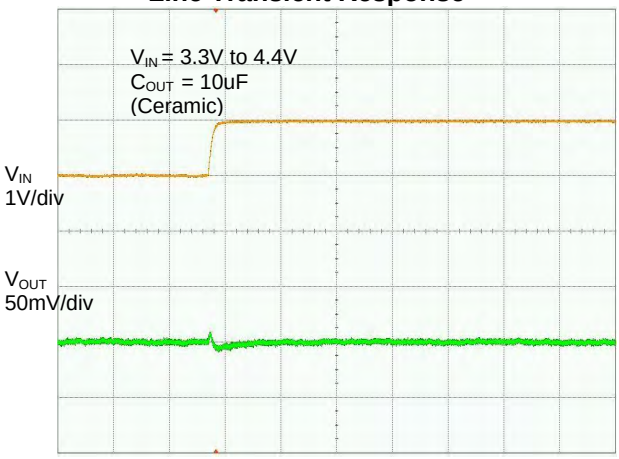
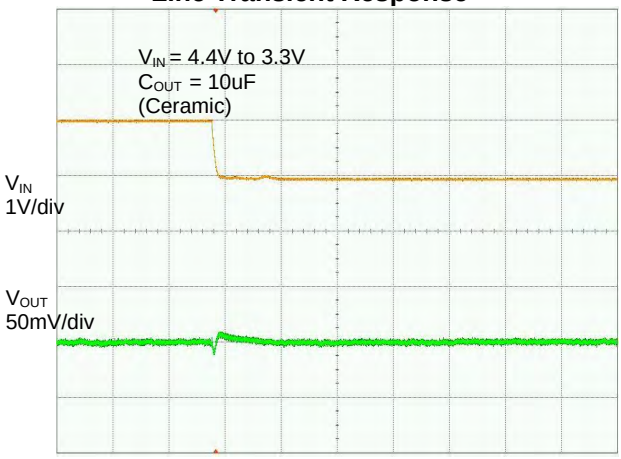
Typical Performance Characteristics (cont.)

Line Transient Response



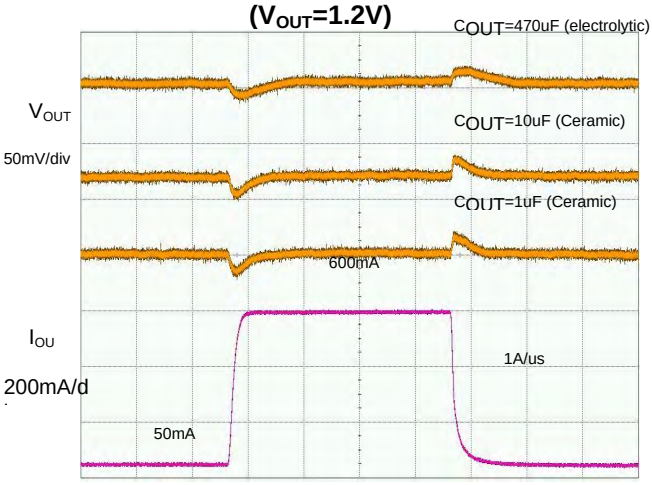
Time (50µs/div)

Line Transient Response



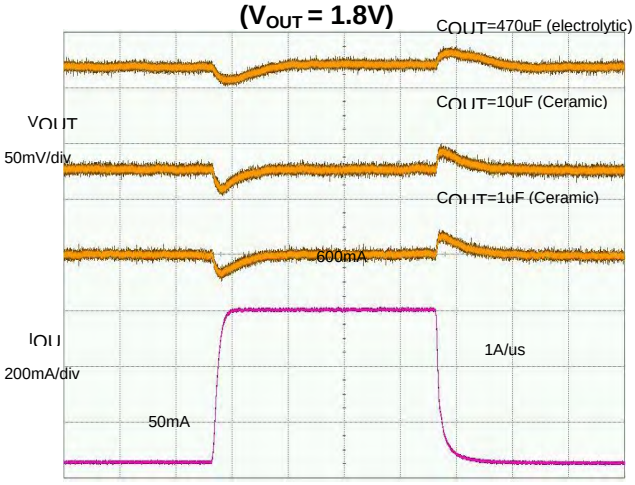
Time (50µs/div)

Output Load Transient Response (V_{OUT}=1.2V)



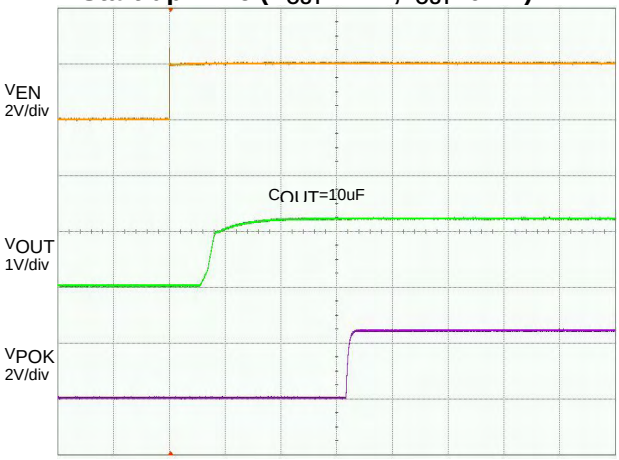
Time (100µs/div)

Output Load Transient Response (V_{OUT} = 1.8V)



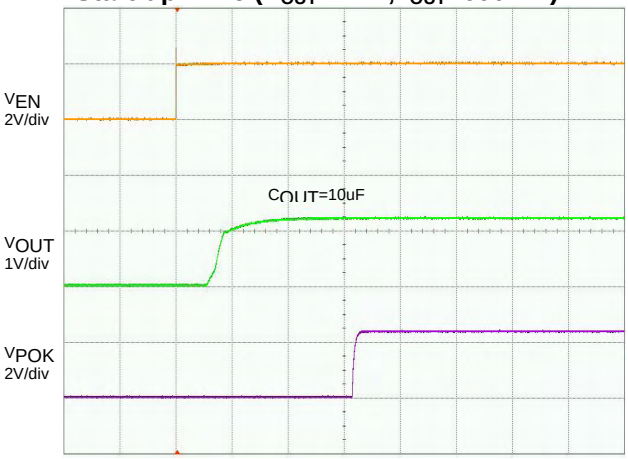
Time (100µs/div)

Start-up Time (V_{OUT}=1.2V, I_{OUT}=0.1A)



Time (50µs/div)

Start-up Time (V_{OUT}=1.2V, I_{OUT}=600mA)



Time (50µs/div)

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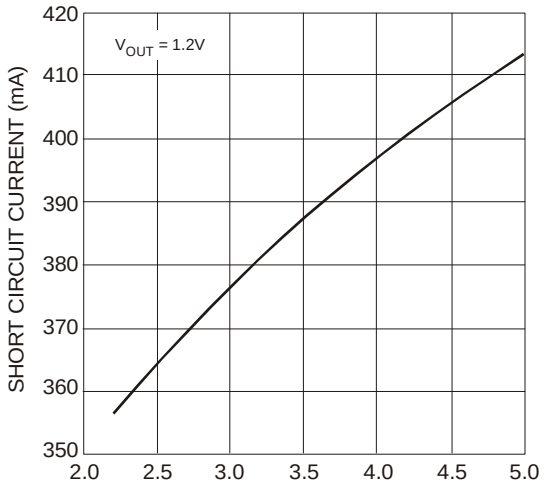
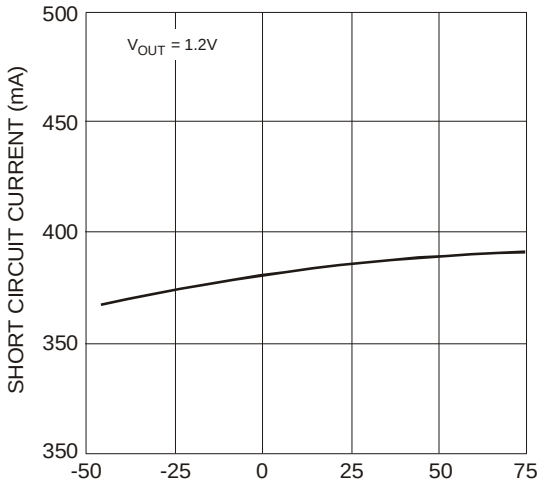
Typical Performance Characteristics (cont.)

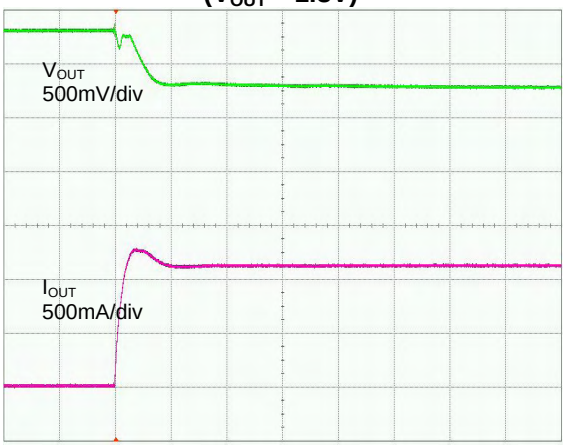


Short Circuit Current vs. Input Voltage



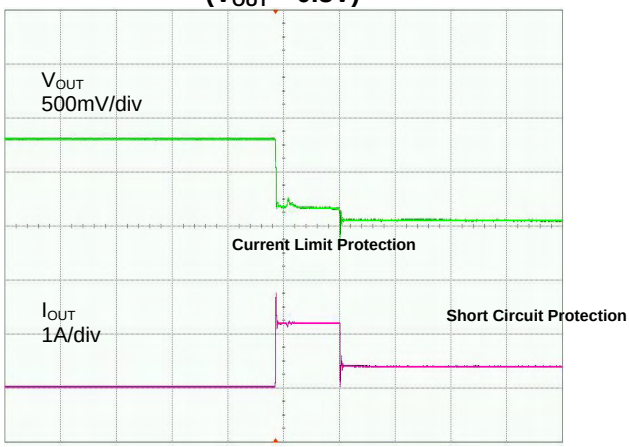
Short Circuit Current vs. Temperature

Current Limit Protection (V_{OUT} = 1.8V)



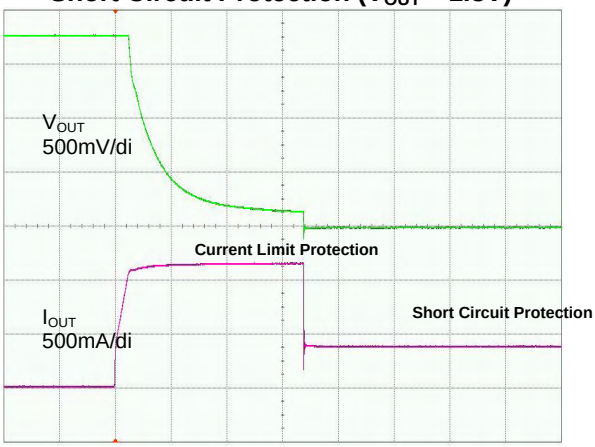
Time (50µs/div)

Current Limit & Short Circuit Protection (V_{OUT} = 0.8V)



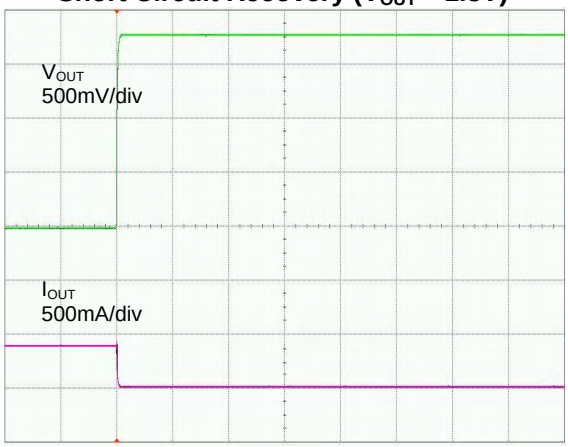
Time (500µs/div)

Short Circuit Protection (V_{OUT} = 1.8V)



Time (2ms/div)

Short Circuit Recovery (V_{OUT} = 1.8V)



Time (50µs/div)

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Application Notes

Input Capacitor

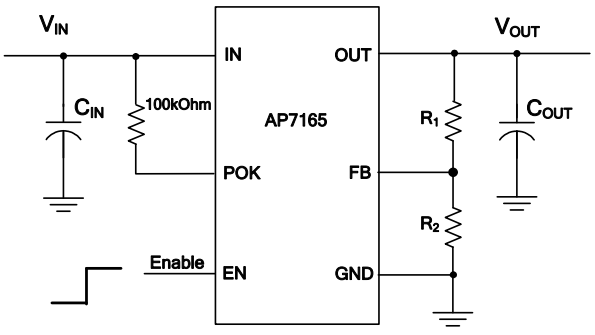
A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. A lower ESR (Equivalent Series Resistance) capacitor allows the use of less capacitance, while higher ESR type requires more capacitance. This input capacitor should be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The AP7165 is designed to have excellent transient response for most applications with a small amount of output capacitance. The AP7165 is stable for all available types and values of output capacitors ≥ 4.7μF. The device is also stable with multiple capacitors in parallel, which can be of any type of value. Additional capacitance helps to reduce undershoot and overshoot during transient. This capacitor should be placed as close as possible to OUT and GND pins for optimum performance.

Adjustable Operation

The AP7165 provides output voltage from 0.8V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Where V_{REF} = 0.8V (the internal reference voltage).

Rearranging the equation will give the following equation to find the approximate resistor divider values:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}}-1\right)$$

To maintain the stability of the internal reference voltage, R_2 needs to be kept smaller than 250kΩ.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ENABLE/SHUTDOWN Operation

The AP7165 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

POWER-OK

The Power-Ok (POK) pin is an active high open-drain output. It can be connected to any 5.5V or lower rail through an external pull-up resistor. The recommended sink current of POK pin is up to 4mA, so the pull-up resistor for POK should be in the range of 10kΩ to 1MΩ. If output voltage monitoring is not needed, the POK pin can be left floating.

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 950mA (600A min) to prevent over-current and to protect the regulator from damage due to overheating.

Short Circuit Protection

When OUT pin is short-circuited to GND or OUT pin voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 380mA. This feature protects the regulator from over-current and damage due to overheating.

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Application Notes (cont.)

Low Quiescent Current

The AP7165, consuming only around 125µA for all input range and output loading, provides great power saving in portable and low power applications.

Wide Output Range

The AP7165, with a wide output range of 0.8V to 5.0V, provides a versatile solution for many portable and low power applications.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +125°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Power Dissipation

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) x I_{OUT}$$

The AP7165 is available in the U-DFN3030-10 and SO-8EP packages, both with exposed pad, which is the primary conduction path for heat to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, to ensure the device will not overheat, it should be attached to an appropriate amount of copper PCB area.

However, the maximum power dissipation that can be handled by the device depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be approximated by the equation below:

$$P_D(max@T_A) = \frac{(+145°C - T_A)}{R_{\theta JA}}$$

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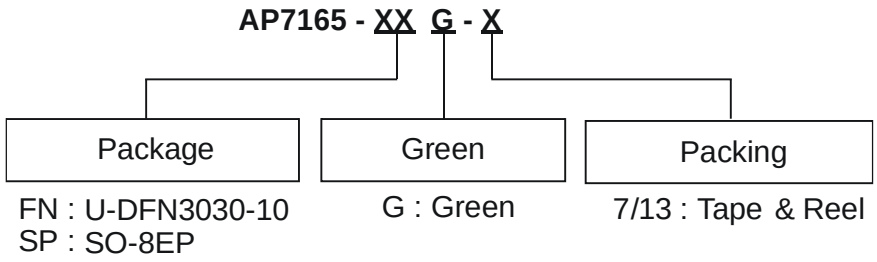
Ordering Information

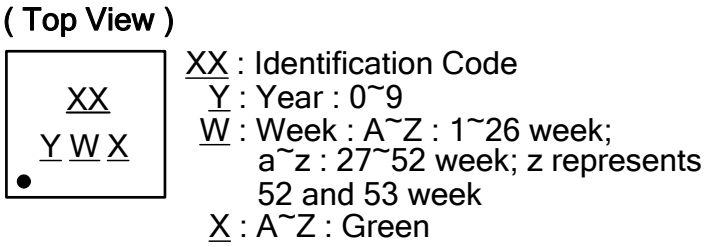


Device	Package Code	Packaging (Note 2)	Tube		7"/13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP7165-FNG-7	FN	U-DFN3030-10	NA	NA	3000/Tape & Reel	-7
AP7165-SPG-13	SP	SO-8EP	NA	NA	2500/Tape & Reel	-13

Notes: 6. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

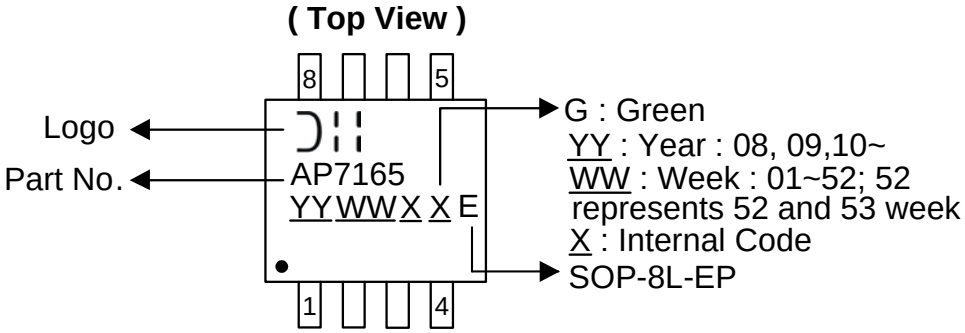
Marking Information

(1) U-DFN3030-10



Part Number	Package	Identification Code
AP7165	U-DFN3030-10	B2

(2) SO-8EP



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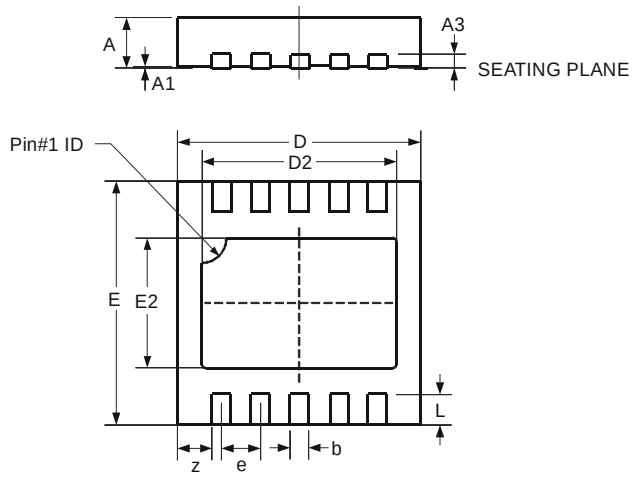
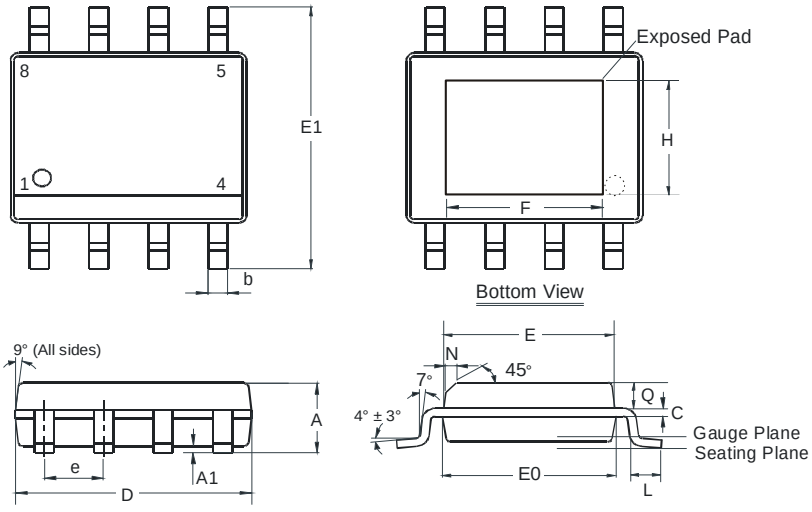
Package Outline Dimensions

(1) Package Type: U-DFN3030-10



U-DFN3030-10			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	—	—	0.50
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

(2) Package Type: SO-8EP



SO-8EP (SOP-8L-EP)			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Notes: 7. All dimensions are in millimeters. Angles are in degrees.
8. Coplanarity applies to the exposed heat sink slug as well as the terminals.

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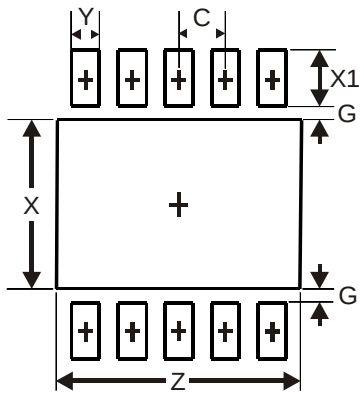
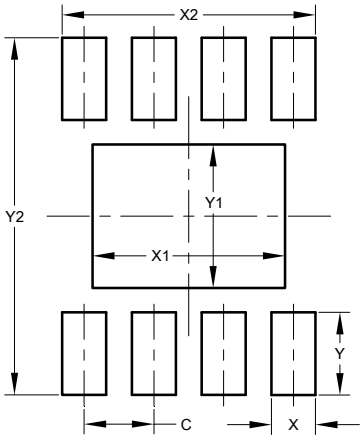
Suggested Pad Layout

(1) Package Type: U-DFN3030-10



Dimensions	Value (in mm)
Z	2.60
G	0.15
X	1.80
X1	0.60
Y	0.30
C	0.50

(2) Package Type: SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

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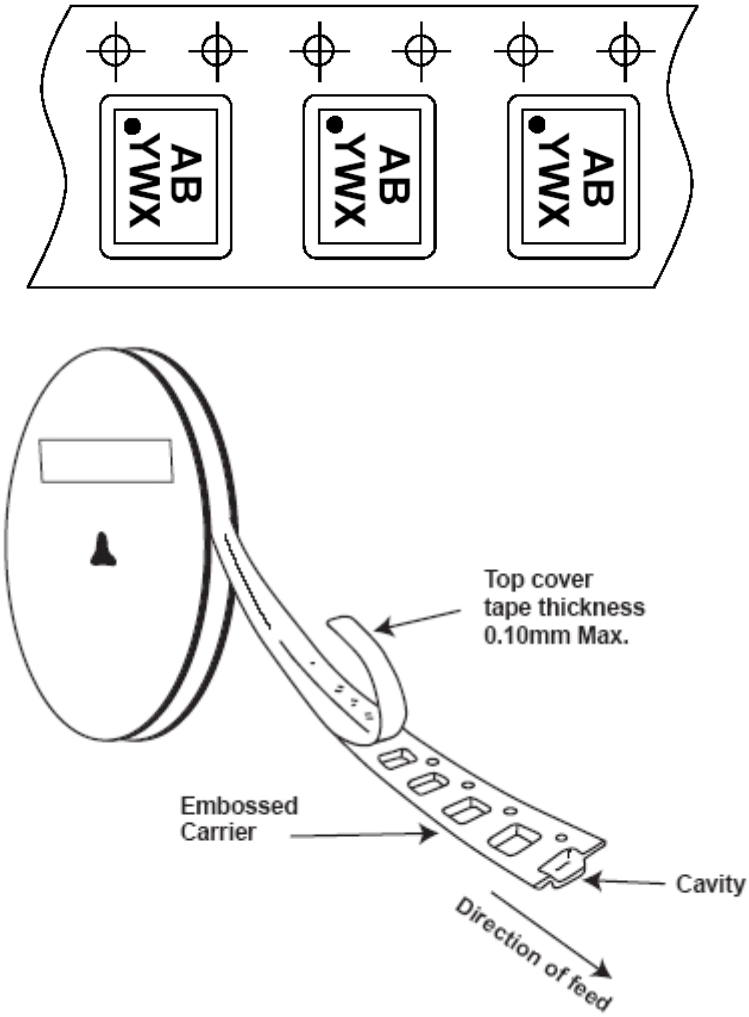
Taping Orientation (Note 9)

For U-DFN3030-10



Notes: 9.The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf.

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