3A ULTRA LOW-DROPOUT LINEAR REGULATOR WITH ENABLE

Description

The AP7176B is a 3.0A ultra low-dropout (LDO) linear regulator that features an enable input and a power-good output.

The enable input and power-good output allow users to configure power management solutions that can meet the sequencing requirements of FPGAs, DSPs, and other applications with different startup and power-down requirements.

The AP7176B features two supply inputs, for power conversion supply and control. With the separation of the control and the power input very low dropout voltages can be reached and power dissipation is reduced.

A precision reference and feedback control deliver 1.5% accuracy over load, line, and operating temperature ranges.

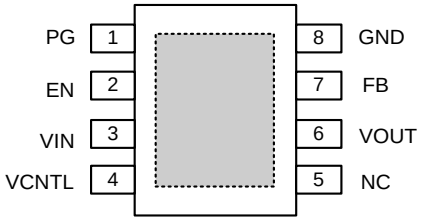
The AP7176B is available in SO-8EP, MSOP-8EP and U-DFN3030-10 packages with an exposed PAD to reduce the junction to case resistance and extend the temperature range it can be used in.

Features

- V_{IN} Range: 1.2V to 3.65V, V_{CNTL} 3.0V to 5.5V
- Adjustable Output Voltage
- Continuous Output Current I_{OUT} = 3A
- Fast Transient Response
- Power-On-Reset Monitoring on V_{CNTL} and V_{IN}
- Internal Soft-Start
- Stable with Low ESR MLCC Capacitors
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

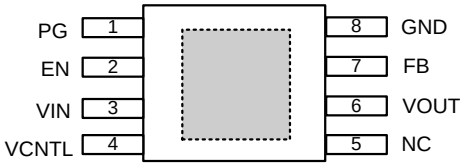
Pin Assignments

(Top View)



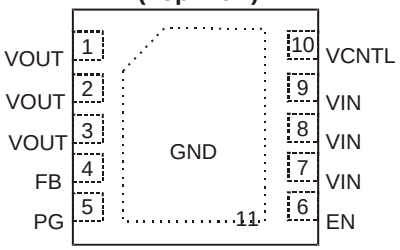
SO-8EP

(Top View)



MSOP-8EP

(Top View)



U-DFN3030-10

= PAD
(connected to ground plane for better heat dissipation)

Applications

- Notebooks
- PCs
- Netbooks
- Wireless communication
- Servers
- Motherboards
- Dongles
- Front side bus VTT (1.2V/3.3A)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

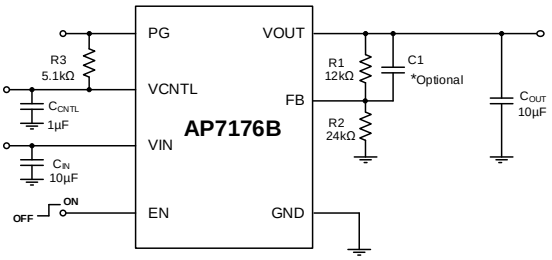
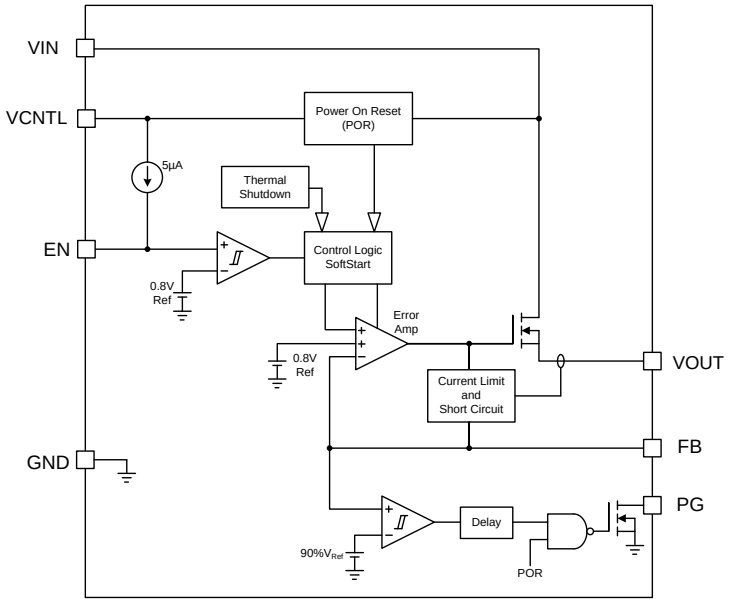


Figure 1. Typical Application Circuit

Pin Descriptions

Pin Name	Pin Number			Function
	SO-8EP	MSOP-8EP	U-DFN3030-10	
PG	1	1	5	Power-Good. Output open drain to indicate the status of V_{OUT} via monitoring the FB pin. This pin is pulled low when the voltage is outside the limits, during thermal shutdown and if either V_{CNTL} or V_{IN} goes below their thresholds.
EN	2	2	6	Enable pin. Driving this pin low will disable the part. When left floating an internal current source will pull this pin high and enable it.
VIN	3	3	7, 8, 9	Power input pin for current supply. Connect a decoupling capacitor (≥ 10µF) as close as possible to the pin for noise filtering.
VCNTL	4	4	10	BIAS supply for the controller, recommended 5V. Connect a decoupling capacitor (≥ 1µF) as close as possible to the pin for noise filtering.
NC	5	5	—	No connection
VOUT	6	6	1, 2, 3	Power output pin
FB	7	7	4	Feedback to set the output voltage via an external resistor divider between VOUT and GND
GND	8	8	11	Ground
PAD	EP	EP	EP	Exposed pad connected to GND for good thermal conductivity.

Functional Block Diagram



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Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 to +4.0	V
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 to +7.0	V
V_{OUT}	VOUT to GND Voltage	-0.3 to V_{IN} +0.3	V
—	PG to GND Voltage	-0.3 to +7.0	V
—	EN, FB to GND Voltage	-0.3 to V_{CNTL} +0.3	V
P_D	Power Dissipation (SO-8EP)	1.7	W
	Power Dissipation (MSOP-8EP)	1.5	
	Power Dissipation (U-DFN3030-10)	1.9	
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	+260	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Range	Unit
V_{CNTL}	VCNTL Supply Voltage		3.0 to 5.5	V
V_{IN}	VIN Supply Voltage		1.2 to 3.65	V
V_{OUT}	VOUT Output Voltage (when V_{CNTL} - V_{OUT} > 1.9V)		0.8 to V_{IN} – V_{DROP}	V
I_{OUT}	VOUT Output Current		0 to 3	A
C_{OUT}	VOUT Output Capacitance	I_{OUT} = 3A at 25% nominal V_{OUT}	8 to 1100	µF
		I_{OUT} = 2A at 25% nominal V_{OUT}	8 to 1700	
		I_{OUT} = 1A at 25% nominal V_{OUT}	8 to 2400	
E_{SRCOUT}	ESR of VOUT Output Capacitor		0 to 200	mΩ
T_A	Ambient Temperature		-40 to +85	°C
T_J	Junction Temperature		-40 to +125	°C

Electrical Characteristics (Specifications apply over V_{CNTL} = 5V, V_{IN} = 1.8V, V_{OUT} = 1.2V and T_A = -40°C to +85°C, typical values @T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	AP7176B			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VCNTL}	VCNTL Supply Current	EN = V_{CNTL}, I_{OUT} = 0A	—	1.0	1.5	mA
I_{SD}	VCNTL Supply Current at Shutdown	EN = GND	—	15	30	µA
	VIN Supply Current at Shutdown	EN = GND, V_{IN} = 3.65V	—	—	1	µA
POWER-ON RESET (POR)						
$V_{POR_Rising\ (VCNTL)}$	Rising VCNTL POR Threshold	—	2.50	2.70	2.95	V
$V_{POR_Hysteresis\ (VCNTL)}$	VCNTL POR Hysteresis	—	—	0.4	—	V
$V_{POR_Rising\ (VIN)}$	Rising VIN POR Threshold	—	0.8	0.9	1.0	V
$V_{POR_Hys\ (VIN)}$	VIN POR Hysteresis	—	—	0.5	—	V

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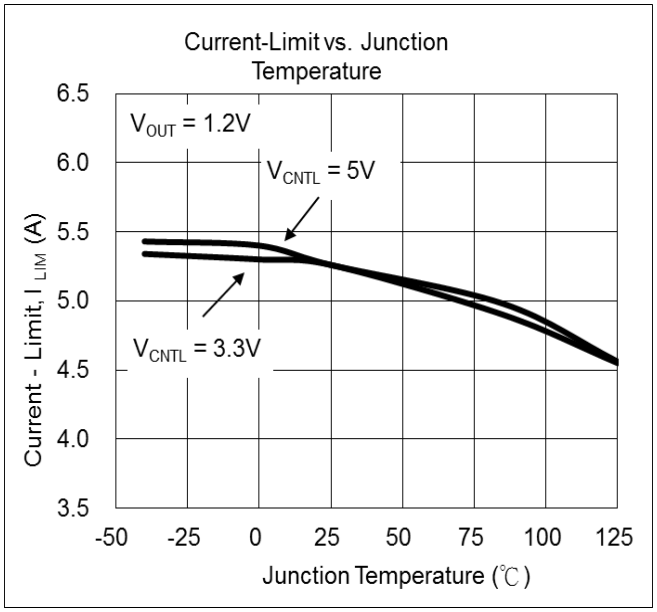
Electrical Characteristics (continued) (Specifications apply over V_{CNTL} = 5V, V_{IN} = 1.8V, V_{OUT} = 1.2V and T_A = -40°C to +85°C, typical values @T_A = +25°C, unless otherwise specified.)

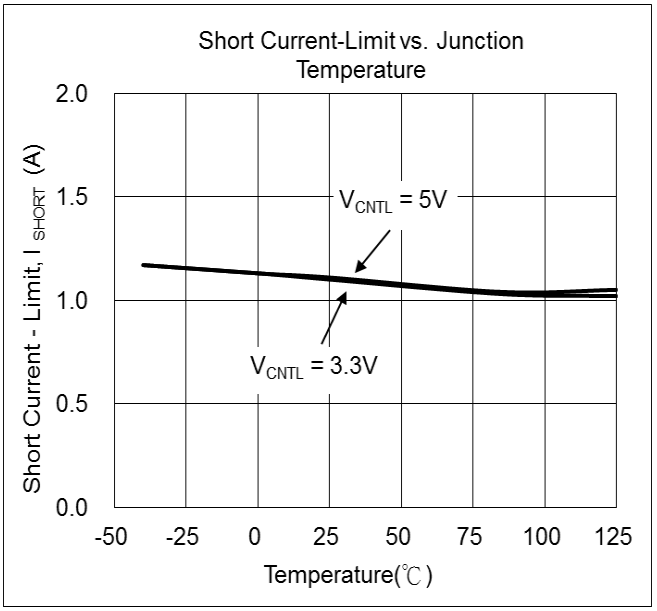
Symbol	Parameter	Conditions			AP7176B Min	AP7176B Typ	AP7176B Max	Unit
OUTPUT VOLTAGE								
V_{REF}	Reference Voltage	FB = V_{OUT}			—	0.8	—	V
	Output Voltage Accuracy	V_{CNTL} = 3.0V to 5.5V, I_{OUT} = 0A to 3A T_J = -40°C to +125°C			-1.5	—	+1.5	%
	Load Regulation	I_{OUT} = 0A to 3A			—	0.06	0.25	%
	Line Regulation	I_{OUT} = 10mA, V_{CNTL} = 3.0V to 5.5V			-0.15	—	+0.15	%/V
	VOUT Pull-Low Resistance	V_{CNTL} = 3.3V, V_{EN} = 0V, V_{OUT} < 0.8V			—	10	—	Ω
	FB Input Current	V_{FB} = 0.8V			-100	—	+100	nA
DROPOUT VOLTAGE								
V_{DROP}	VIN-to-VOUT Dropout Voltage (Note 5)	V_{CNTL} = 5.0V I_{OUT} = 3A	V_{OUT} = 2.5V	T_J = +25°C	—	0.33	0.38	V
				T_J = -40°C to +125°C	—	—	0.53	
			V_{OUT} = 1.8V	T_J = +25°C	—	0.31	0.36	
				T_J = -40°C to +125°C	—	—	0.50	
			V_{OUT} = 1.2V	T_J = +25°C	—	0.30	0.35	
				T_J = -40°C to +125°C	—	—	0.48	
I_{LIM}	Current-Limit Level	T_J = +25°C, V_{OUT} = 80% $V_{NOMINAL}$			4.5	5.7	6.7	A
		T_J = -40°C to +125°C			4.2	—	—	A
PROTECTIONS								
I_{SHORT}	Short Current-Limit Level	V_{FB} < 0.2V			—	1.1	—	A
T_{SD}	Thermal Shutdown Temperature	T_J rising			—	+170	—	°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	—			—	+50	—	°C
ENABLE AND SOFT-START								
$EN_{_HI}$	EN Logic High Threshold Voltage	V_{EN} rising			0.5	0.8	1.1	V
$EN_{_Hys}$	EN Hysteresis	—			—	0.1	—	V
$I_{_EN}$	EN Pull-High Current	EN = GND			—	5	—	µA
t_{SS}	Soft-Start Interval	—			0.3	0.6	1.2	ms
$t_{_DELAY}$	Turn-On Delay	From being enabled to V_{OUT} rising 10%			200	350	500	µs
POWER-GOOD AND DELAY								
V_{THPG}	Rising PG Threshold Voltage	V_{FB} rising			90	92	95	%
V_{PG_Hys}	PG Threshold Hysteresis	—			—	8	—	%
V_{PG_Low}	PG Pull-Low Voltage	PG sinks 5mA			—	0.25	0.4	V
t_{PG_Deb}	PG Debounce Interval	V_{FB} < falling PG voltage threshold			—	10	—	µs
$t_{_PGDEL}$	PG Delay Time	From V_{FB} = V_{THPG} to rising edge of the V_{PG}			1	2	4	ms
THERMAL CHARACTERISTIC								
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-8EP (Note 6)			—	70	—	°C/W
		MSOP-8EP (Note 7)			—	80	—	°C/W
		U-DFN3030-10 (Note 6)			—	60	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	SO-8EP (Note 6)			—	30	—	°C/W
		MSOP-8EP (Note 7)			—	30	—	°C/W
		U-DFN3030-10 (Note 6)			—	20	—	°C/W

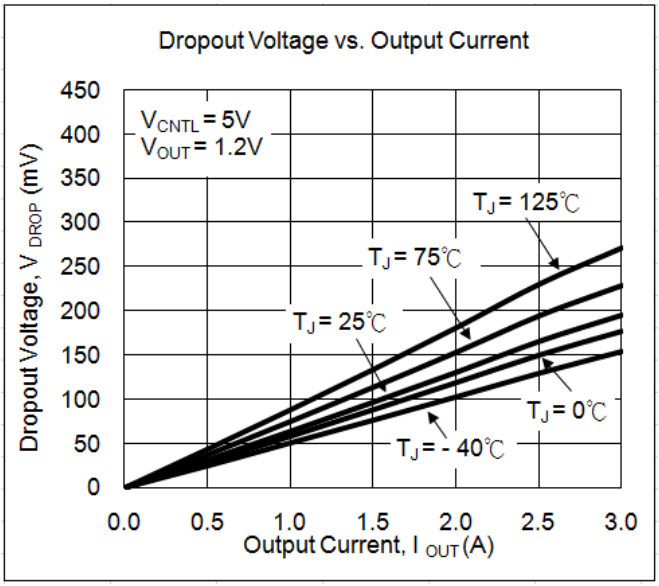
Notes:
5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
6. Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
7. Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

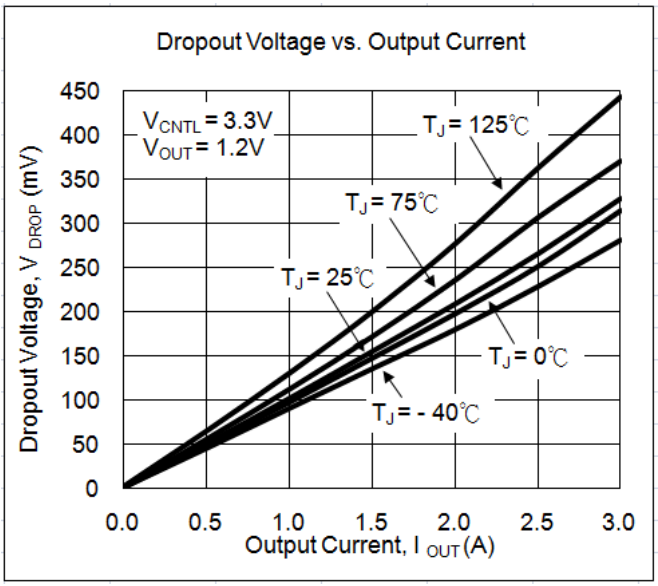
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Typical Characteristics



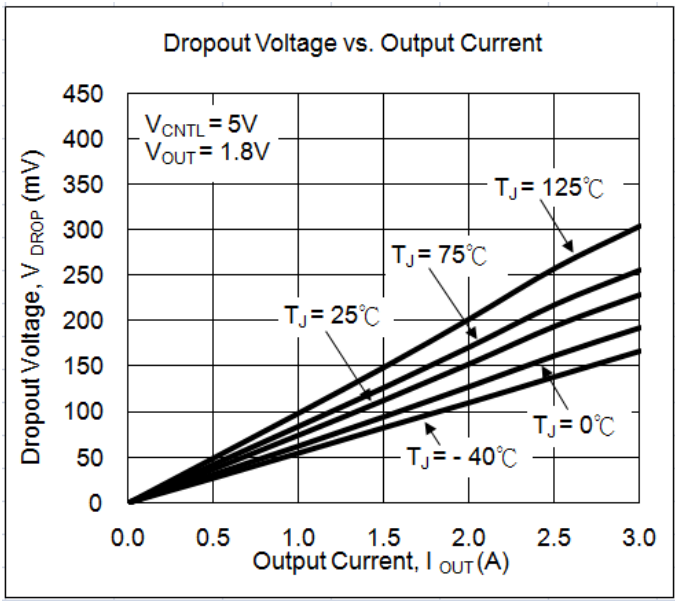


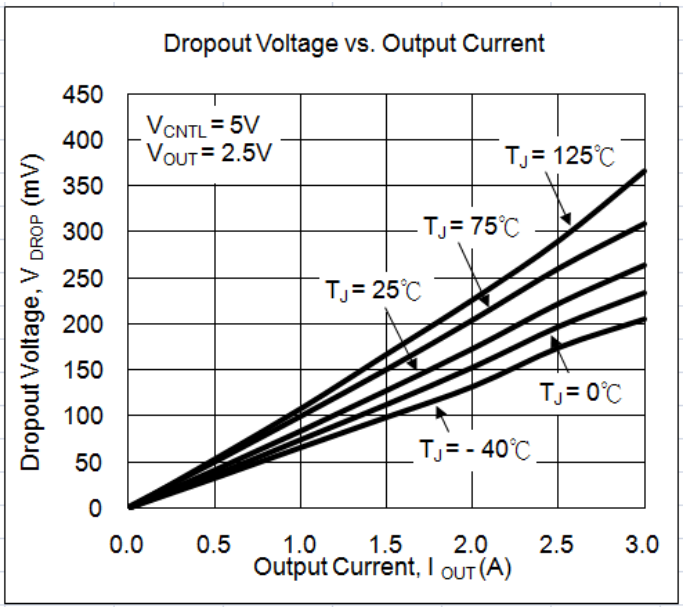


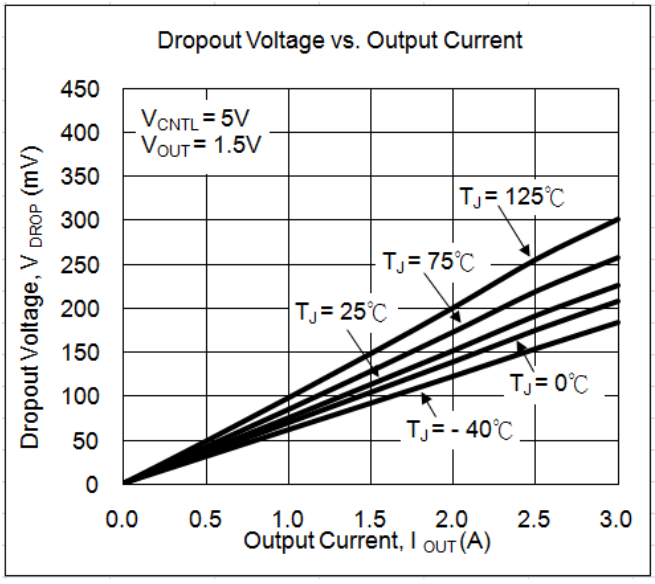


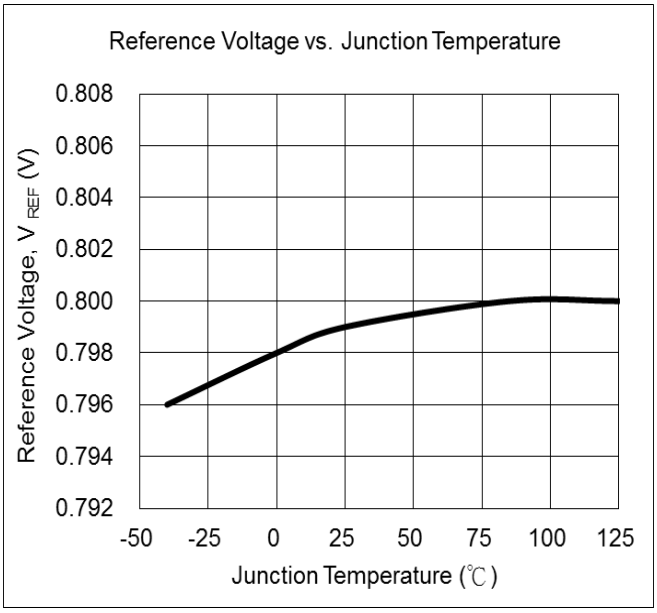
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Typical Characteristics (continued)



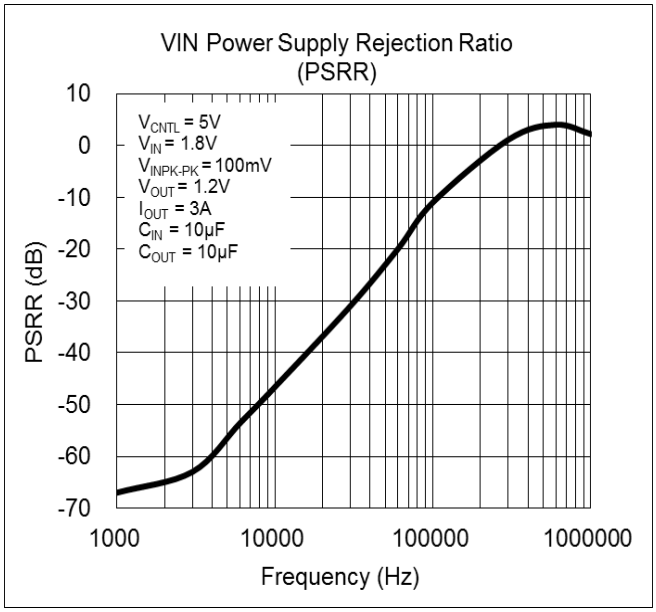


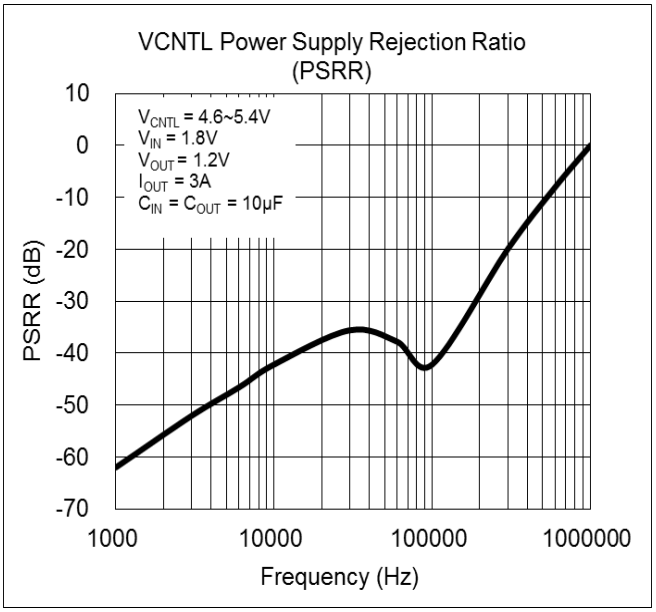




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Typical Characteristics (continued)

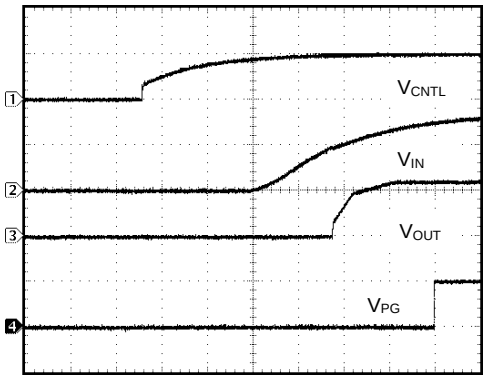




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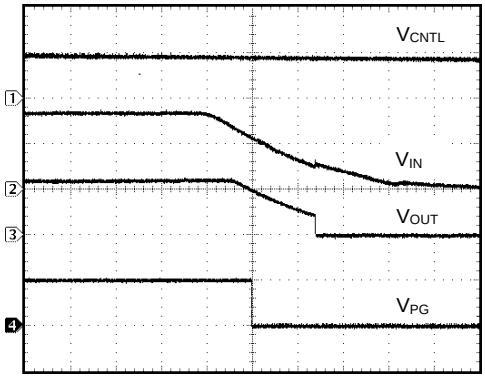
Operating Waveforms (Test Conditions V_{IN} = 1.8V, V_{CNTL} = 5V, V_{OUT} 1.2V, T_A = +25°C unless otherwise specified.)

Power On



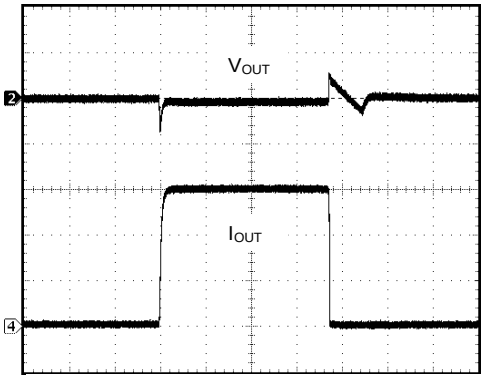
C_{OUT} =10µF, C_{IN} =10µF, R_L = 0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 2ms/Div

Power Off



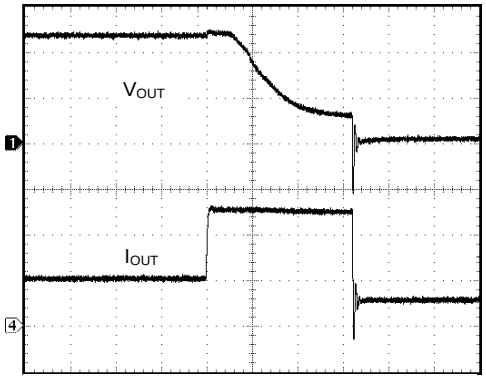
C_{OUT} = 10µF, C_{IN} =10µF, R_L = 0.4Ω
CH1: V_{CNTL}, 5V/Div, DC
CH2: V_{IN}, 1V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 2ms/Div

Load Transient Response



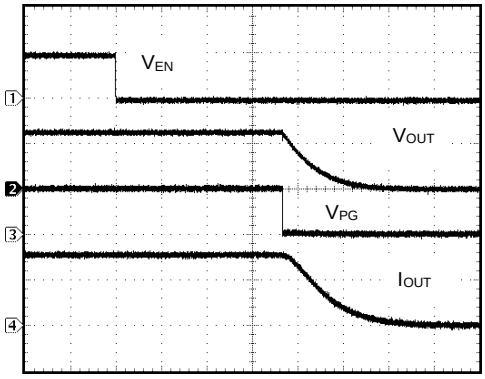
I_{OUT} = 10mA to 3A to10mA (rise / fall time = 1µs)
C_{OUT} = 10µF, C_{IN} = 10µF
CH2: V_{OUT}, 50mV/Div, AC
CH4: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Overcurrent Protection



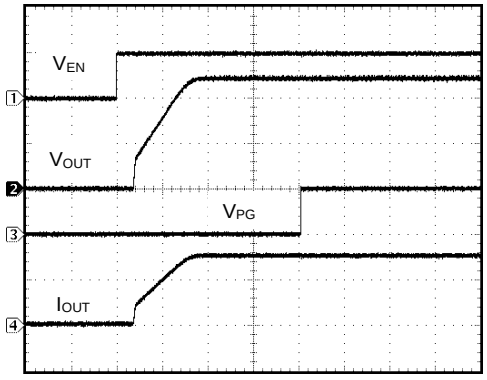
C_{OUT} = 10µF, C_{IN} = 10µF, I_{OUT} = 2A to 5.6A
CH1: V_{OUT}, 0.5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 0.2ms/Div

Shutdown



C_{OUT} = 10µF, C_{IN} = 10µF, R_L = 0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PG}, 5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 4µs/Div

Enable



C_{OUT} = 10µF, C_{IN} = 10µF, R_L = 0.4Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PG}, 5V/Div, DC
CH4: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

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Application Information

Power-Good and Delay

AP7176B monitors the feedback voltage V_{FB} on the FB pin. An internal delay timer is started after the PG voltage threshold (V_{THPG}) on the FB pin is reached. At the end of the delay time an internal nMOS of the PG is turned off to indicate that the power at the output is good (PG). This monitoring function is continued during operation and if V_{FB} falls 8% (typ) below V_{THPG}, the nMOS of the PG is turned on after a delay time of typical 10µs to avoid oscillating of the PG signal.

Power-On Reset

AP7176B monitors both supply voltages, V_{CNTL} and V_{IN} to ensure operation as intended. A Soft-Start process is initiated after both voltages exceed their POR threshold during power on. During operation the POR component continues to monitor the supply voltage and pulls the PG low to indicate an out of regulation supply. This function will engage without regard to the status of the output.

Soft-Start

AP7176B incorporates an internal Soft-Start function. The output voltage rise is controlled to limit the current surge during startup. The typical Soft-Start time is 0.6ms

Current-Limit Protection

AP7176B monitors the current flow through the nMOS and limits the maximum current to avoid damage to the load and AP7176B during overload conditions.

Short-Circuit Current-Limit Protection

AP7176B incorporates a current-limit function to reduce the maximum current to 1.1A (typ) when the voltage at FB falls below 0.2V (typ) during an overload or short-circuit situation.

During startup period, this function is disabled to ensure successful heavy load startup.

Enable Control

If the enable pin (EN) is left open, an internal current source around 5µA pulls the pin up and enables the AP7176B. This will reduce the bill of material saving an external pullup resistor. Driving the enable pin low disables the device. Driving the pin high subsequently initiates a new Soft-Start cycle.

Output Voltage Regulation

Output Voltage is set by resistor divider from V_{OUT} via FB pin to GND. Internally V_{FB} is compared to a 0.8V temperature compensated reference voltage and the nMOS pass element regulates the output voltage while delivering current from VIN to VOUT.

Setting the Output Voltage

A resistor divider connected to FB pin programs the output voltage.

$$V_{OUT} = V_{REF} * \left(1 + \frac{R1}{R2}\right) V$$

R1 is connected from VOUT to FB with Kelvin sensing connection. R2 is connected from FB to GND. To improve load transient response and stability, a bypass capacitor can be connected in parallel with R1. (optional in typical application circuit)

Power Sequencing

AP7176B requires no specific sequencing between VIN and VCNTL. However, care should be taken to avoid forcing VOUT for prolonged times without the presence of VIN. Conduction through internal parasitic diode (from VOUT to VIN) could damage AP7176B.

Thermal Shutdown

The PCB layout and power requirements for AP7176B under normal operation condition should allow enough cooling to restrict the junction temperature to +125°C. The packages for AP7176B have an exposed PAD to support this. These packages provide better connection to the PCB and thermal performance. Refer to the *Layout Consideration*.

If AP7176B junction temperature reaches +170°C a thermal protection block disables the nMOS pass element and lets the part cool down. After its junction temperature drops by 50°C (typ), a new Soft-Start cycle will be initiated. A new thermal protection will start, if the load or ambient conditions continue to raise the junction temperature to +170°C. This cycle will repeat until normal operation temperature is maintained again.

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Application Information (continued)

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The ESR (equivalent series resistance) and capacitance drives the selection. Care needs to be taken to cover the entire operating temperature range.

The output capacitor can be an Ultra-Low-ESR ceramic chip capacitor or a low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor.

C_{OUT} is used to improve the output stability and reduces the changes of the output voltage during load transitions. The slew rate of the current sensed via the FB pin in AP7176B is reduced. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors.

It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps it is recommended to utilize an input capacitor (C_{IN}). As with the output capacitor the following are acceptable, Ultra-Low-ESR ceramic chip capacitor or low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor. Typically, it is recommended to utilize a capacitance of at least 10µF to avoid output voltage drop due to reduced input voltage. The value can be lower if V_{IN} changes are not critical for the application.

Layout Consideration

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. No other application circuit is connected within the loop. Avoid using vias within ground loop. If vias must be used, multiple vias should be used to reduce via inductance.

The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance.

Wide trace should be used for large current paths from VIN to VOUT, and load circuit.

Place the R1, R2, and C1 (optional) near the LDO as close as possible to avoid noise coupling.

R2 is placed close to device ground. Connect the ground of the R2 to the GND pin by using a dedicated trace.

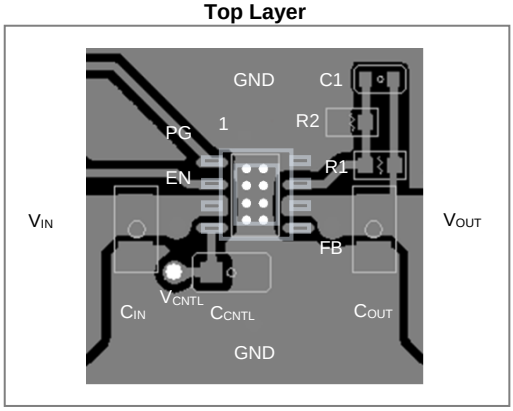
Connect the pin of the R1 directly to the load for Kelvin sensing.

No high current should flow through the ground trace of feedback loop and affect reference voltage stability.

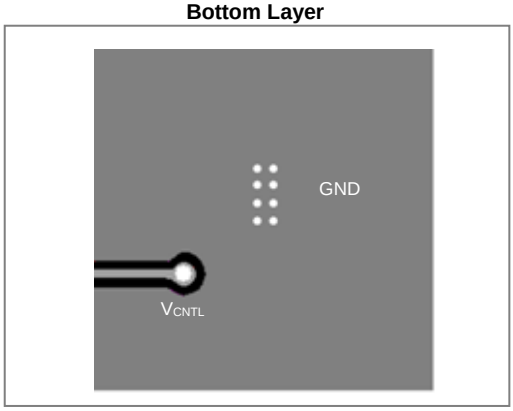
For the packages with exposed pads, heat sinking is accomplished using the heat spreading capability of the PCB and its copper traces. Suitable PCB area on the top layer and thermal vias (0.3mm drill size with 1mm spacing, 4 to 8 vias at least) to the VIN power plane can help to reduce device temperature greatly.

Reference Layout Plots:

Top Layer

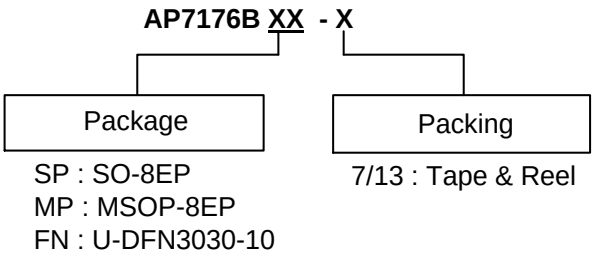


Bottom Layer



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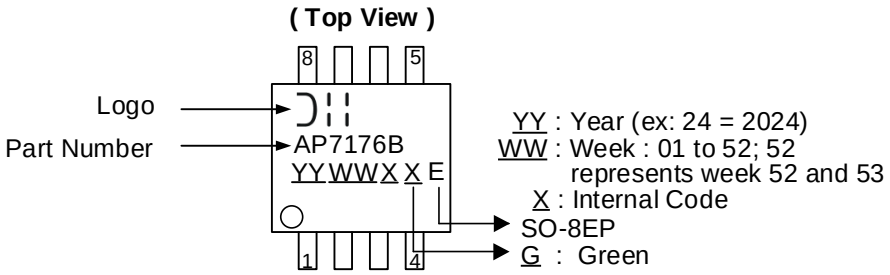
Ordering Information



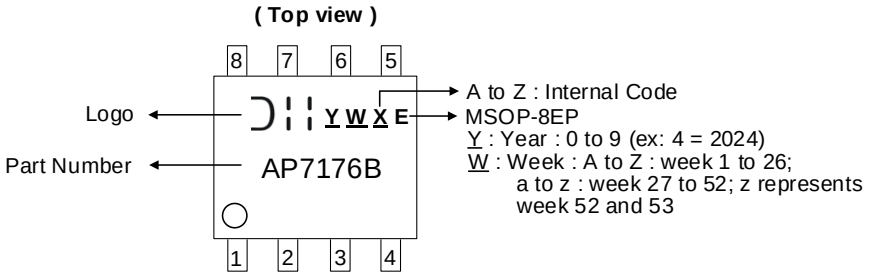
Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7176BSP-13	SP	SO-8EP	2500	Tape & Reel
AP7176BMP-13	MP	MSOP-8EP	2500	Tape & Reel
AP7176BFN-7	FN	U-DFN3030-10	3000	Tape & Reel
AP7176BFN-13	FN	U-DFN3030-10	3000	Tape & Reel

Marking Information

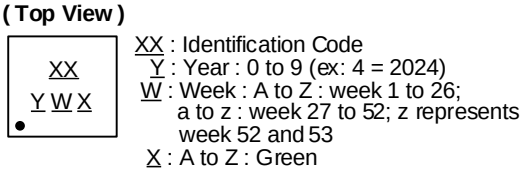
(1) SO-8EP



(2) MSOP-8EP



(3) U-DFN3030-10



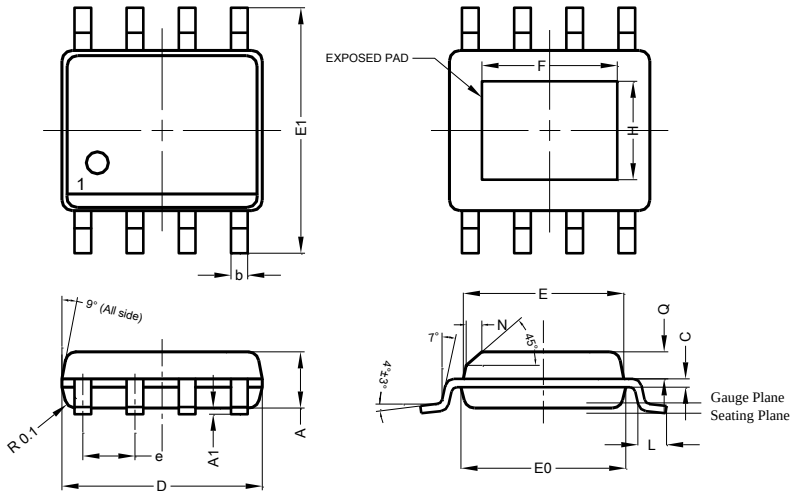
Orderable Part Number	Package	Identification Code
AP7176BFN-7	U-DFN3030-10	A7
AP7176BFN-13	U-DFN3030-10	A7

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Package Outline Dimensions

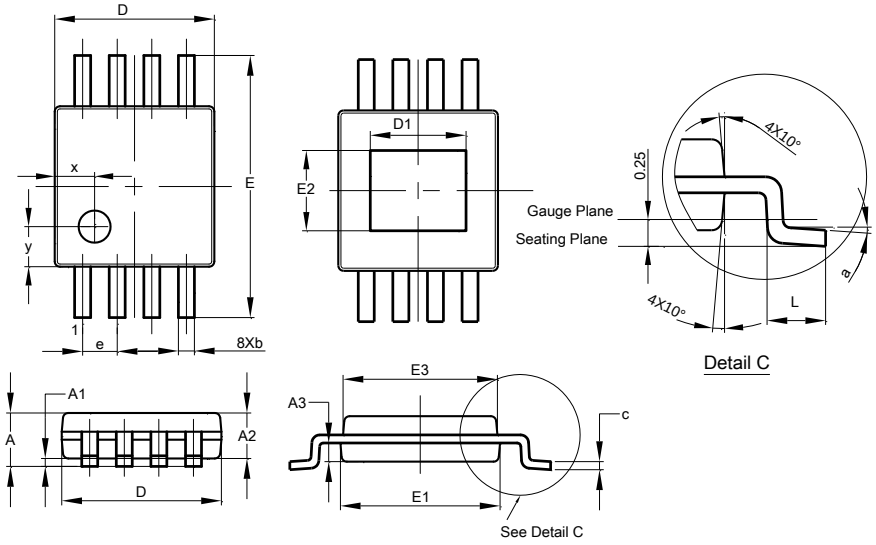
Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

MSOP-8EP



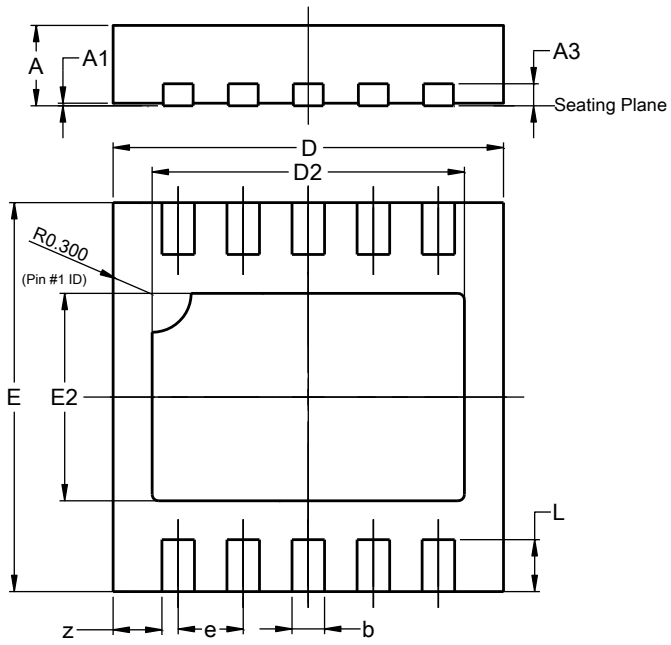
MSOP-8EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

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Package Outline Dimensions (continued)

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U-DFN3030-10

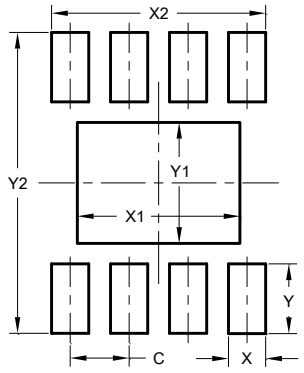


U-DFN3030-10			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
e	--	--	0.50
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



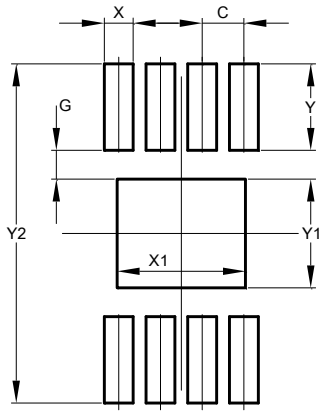
Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

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Suggested Pad Layout (continued)

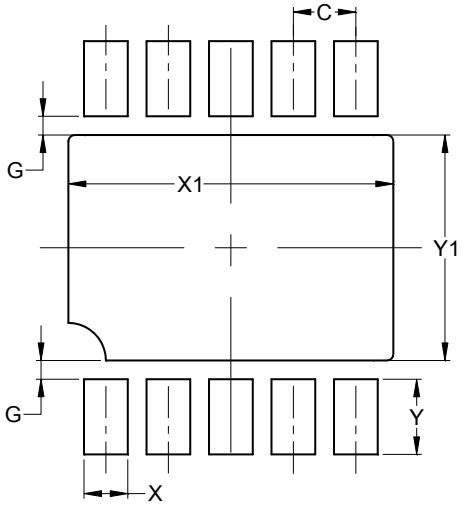
Please see http://www.diodes.com/package-outlines.html for the latest version.

MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

U-DFN3030-10



Dimensions	Value (in mm)
C	0.50
G	0.15
X	0.35
X1	2.60
Y	0.60
Y1	1.80

Mechanical Data

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals:
  - SO-8EP/MSOP-8EP: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
  - U-DFN3030-10: Finish – NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 e4
- Weight:
  - SO-8EP: 0.081 grams (Approximate)
  - MSOP-8EP: 0.026 grams (Approximate)
  - U-DFN3030-10: 0.01 grams (Approximate)

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