Description

The AP7369Q series is a wide input-voltage range (45V), low quiescent current (2.1μA), low-dropout linear regulator (LDO) able to provide 150mA load current.

The device provides a very fast response against line voltage transient and load current transient, ensuring no overshoot voltage occurs during startup and short-circuit recovery. It also features integrated short-circuit and thermal-shutdown protection.

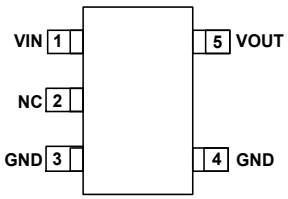
The AP7369Q has 2.5V, 3.3V, and 5.0V fixed output voltage versions. It is available in the SOT25 and SOT223 packages.

Features

- Wide Input-Voltage Range: 3V to 45V
- Maximum Output Current: 150mA
- Low Dropout Voltage:
  V_{DROP} = 35mV @ I_{OUT} = 10mA (typ)
  V_{DROP} = 350mV @ I_{OUT} = 100mA (typ)
- Low Quiescent Current: 2.1μA (typ)
- Fixed Output Voltages: 2.5V, 3.3V and 5.0V
- High Output Voltage Accuracy: ±2%
- High PSRR: 85dB@1kHz
- Excellent Line/Load Regulation
- Thermal Shutdown Function
- Short-Current Protection Function
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP7369Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

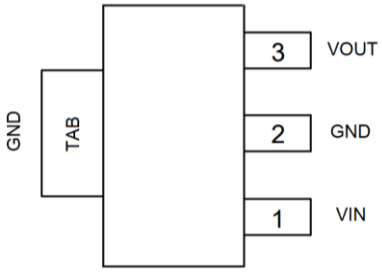
Pin Assignments

(Top View)



SOT25

(Top View)



SOT223

Applications

- Powering MCUs and CAN/LIN transceivers
- Automotive head units
- EV and HEV battery management systems
- Body control modules
- Transmission control units (TCUs)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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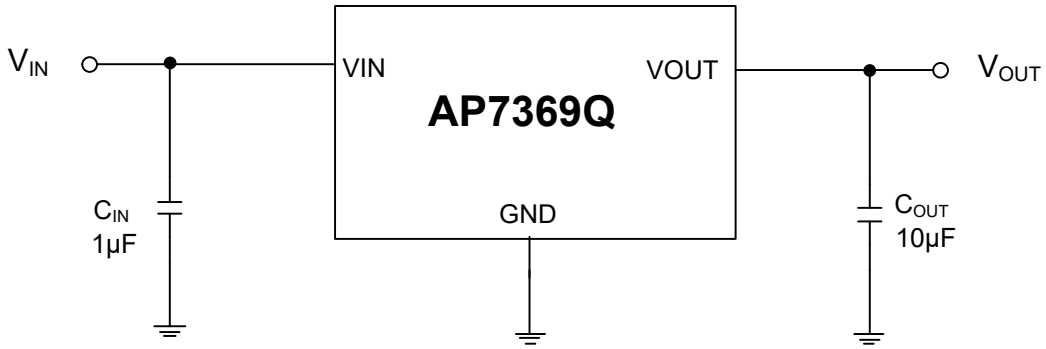
Typical Applications Circuit



Pin Descriptions

Pin Number		Pin Name	Function
SOT25	SOT223		
1	1	VIN	Input voltage
2	—	NC	Not connected internally, recommend connect to GND to maximize PCB copper for thermal dissipation.
3, 4	2	GND	Ground
5	3	VOUT	Regulated output voltage
—	TAB	Expose Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone.

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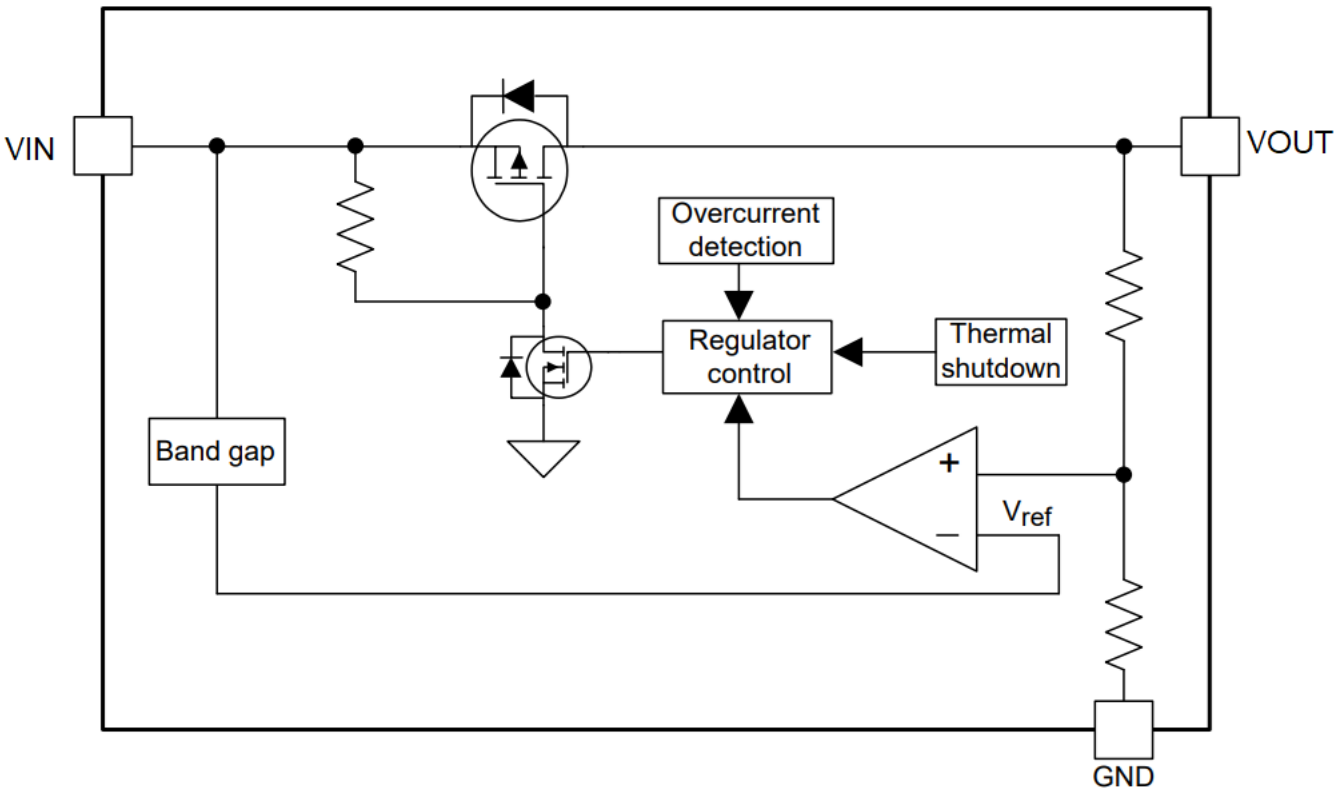
Functional Block Diagram



Absolute Maximum Ratings (Notes 4 and 5)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Input Voltage	-0.3 to 55	V
V_{OUT}	Regulated Output Voltage	-0.3 to 6	V
V_{EN}	EN to GND	-0.3 to 55	V
I_{OUT}	Output Current	Internally Limited	mA
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
T_J	Operating Junction Temperature	+150	°C
T_A	Operating Ambient Temperature	-40 to +125	°C
T_{STG}	Storage Temperature Range	-40 to +150	°C
CDM	ESD (Charged Device Model)	±1.5	kV
HBM	ESD (Human Body Model)	3	kV

Notes: 4. Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period can affect device reliability.

5. Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch × 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

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Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Input Voltage	3.0	—	45	V
V_{OUT}	Output Voltage	—	—	5	V
T_J	Operating Junction Temperature	-40	—	+150	°C
C_{IN}	Input Capacitor	—	1	—	μF
C_{OUT}	Output Capacitor	1	—	100	μF
ESR_{CO}	Output ESR Requirements	0.0001	—	2	Ω

Package Thermal Information (Note 5)

THERMAL METRIC		SOT25	SOT233	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	159.89	104.59	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	64.45	89.11	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	89.72	52.3	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	19.49	32.44	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	88.86	67.12	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	60.05	50.17	°C/W

Note: 5. Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch × 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Electrical Characteristics (@T_A = -40°C to +125°C, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 10μF ceramic capacitor, V_{IN} = 14V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage	—	3	—	45	V
I_{GND}	Quiescent Current	No Load	—	2.1	8	μA
V_{OUT}	Output Voltage	I_{OUT} = 10mA	V_{OUT}x98%	—	V_{OUT}x102%	V
I_{OUT_MAX}	Output Current	—	150	—	—	mA
V_{DROP}	Dropout Voltage (Note 6)	I_{OUT} = 10mA, V_{IN} = V_{OUTNOM} – 0.1V	—	35	80	mV
		I_{OUT} = 100mA, V_{IN} = V_{OUTNOM} – 0.1V	—	350	800	mV
		I_{OUT} = 150mA, V_{IN} = V_{OUTNOM} – 0.1V	—	1000	1200	mV
$\triangle V_{OUT}(\triangle I_{OUT})$	Load Regulation (Note 7)	1mA ≤ I_{OUT} ≤ 100mA	—	0.02	0.025	%/mA
$\triangle V_{OUT}(\triangle V_{IN})$	Line Regulation	V_{OUTNOM} + 2V ≤ V_{IN} ≤ 45V, I_{OUT} = 1mA	—	0.01	0.02	%/V
I_{LIMIT}	Current Limit	—	150	—	500	mA
T_{OTSD}	Thermal Shutdown Temperature	—	—	+175	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—	—	+25	—	°C
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, V_{OUT} = 3.3V@1kHz	—	85	—	dB
V_n	Output Noise Voltage	BW = 10Hz to 100kHz, I_{OUT} = 30mA	—	120	—	μVrms

Notes: 6. Dropout voltage is the voltage difference between the input and output at which the output voltage drops 100mV below its nominal value. This parameter only applies to output voltages above 3.0V since minimum V_{IN} = 3.0V.
7. The AP7369Q internal circuitry is not fully operational until V_{IN} is at least the greater of 3V or (V_{OUT}+$V_{DROPOUT(MAX)}$).

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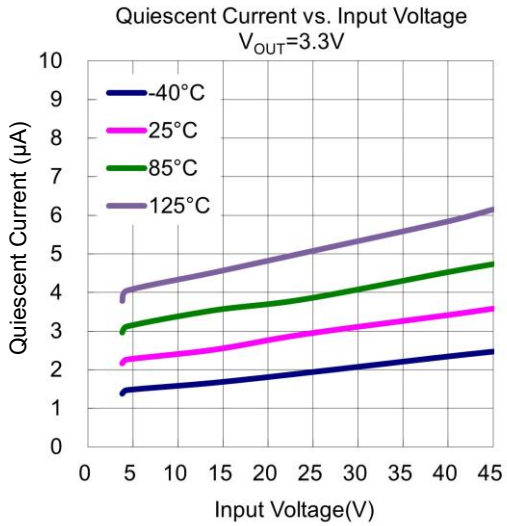
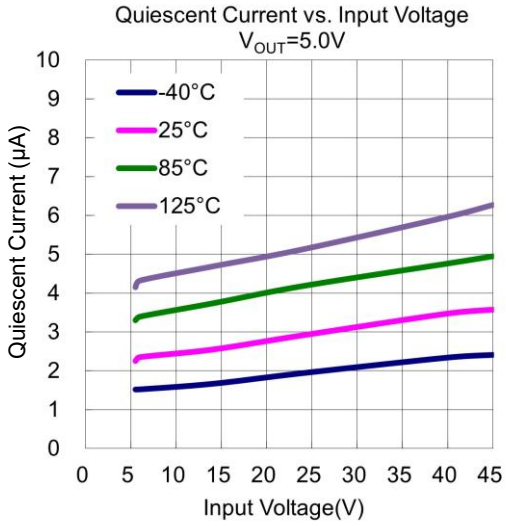
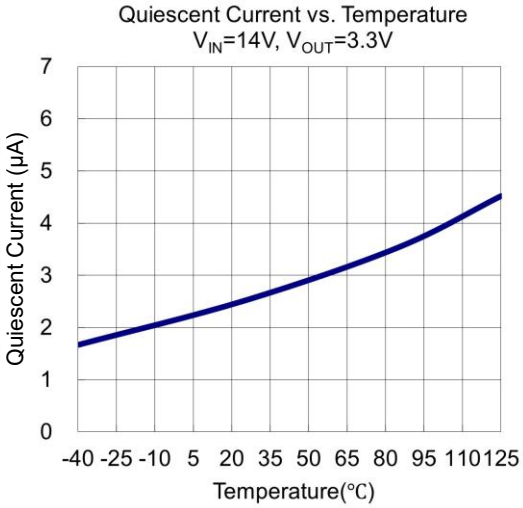
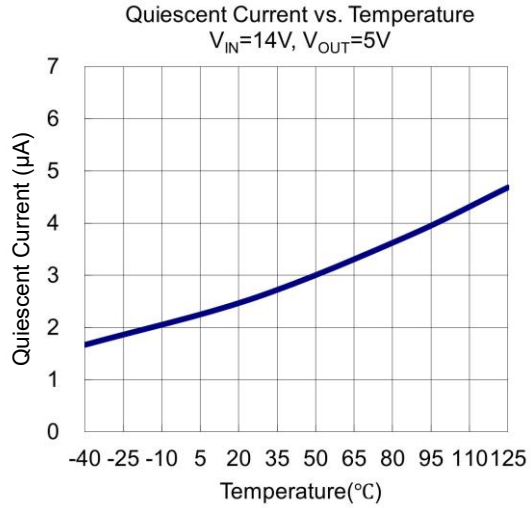
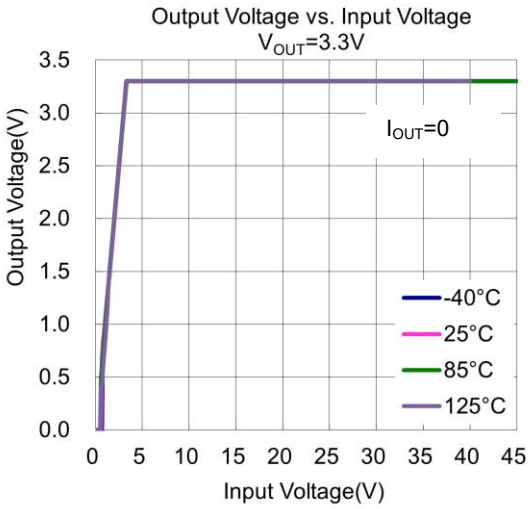
Performance Characteristics

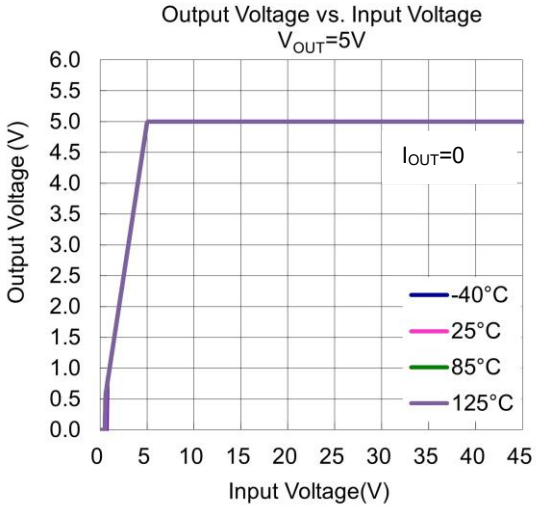












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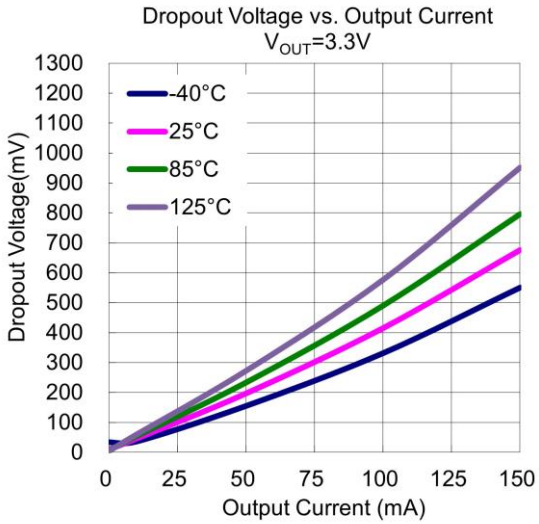
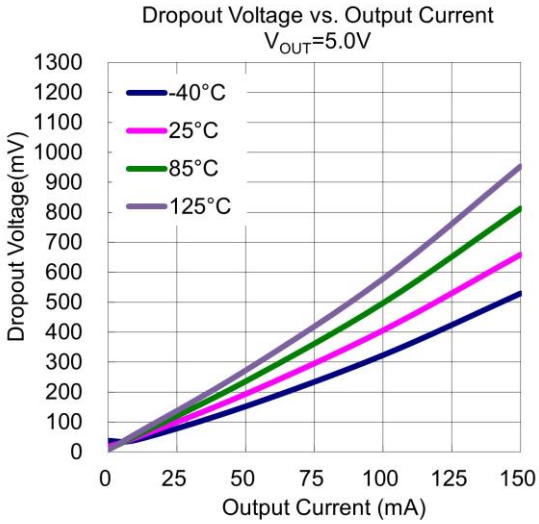
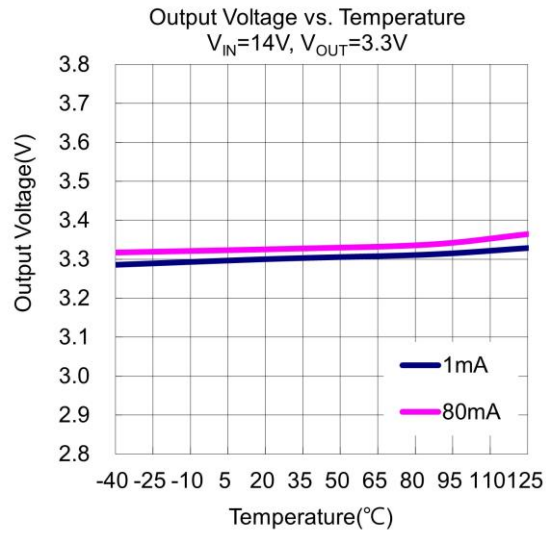
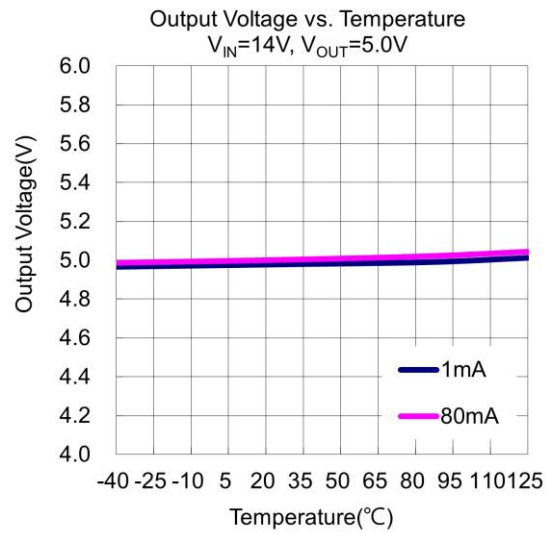
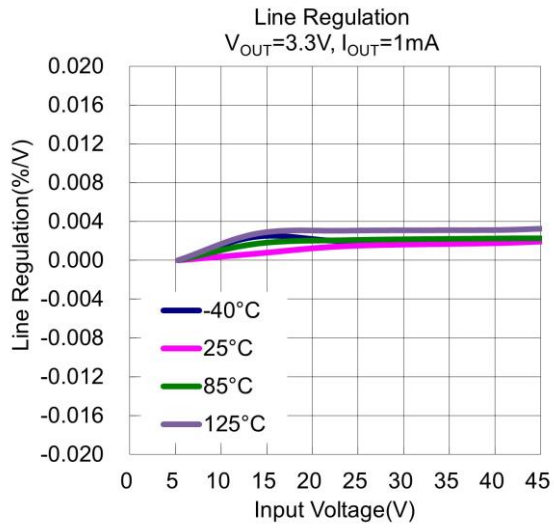
Performance Characteristics (continued)

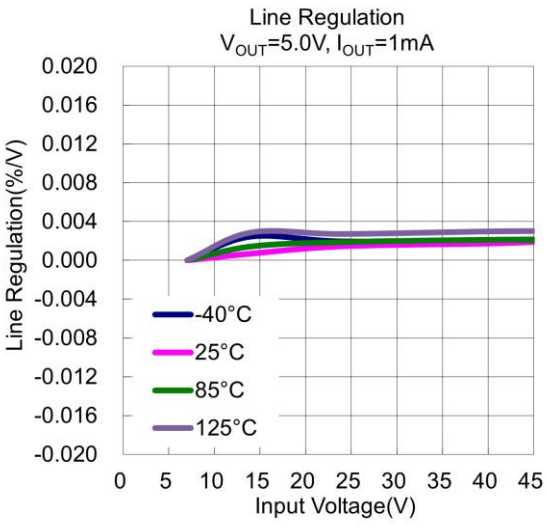












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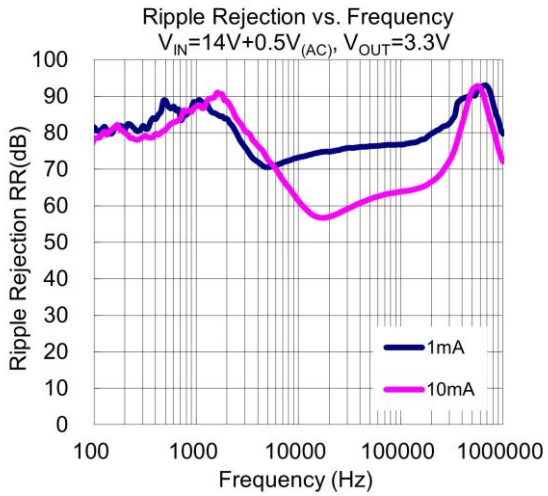
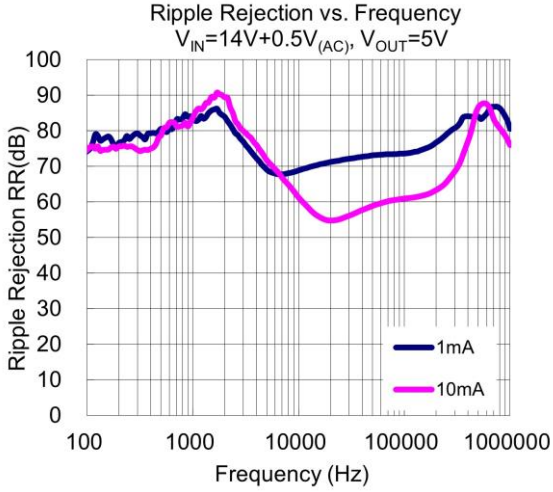
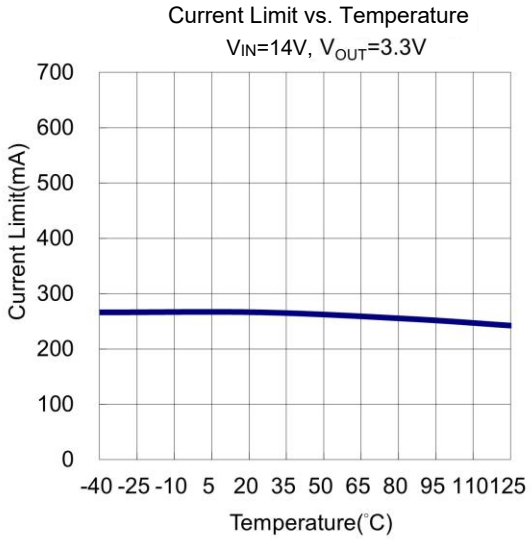
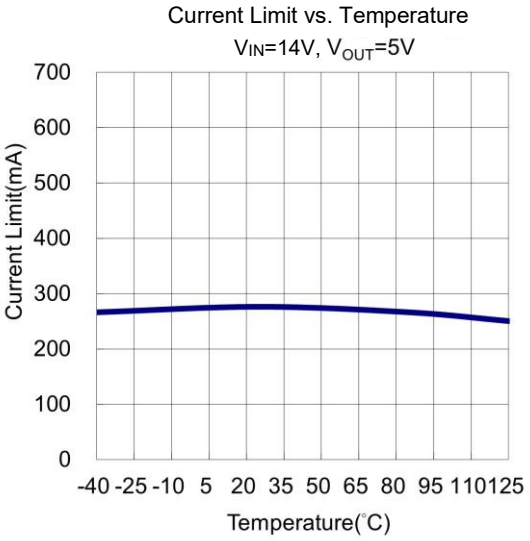
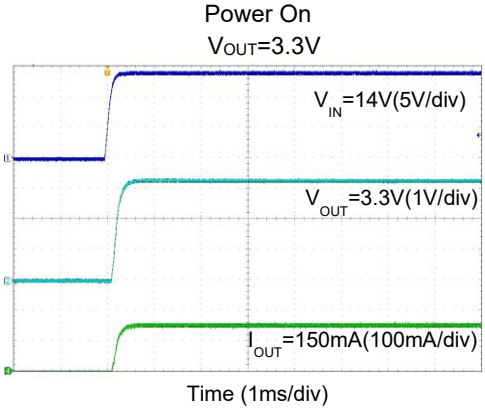
Performance Characteristics (continued)

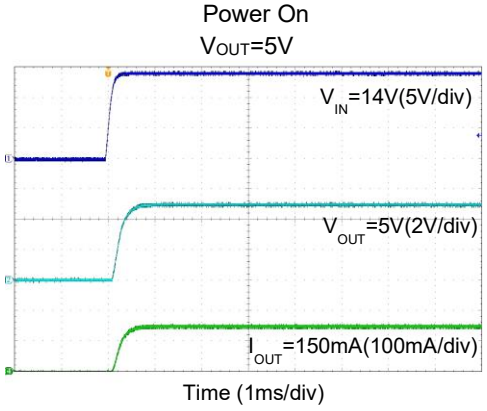












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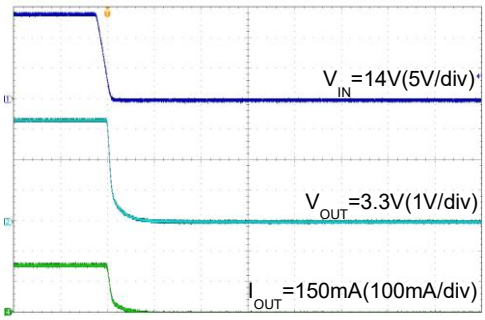
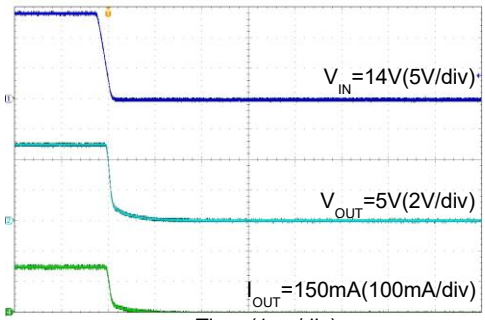
Performance Characteristics (continued)

Power Off
V_{OUT}=3.3V



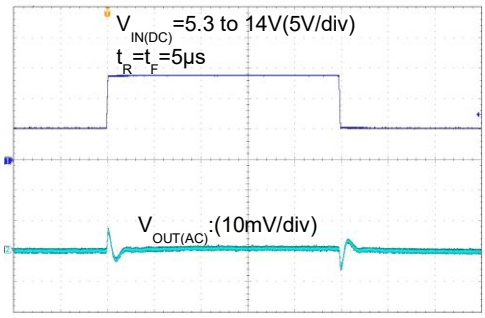
Time (1ms/div)

Power Off
V_{OUT}=5V



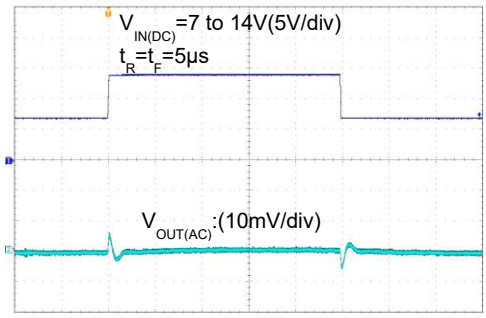
Time (1ms/div)

Line Transient Response
V_{OUT}=3.3V, I_{OUT}=10mA



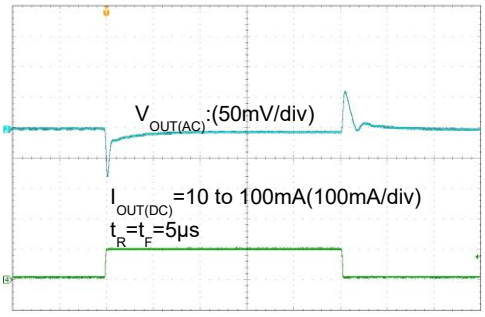
Time: 200μs/div

Line Transient Response
V_{OUT}=5V, I_{OUT}=10mA



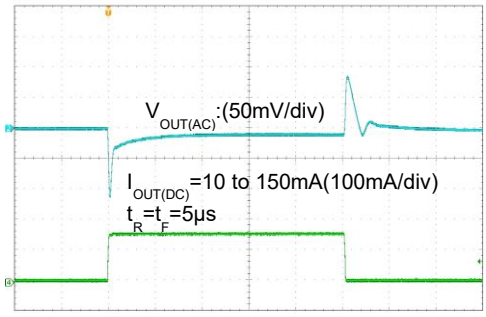
Time: 200μs/div

Load Transient Response
V_{OUT}=3.3V



Time: 200μs/div

Load Transient Response
V_{OUT}=3.3V



Time: 200μs/div

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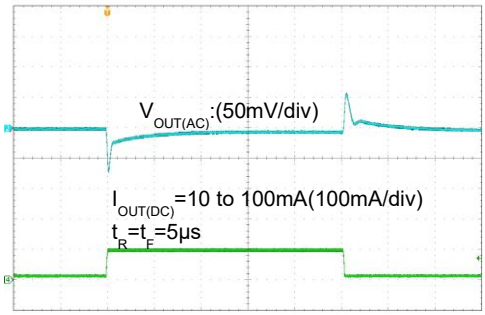
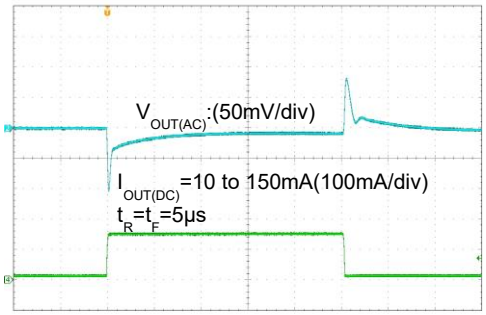
Performance Characteristics (continued)

Load Transient Response
V_{OUT}=5V



Time: 200μs/div

Load Transient Response
V_{OUT}=5V



Time: 200μs/div

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Application Information

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1μF. A ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place the output capacitor as close as possible to VOUT and GND pins.

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Current-Limit and Short-Circuit Protection

When output current at VOUT pin is higher than current-limit threshold or the VOUT pin directly shorts to GND, current-limit protection will trigger and clamp the output current at a pre-designed level to prevent overcurrent and thermal damage.

Thermal Protection

The AP7369Q has internal thermal sense and protection circuits. When excessive power dissipation happens on the device, such as short circuit at the output pin or very heavy load current with a large voltage drop across the device, the internal thermal protection circuit will trigger, shutting down the power MOSFET to prevent the LDO from damage. As soon as the excessive thermal condition is removed and the temperature of the device drops down, the thermal protection circuit will release the control of the power MOSFET, and the LDO device returns to normal operation.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

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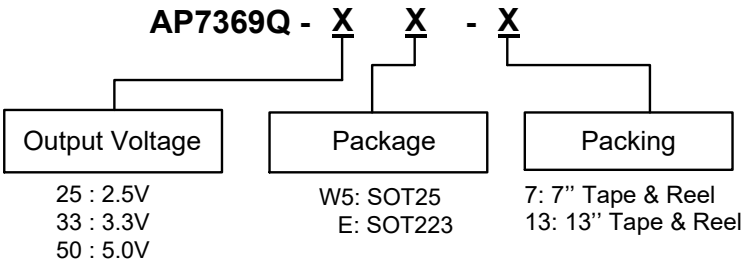
Ordering Information (Note 8)



Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7369Q-XXW5-7	W5	SOT25	3,000	7'' Tape & Reel
AP7369Q-XXE-13	E	SOT223	2,500	13'' Tape & Reel

Note: 8. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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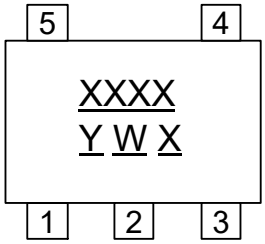
Marking Information

(1) SOT25

(Top View)

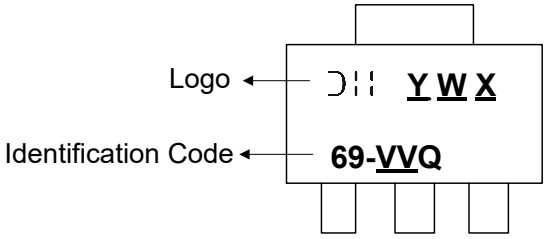


XXXX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents
52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP7369Q-25W5-7	SOT25	2AAQ
AP7369Q-33W5-7	SOT25	2ACQ
AP7369Q-50W5-7	SOT25	2ADQ

(2) SOT223

(Top View)



Y: Year: 0 to 9
W: Week: A to Z: 1 to 26 Week;
a to z: 27 to 52 Week; z Represents
52 and 53 Week
X: Internal Code
VV: Output Voltage

Orderable Part Number	Package	Identification Code
AP7369Q-25E-13	SOT223	69-25Q
AP7369Q-33E-13	SOT223	69-33Q
AP7369Q-50E-13	SOT223	69-50Q

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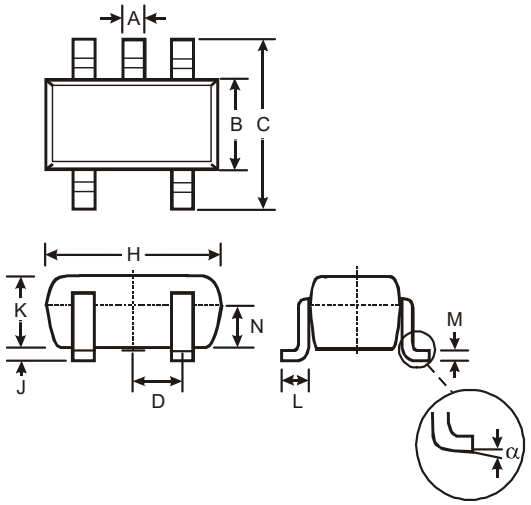
Package Outline Dimensions

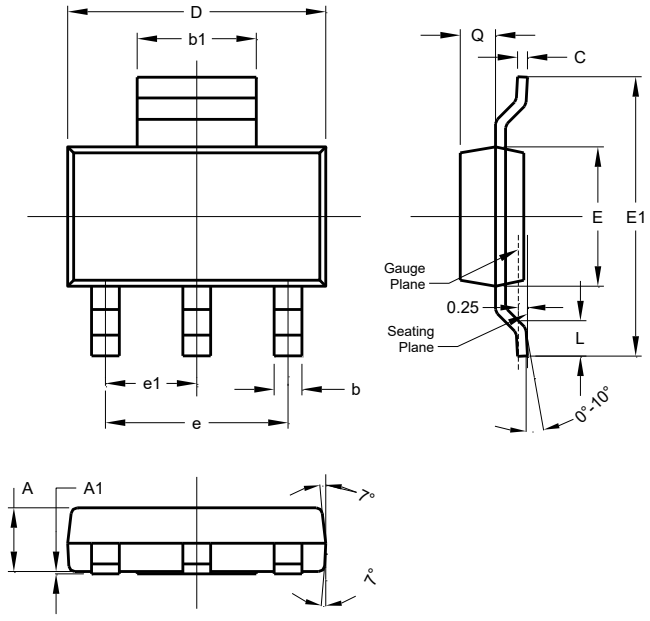
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT25



SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

SOT223



SOT223			
Dim	**Min**	**Max**	**Typ**
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b	0.60	0.80	0.70
b1	2.90	3.10	3.00
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	-	-	4.60
e1	-	-	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

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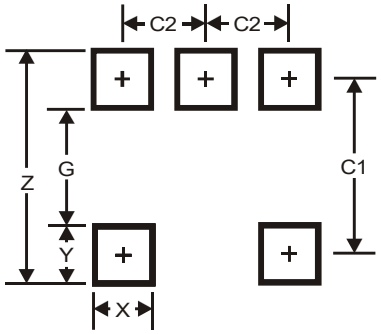
Suggested Pad Layout

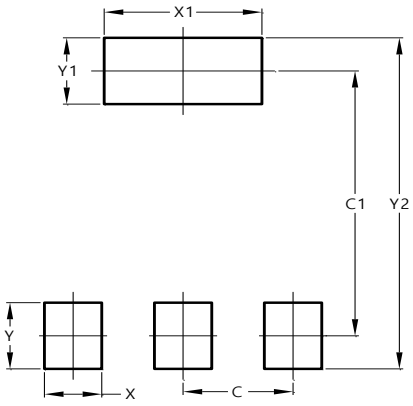
Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT25



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

SOT223



Dimensions	Value (in mm)
C	2.30
C1	6.40
X	1.20
X1	3.30
Y	1.60
Y1	1.60
Y2	8.00

Mechanical Data

SOT25

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.018 grams (Approximate)

SOT223

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.113 grams (Approximate)

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