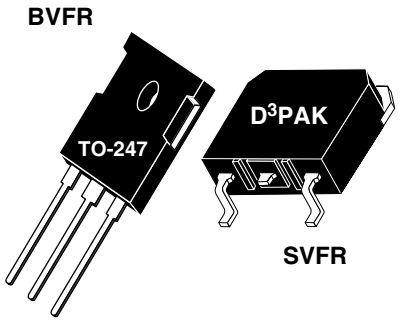
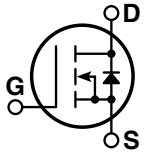
APT10M19BVFR
APT10M19SVFR
100V 75A 0.019Ω

POWER MOS V® FREDFET



Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- **Faster Switching**
- **Avalanche Energy Rated**
- **Lower Leakage**
- **FAST RECOVERY BODY DIODE**
- **TO-247 or Surface Mount D³PAK Package**



MAXIMUM RATINGS All Ratings: $T_C = 25°C$ unless otherwise specified.

Symbol	Parameter	APT10M19BVFR_SVFR	UNIT
V_{DSS}	Drain-Source Voltage	100	Volts
I_D	Continuous Drain Current @ $T_C = 25°C$	75	Amps
I_{DM}	Pulsed Drain Current ①	300	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ $T_C = 25°C$	370	Watts
	Linear Derating Factor	2.96	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① (Repetitive and Non-Repetitive)	75	Amps
E_{AR}	Repetitive Avalanche Energy ①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ④	1500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V$, $I_D = 250\mu A$)	100			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ② ($V_{GS} = 10V$, $I_D = 37.5A$)			0.019	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 100V$, $V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 80V$, $V_{GS} = 0V$, $T_C = 125°C$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V$, $V_{DS} = 0V$)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1mA$)	2		4	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1 MHz		5100	6120	pF
C_{oss}	Output Capacitance			1900	2660	
C_{rss}	Reverse Transfer Capacitance			800	1200	
Q_g	Total Gate Charge ③	V_{GS} = 10V V_{DD} = 50V I_D = 75A @ 25°C		200	300	nC
Q_{gs}	Gate-Source Charge			40	60	
Q_{gd}	Gate-Drain ("Miller") Charge			92	140	
$t_{d(on)}$	Turn-on Delay Time	V_{GS} = 15V V_{DD} = 50V I_D = 75A @ 25°C R_G = 1.6Ω		16	32	ns
t_r	Rise Time			40	80	
$t_{d(off)}$	Turn-off Delay Time			50	75	
t_f	Fall Time			20	40	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions		MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)				75	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)				300	
V_{SD}	Diode Forward Voltage ② (V_{GS} = 0V, I_S = -75A)				1.3	Volts
$^{dv}/_{dt}$	Peak Diode Recovery $^{dv}/_{dt}$ ⑤				5	V/ns
t_{rr}	Reverse Recovery Time (I_S = -75A, $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C			200	ns
		T_j = 125°C			350	
Q_{rr}	Reverse Recovery Charge (I_S = -75A, $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C		0.5		µC
		T_j = 125°C		1.0		
I_{RRM}	Peak Recovery Current (I_S = -75A, $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C		8		Amps
		T_j = 125°C		12		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.34	°C/W
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 µs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 0.53mH, R_G = 25Ω, Peak I_L = 75A

⑤ $^{dv}/_{dt}$ numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 75A$ $^{di}/_{dt} \leq 700A/\mu s$ $V_R \leq 100V$ $T_J \leq 150°C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

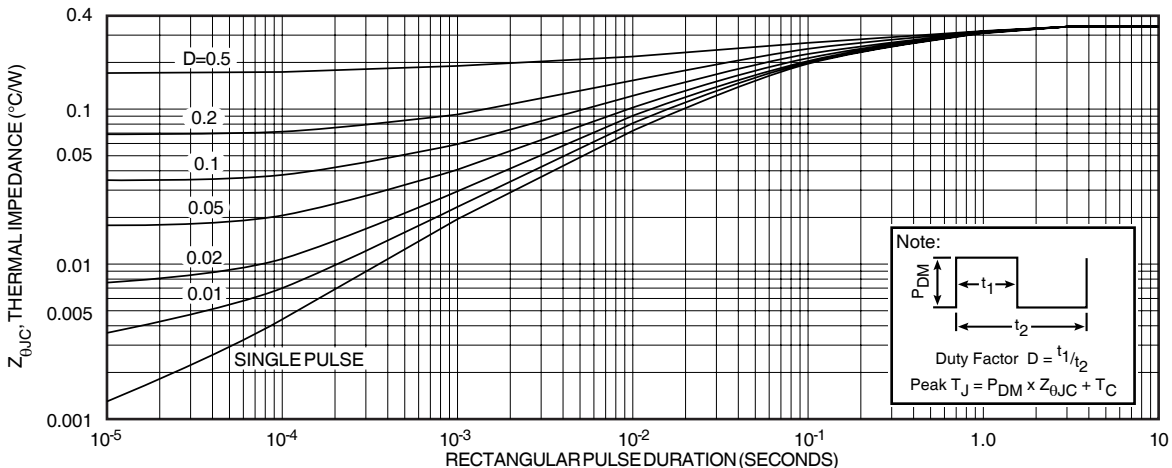


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

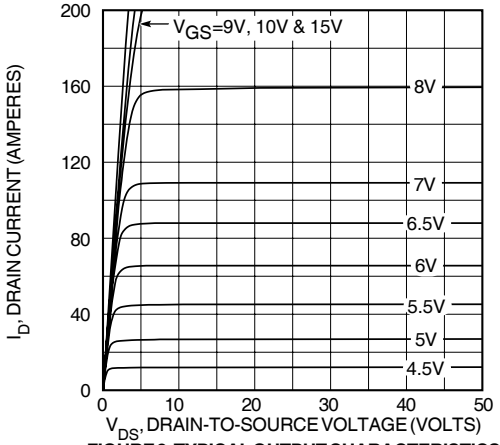


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

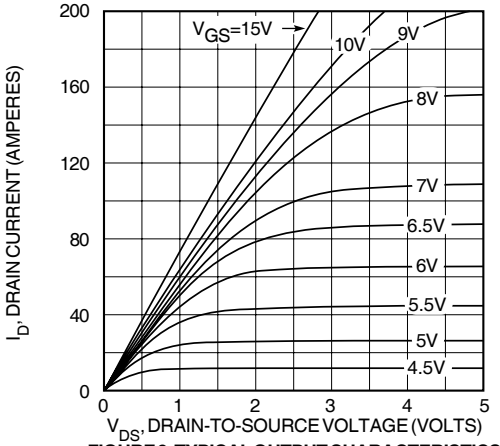


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

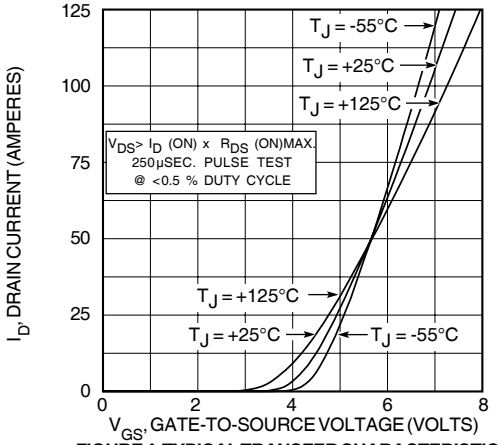


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

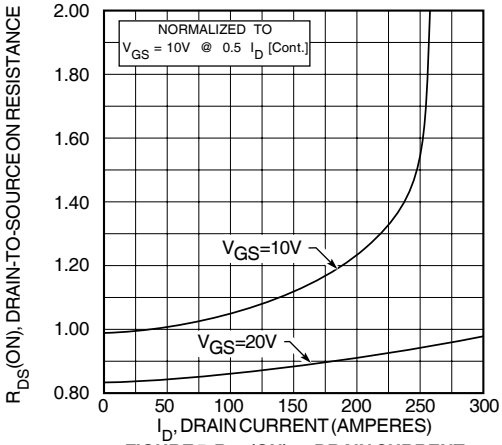


FIGURE 5, R_{DS}(ON) vs DRAIN CURRENT

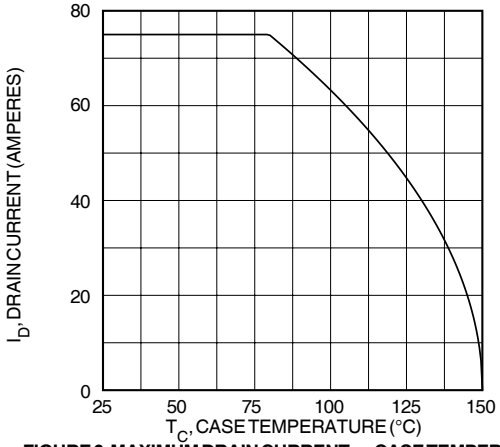


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

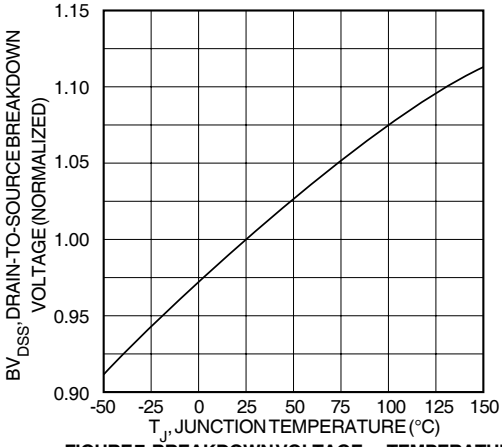


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

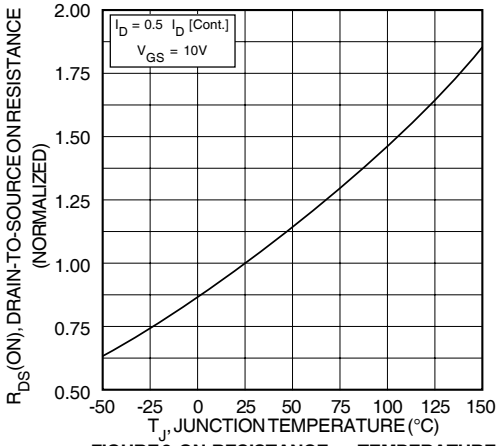


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

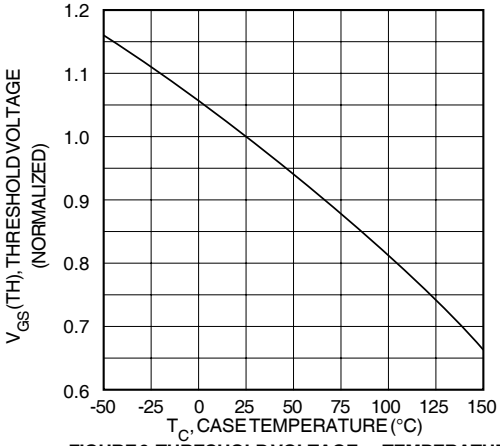


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

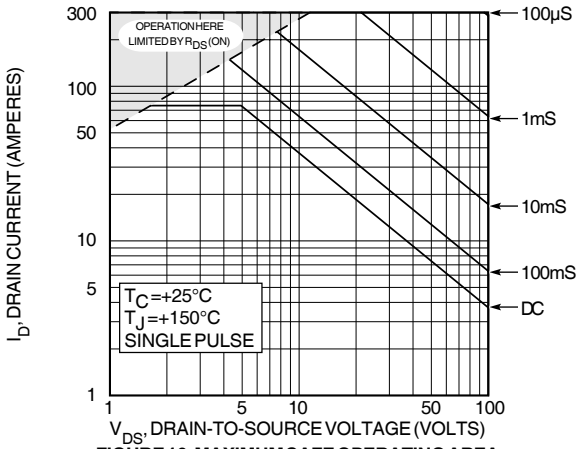


FIGURE 10, MAXIMUM SAFE OPERATING AREA

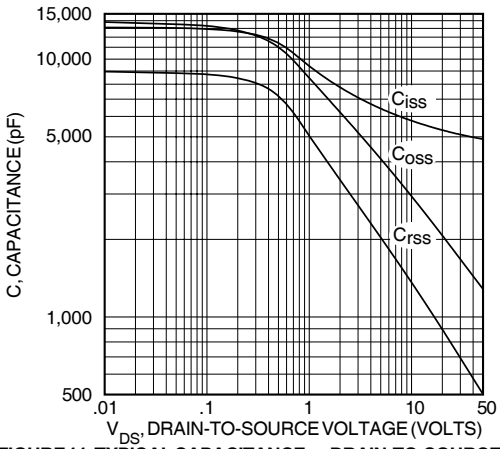


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

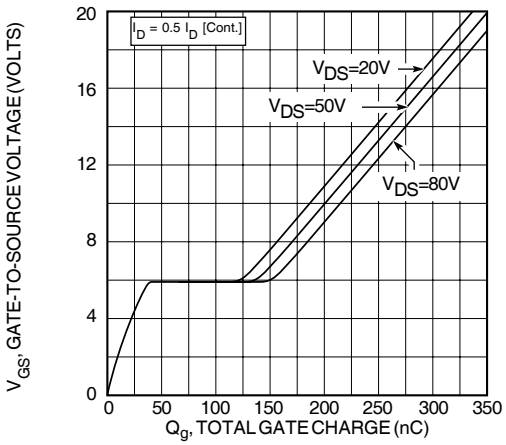


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

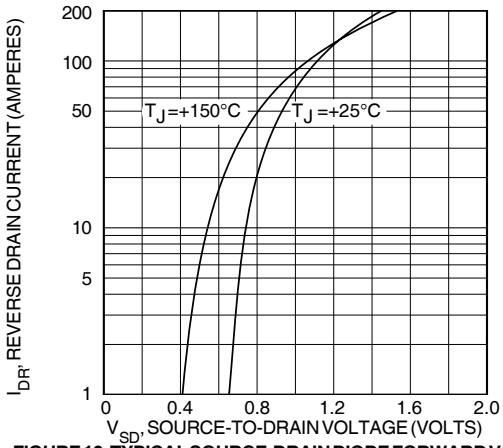
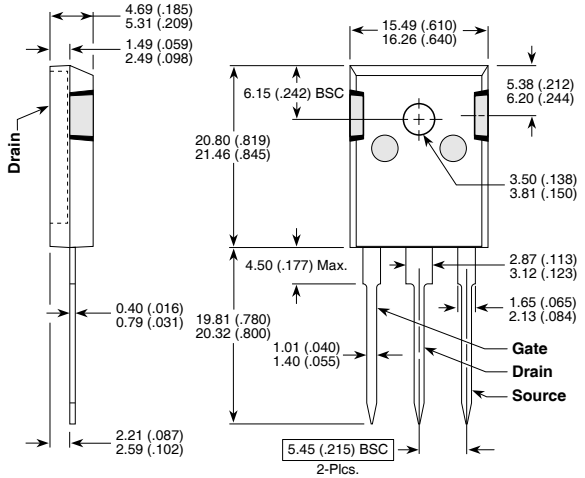


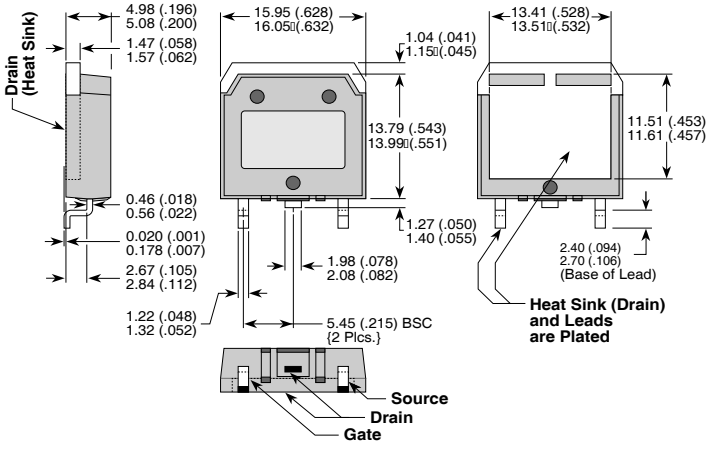
FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)



Dimensions in Millimeters and (Inches)

D^{3}PAK Package Outline (SVFR)



Dimensions in Millimeters (Inches)

APT's products are covered by one or more of U.S.patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522
5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.

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