ART800PE; ART800PEG

Power LDMOS transistor

AMPLEON

Rev. 1 — 28 September 2023 **Product data sheet**

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 800 W LDMOS RF power transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 650 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW pulsed [1][2]	108	65	800	29.3	77.2
CW	108	65	800	28.7	77.4

[1] Test circuit.

[2] t_p = 100 µs; δ = 10 %.

1.2 Features and benefits

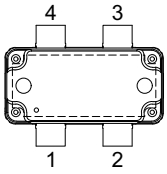
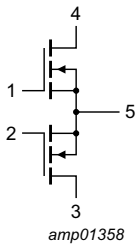
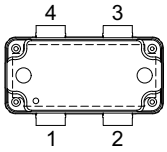
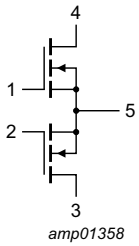
- High breakdown voltage enables class E operation at V_{DS} = 53 V
- Qualified up to a maximum of V_{DS} = 65 V
- Characterized from 30 V to 65 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
  - Plasma generators
  - MRI systems
  - Particle accelerators
- Broadcast
  - FM radio
  - VHF TV
- Communications
  - Non cellular communications
  - UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
ART800PE (OMP-780-4F-1)			
1	gate1		
2	gate2		
3	drain2		
4	drain1		
5	source [1]		
ART800PEG (OMP-780-4G-1)			
1	gate1		
2	gate2		
3	drain2		
4	drain1		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
OMP-780-4F-1	ART800PEY	9349 606 83518	TR13; 100-fold; 44 mm; dry pack	100
OMP-780-4G-1	ART800PEGY	9349 606 84518	TR13; 100-fold; 44 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	[1]	-	200	V
V_{GS}	gate-source voltage		–9	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]	-	225	°C

[1] Specified over lifetime at maximum operating temperature.

[2] Continuous use at maximum temperature will affect the reliability.

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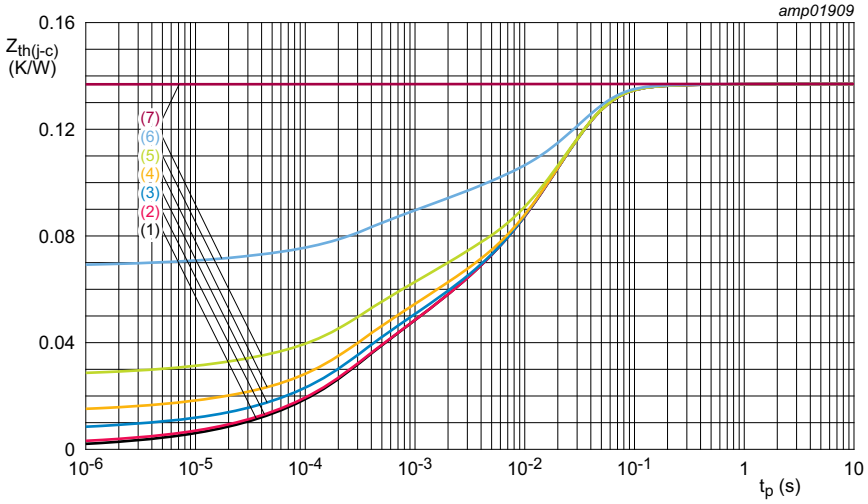
5. Thermal characteristics

Table 5. Thermal characteristics
According to standard MIL-STD-883E.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 100 °C, measured under RF condition [1]	0.137	K/W

[1] Refer to application note *AN221014* on the Ampleon website.

[2] See Figure 1.



(1) δ = 0.1 % (single pulse)
(2) δ = 1 %
(3) δ = 5 %
(4) δ = 10 %
(5) δ = 20 %
(6) δ = 50 %
(7) δ = 100 % (steady state)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.8 mA	203	208	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 275 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	µA

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Table 6. DC characteristics *…continued*

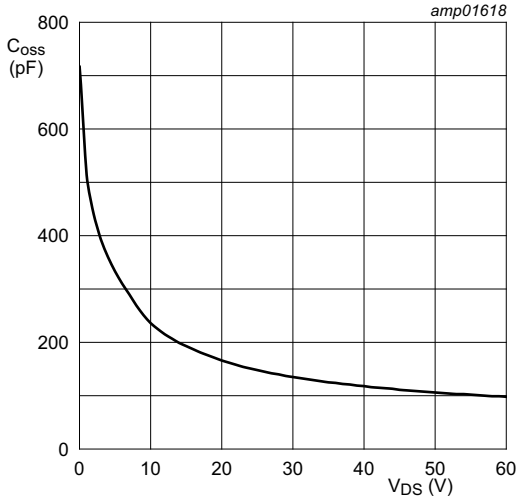
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75$ V; V_{DS} = 20 V	-	37.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75$ V; I_D = 9.625 A	-	0.200	-	Ω

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	1.88	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	313	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	95	-	pF



V_{GS} = 0 V; f = 1 MHz

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 10 %; f = 108 MHz; RF performance at V_{DS} = 65 V; I_{Dq} = 25 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 800 W	26.8	29.2	-	dB
RL_{in}	input return loss	P_L = 800 W	-	17	-	dB
η_D	drain efficiency	P_L = 800 W	70	74.5	-	%

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7. Test information

7.1 Ruggedness in class-AB operation

The ART800PE and ART800PEG are capable of withstanding a load mismatch corresponding to VSWR ≥ 65 : 1 through all phases under the following conditions: P_L = 800 W pulsed at V_{DS} = 65 V; I_{Dq} = 50 mA per section; t_p = 100 μs; δ = 10 %; f = 108 MHz.

7.2 Impedance information

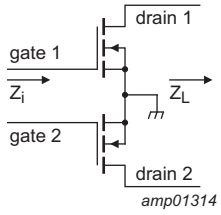


Fig 3. Definition of transistor impedance

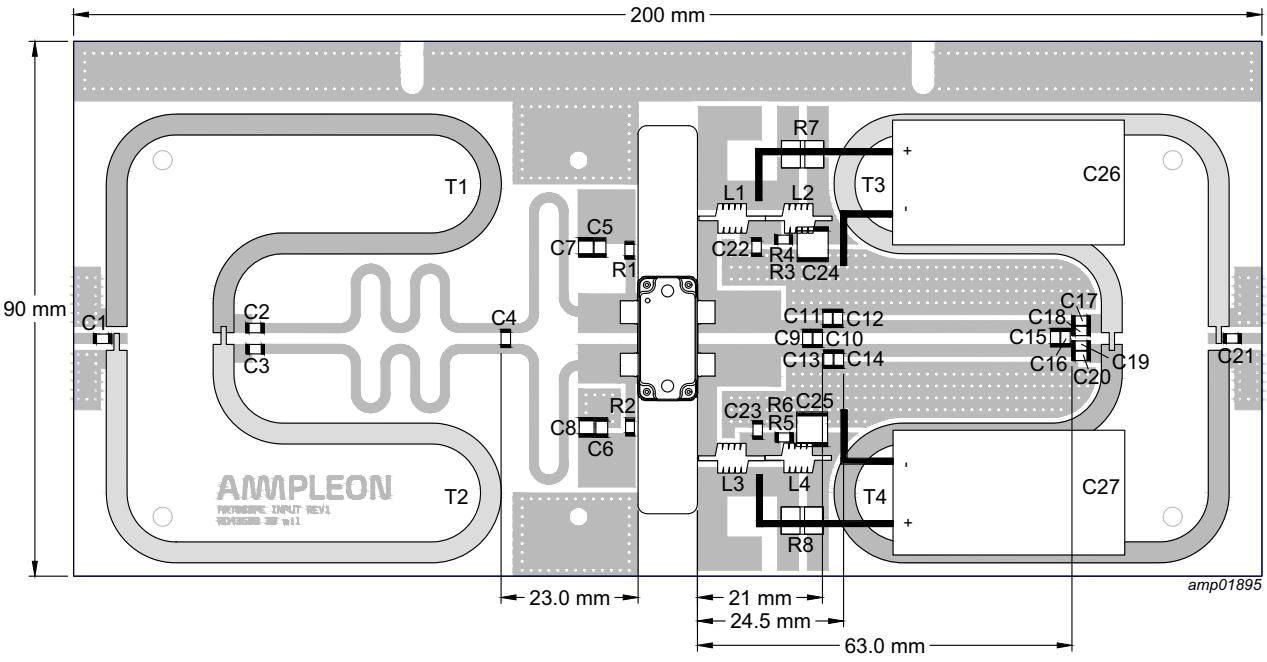
Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 65 V and P_L = 800 W.

f	Z_i	Z_L
(MHz)	(Ω)	(Ω)
108	4.8 – j17.3	9.1 + j3.2

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7.3 Test circuit



Printed-Circuit Board (PCB): RO4350B; ε_r = 3.48 F/m; thickness = 0.762 mm.

See Table 10 for a list of components.

Fig 4. Component layout

Table 10. List of components

For test circuit see Figure 4.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	510 pF [1]	
C2, C3	multilayer ceramic chip capacitor	62 pF [1]	
C4	multilayer ceramic chip capacitor	160 pF [1]	
C5, C6, C22, C23	multilayer ceramic chip capacitor	820 pF [1]	
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: GRM32ER71H475KA88L
C9, C10	multilayer ceramic chip capacitor	36 pF [1]	
C11, C12, C13, C14, C15, C16, C18, C20	multilayer ceramic chip capacitor	56 pF [1]	
C17, C19	multilayer ceramic chip capacitor	51 pF [1]	
C21	multilayer ceramic chip capacitor	220 pF [1]	
C24, C25	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C26, C27	electrolytic capacitor	1500 μF, 80 V	radial leaded
L1, L3	5 turn, 1 mm copper wire	D = 4 mm	
L2, L4	3 turn, 1mm copper wire	D = 4 mm	
R1, R2	chip resistor	4.7 kΩ	SMD 1206

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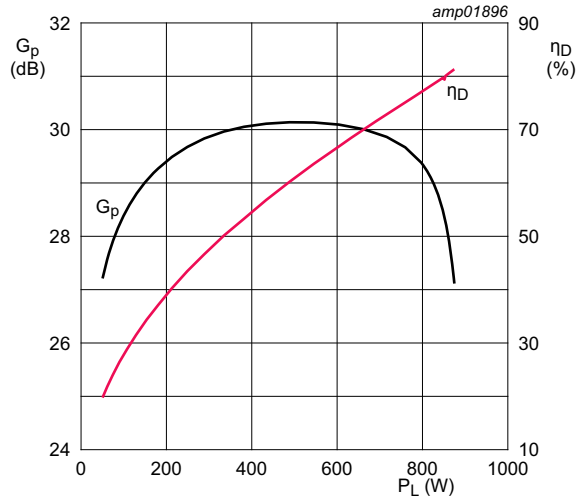
Table 10. List of components *…continued*
For test circuit see Figure 4.

Component	Description	Value	Remarks
R3, R4, R5, R6	chip resistor	20 Ω	SMD 1206
R7, R8	chip resistor	0.01 Ω	Vishay: WSHP2818
T1, T2, T3, T4	hand formable coax	50 Ω, 160 mm	SUCOFORM_141

[1] AVX type 800B or capacitor of same quality.

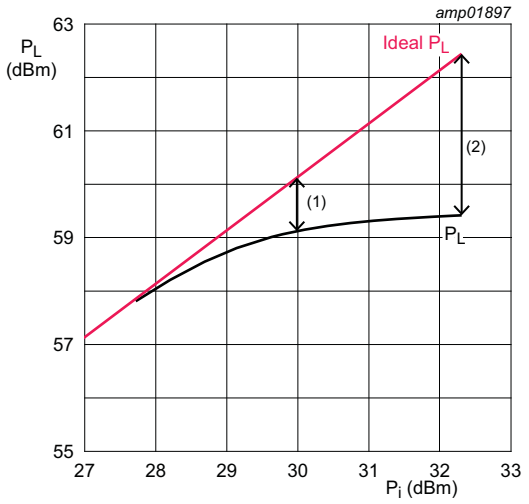
7.4 Graphical data

7.4.1 1-Tone CW pulsed



V_{DS} = 65 V; I_{Dq} = 50 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values



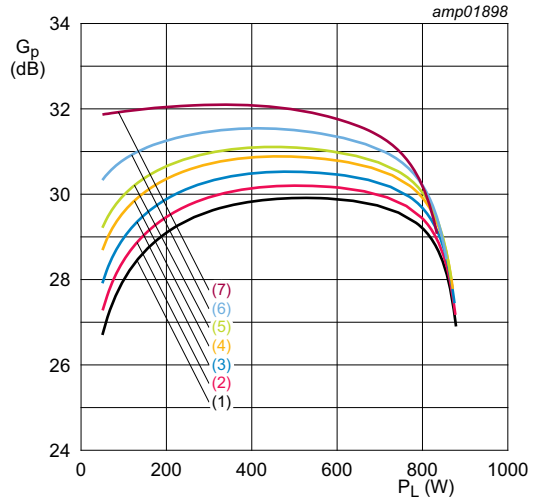
V_{DS} = 65 V; I_{Dq} = 50 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) $P_{L(1dB)}$ = 59.12 dBm (817 W)

(2) $P_{L(3dB)}$ = 59.42 dBm (875 W)

Fig 6. Output power as a function of input power; typical values

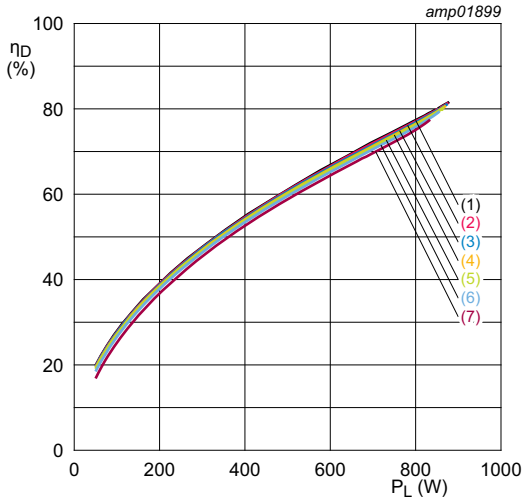
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V_{DS} = 65 V; f = 108 MHz; t_p = 100 µs; δ = 10 %.

(1) I_{Dq} = 25 mA per section
(2) I_{Dq} = 50 mA per section
(3) I_{Dq} = 100 mA per section
(4) I_{Dq} = 200 mA per section
(5) I_{Dq} = 300 mA per section
(6) I_{Dq} = 600 mA per section
(7) I_{Dq} = 1200 mA per section

Fig 7. Power gain as a function of output power; typical values

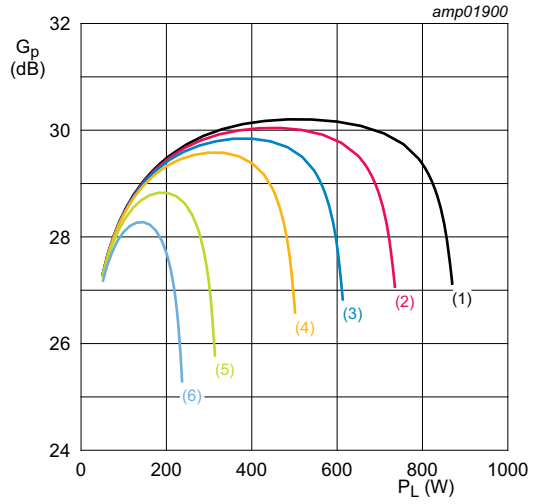


V_{DS} = 65 V; f = 108 MHz; t_p = 100 µs; δ = 10 %.

(1) I_{Dq} = 25 mA per section
(2) I_{Dq} = 50 mA per section
(3) I_{Dq} = 100 mA per section
(4) I_{Dq} = 200 mA per section
(5) I_{Dq} = 300 mA per section
(6) I_{Dq} = 600 mA per section
(7) I_{Dq} = 1200 mA per section

Fig 8. Drain efficiency as a function of output power; typical values

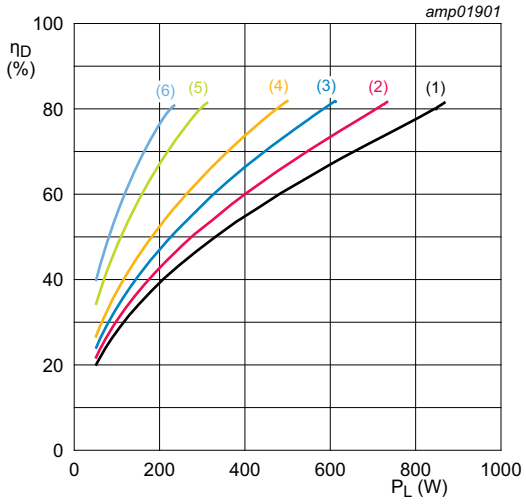
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I_{Dq} = 50 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V
(2) V_{DS} = 60 V
(3) V_{DS} = 55 V
(4) V_{DS} = 50 V
(5) V_{DS} = 40 V
(6) V_{DS} = 30 V

Fig 9. Power gain as a function of output power; typical values



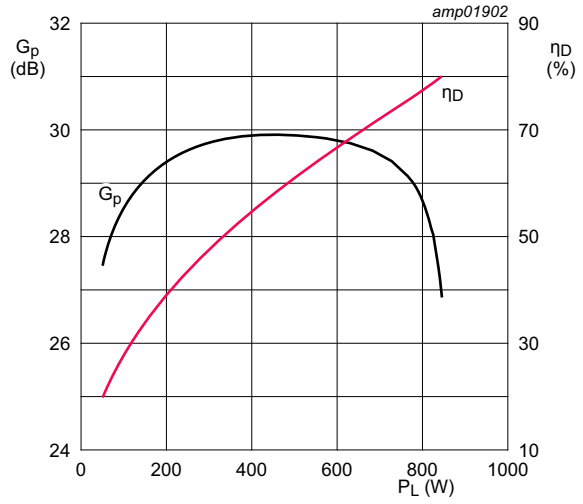
I_{Dq} = 50 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V
(2) V_{DS} = 60 V
(3) V_{DS} = 55 V
(4) V_{DS} = 50 V
(5) V_{DS} = 40 V
(6) V_{DS} = 30 V

Fig 10. Drain efficiency as a function of output power; typical values

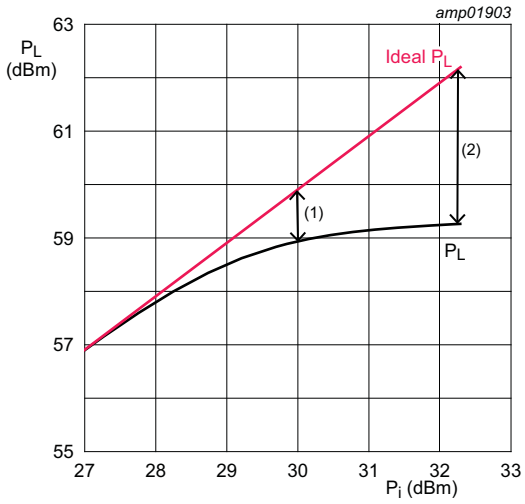
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7.4.2 1-Tone CW



V_{DS} = 65 V; I_{Dq} = 50 mA per section; f = 108 MHz.

Fig 11. Power gain and drain efficiency as function of output power; typical values

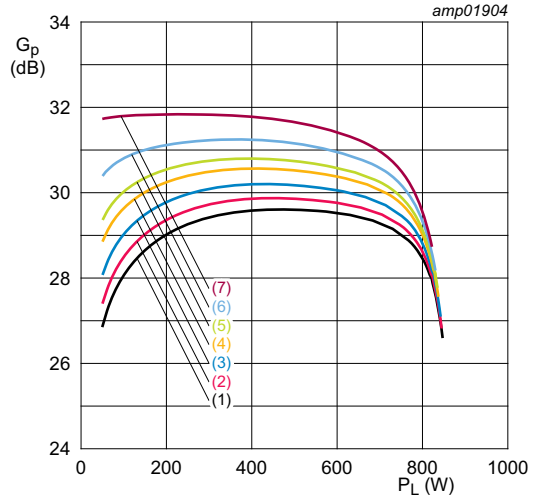


V_{DS} = 65 V; I_{Dq} = 50 mA per section; f = 108 MHz.

(1) $P_{L(1dB)}$ = 58.95 dBm (786 W)

(2) $P_{L(3dB)}$ = 59.26 dBm (844 W)

Fig 12. Output power as a function of input power; typical values



V_{DS} = 65 V; f = 108 MHz.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

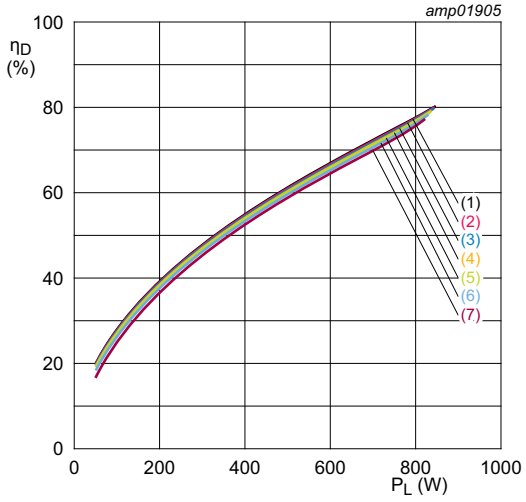
(4) I_{Dq} = 200 mA per section

(5) I_{Dq} = 300 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 1200 mA per section

Fig 13. Power gain as a function of output power; typical values



V_{DS} = 65 V; f = 108 MHz.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

(4) I_{Dq} = 200 mA per section

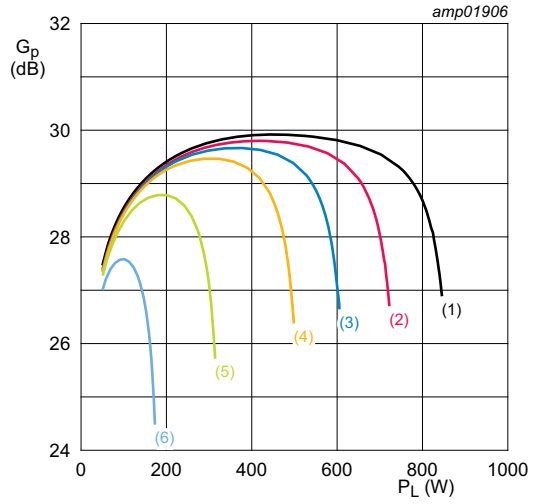
(5) I_{Dq} = 300 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 1200 mA per section

Fig 14. Drain efficiency as a function of output power; typical values

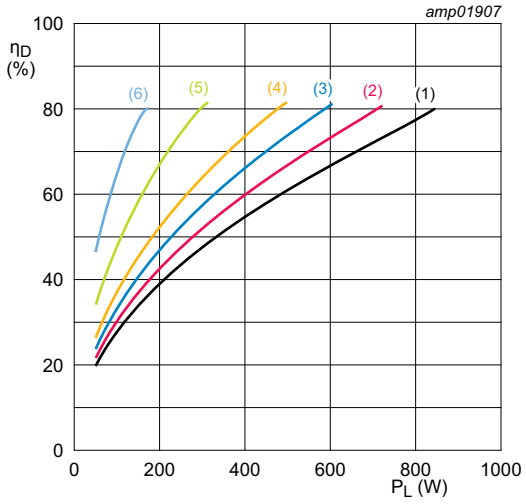
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I_{Dq} = 50 mA per section; f = 108 MHz.

(1) V_{DS} = 65 V
(2) V_{DS} = 60 V
(3) V_{DS} = 55 V
(4) V_{DS} = 50 V
(5) V_{DS} = 40 V
(6) V_{DS} = 30 V

Fig 15. Power gain as a function of output power; typical values



I_{Dq} = 50 mA per section; f = 108 MHz.

(1) V_{DS} = 65 V
(2) V_{DS} = 60 V
(3) V_{DS} = 55 V
(4) V_{DS} = 50 V
(5) V_{DS} = 40 V
(6) V_{DS} = 30 V

Fig 16. Drain efficiency as a function of output power; typical values

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8. Package outline

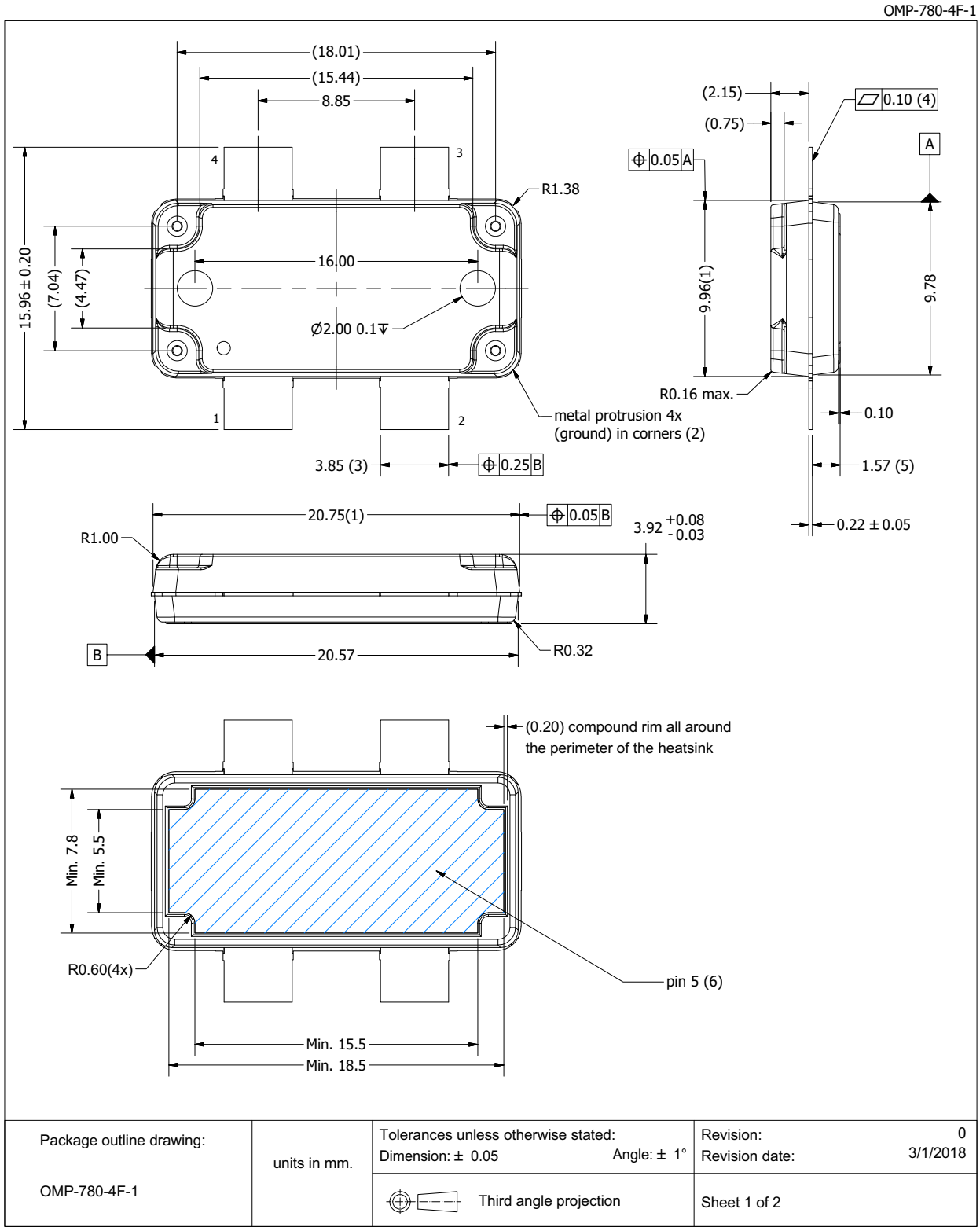
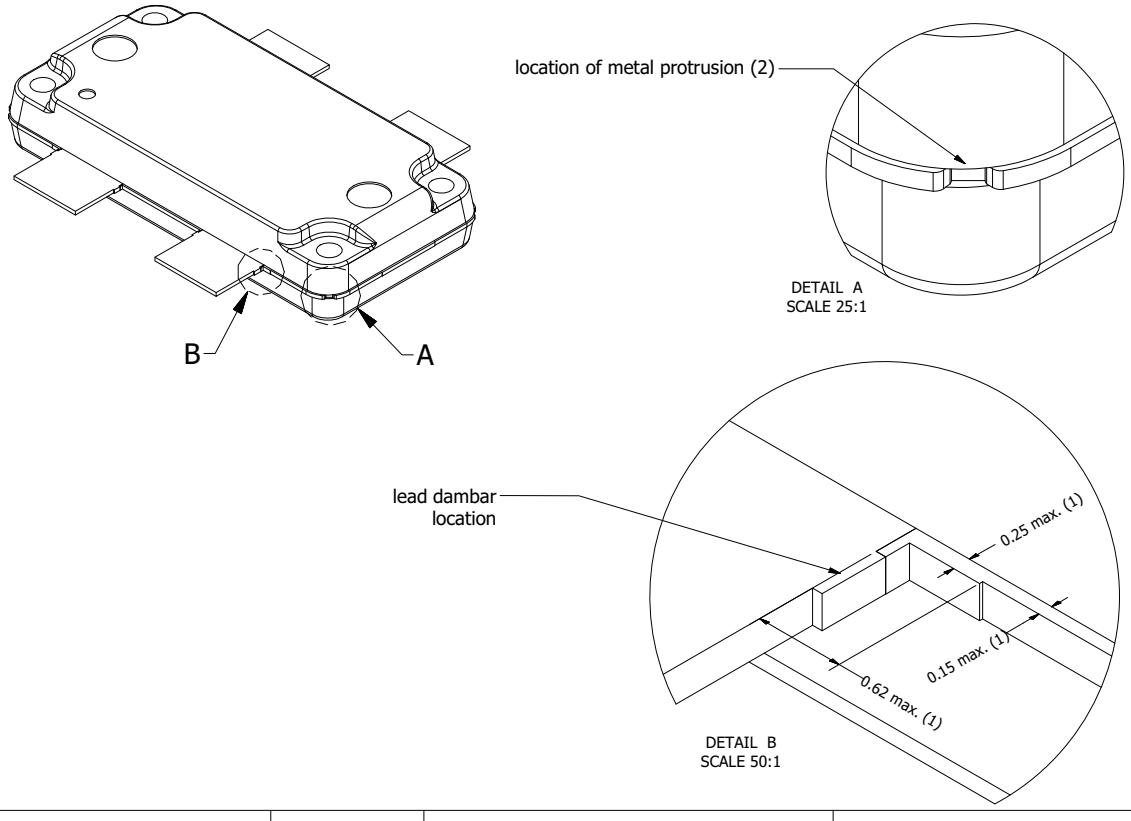


Fig 17. Package outline OMP-780-4F-1 (sheet 1 of 2)

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OMP-780-4F-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and max. 0.62 mm in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured 0.5 mm from the edge of the top package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing: OMP-780-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1° Third angle projection	Revision: 0 Revision date: 3/1/2018 Sheet 2 of 2

Fig 18. Package outline OMP-780-4F-1 (sheet 2 of 2)

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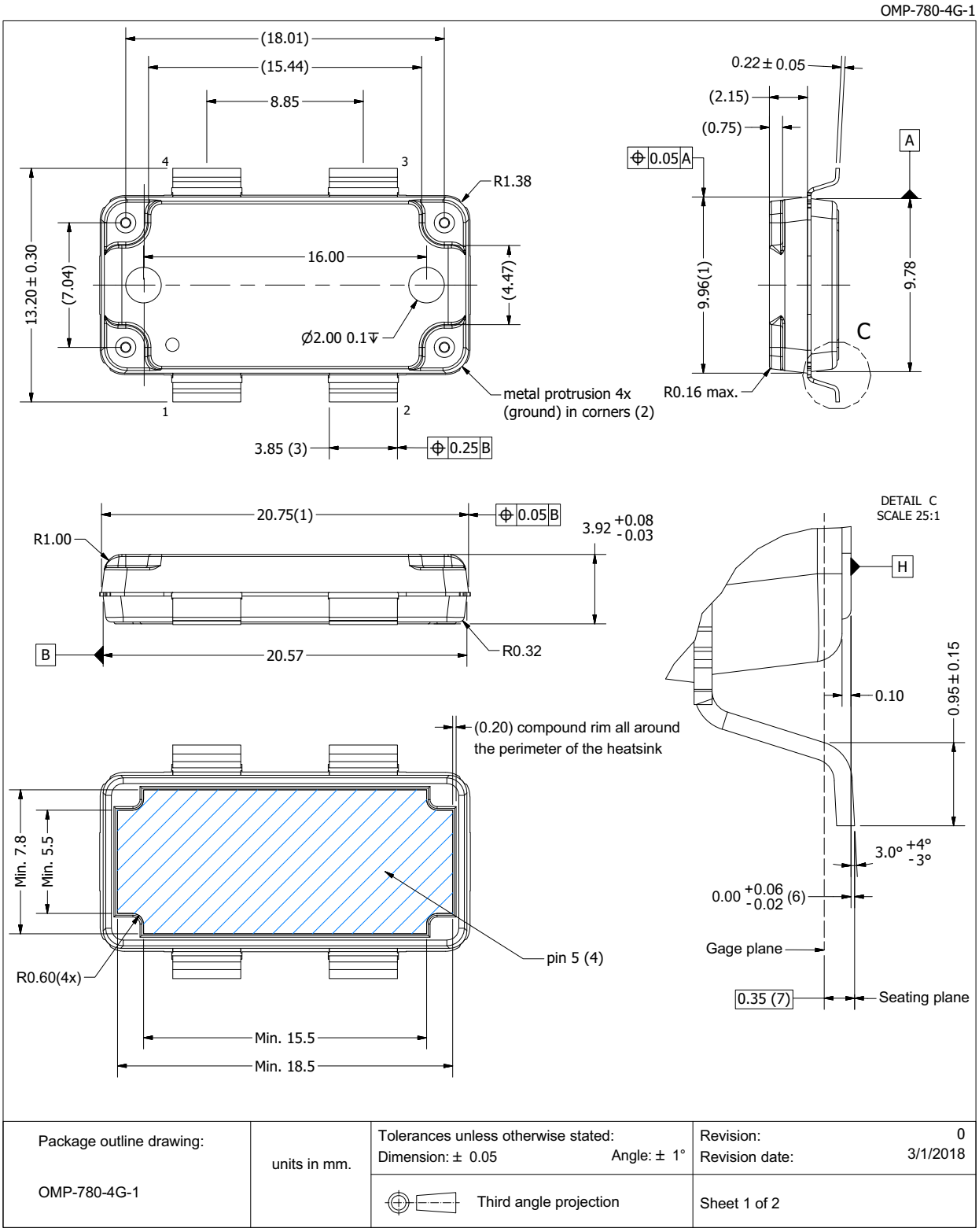
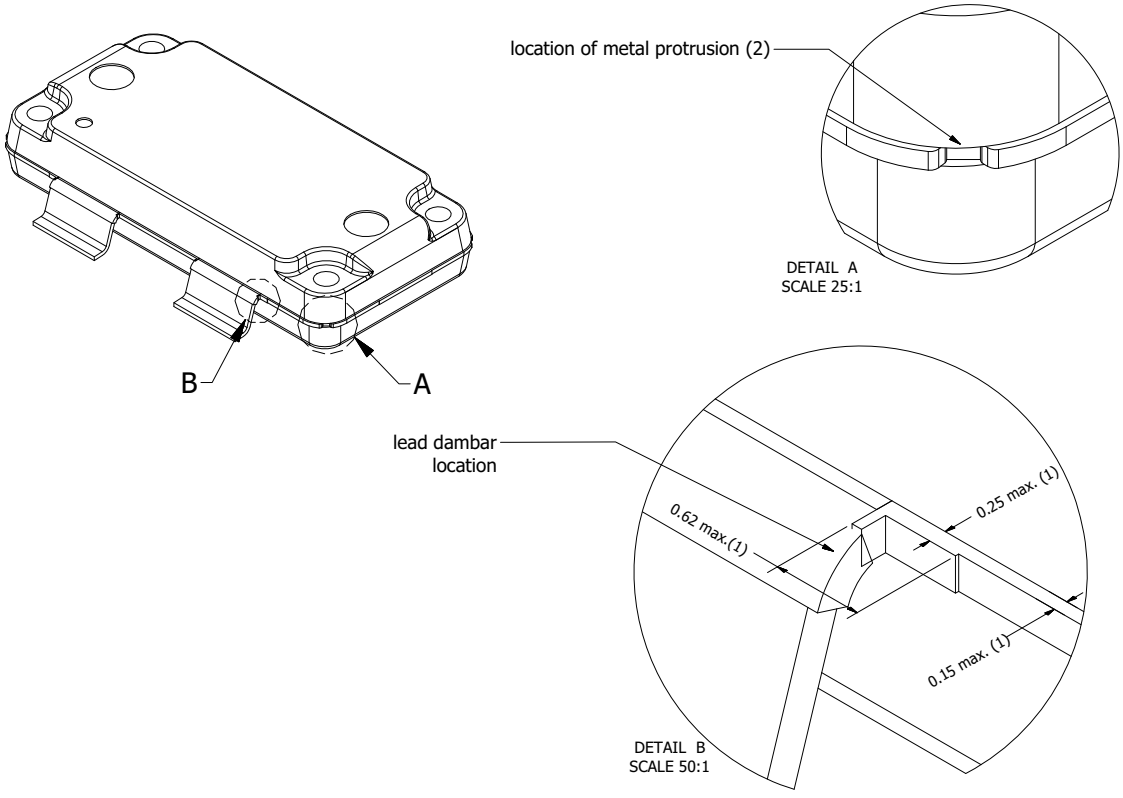


Fig 19. Package outline OMP-780-4G-1 (sheet 1 of 2)

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OMP-780-4G-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The hatched area indicated the exposed heatsink.
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).
(6)	Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.
(7)	Gage plane (foot length) to be measured from the seating plane.



Package outline drawing: OMP-780-4G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1° Third angle projection	Revision: 0 Revision date: 3/1/2018 Sheet 2 of 2

Fig 20. Package outline OMP-780-4G-1 (sheet 2 of 2)

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART800PE_ART800PEG v.1	20230928	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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