BLA9G1011L(S)-300; BLA9G1011L(S)-300G

Power LDMOS transistor

AMPLEON

Rev. 1 — 25 July 2017

Product data sheet

1. Product profile

1.1 General description

300 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Typical information

Typical RF performance at T_{case} = 25 °C; t_p = 50 µs; δ = 2 %; I_{Dq} = 100 mA; in a class-AB demo test circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D	t_r	t_f
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	1030	32	317	20.6	63.5	14	5
	1060	32	317	21.5	64.8	14	5
	1090	32	317	21.8	64.8	14	5

1.2 Features and benefits

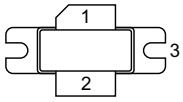
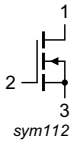
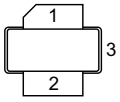
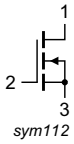
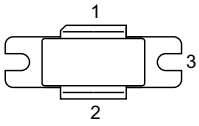
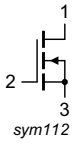
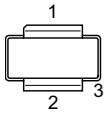
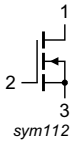
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA9G1011L-300 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLA9G1011LS-300 (SOT502B)			
1	drain		
2	gate		
3	source [1]		
BLA9G1011L-300G (SOT502F)			
1	drain		
2	gate		
3	source [1]		
BLA9G1011LS-300G (SOT502E)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA9G1011L-300	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA9G1011LS-300	-	earless flanged ceramic package; 2 leads	SOT502B
BLA9G1011L-300G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA9G1011LS-300G	-	earless flanged ceramic package; 2 leads	SOT502E

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−6	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 25 °C; t_p = 100 μs; δ = 10 %	0.140	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 330 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	60	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 330 mA	-	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.55 A	-	0.043	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 50 μs; δ = 2 %; V_{DS} = 32 V; f = 1060 MHz; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 300 W	18	19.5	-	dB
RL_{in}	input return loss	P_L = 300 W	-	−10	-	dB
η_D	drain efficiency	P_L = 300 W	56	60.5	-	%
t_r	rise time	P_L = 300 W	-	14	-	ns
t_f	fall time	P_L = 300 W	-	5	-	ns

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7. Test information

7.1 Ruggedness in class-AB operation

The BLA9G1011L-300, BLA9G1011LS-300, BLA9G1011L-300G and BLA9G1011LS-300G are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: t_p = 50 μs; δ = 2 %; V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 300 W; f = 1030 MHz to 1090 MHz.

7.2 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	**(Ω)**	**(Ω)**
1000	0.87 – j2.02	1.38 – j1.78
1050	1.34 – j2.26	1.4 – j1.54
1100	1.82 – j2.77	1.4 – j1.54

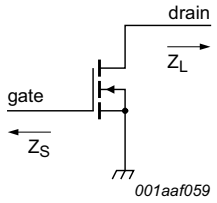
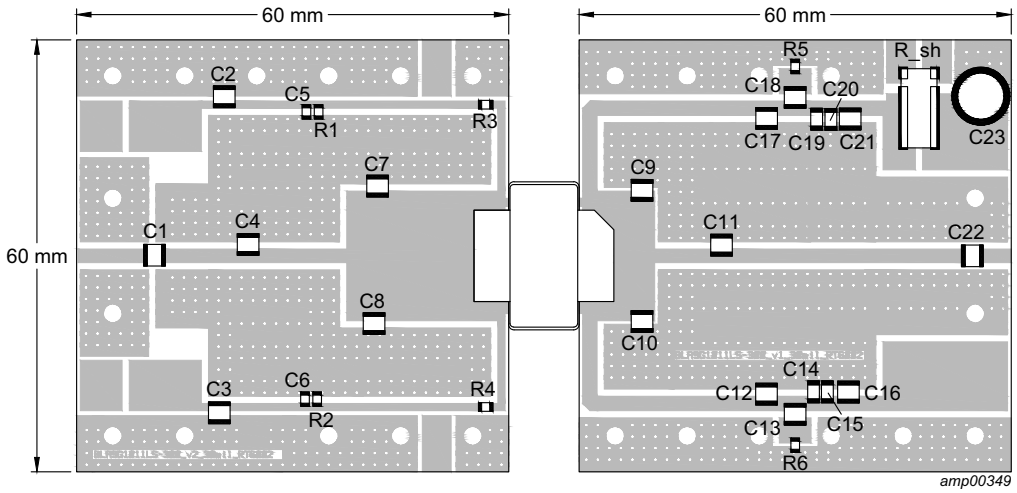


Fig 1. Definition of transistor impedance

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RT/duroid 6002; thickness = 0.762 mm; top/bottom copper plating.

See Table 9 for a list of components.

Fig 2. Demo test circuit component layout

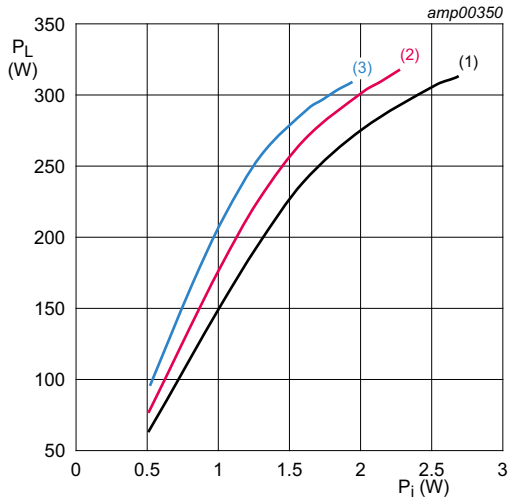
Table 9. Demo test circuit list of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	56 pF	ATC: ATC100A560FT150XTV
C2, C3	multilayer ceramic chip capacitor	750 pF	ATC: ATC100B750FT500XTV
C4	multilayer ceramic chip capacitor	2.4 pF	ATC: ATC100B2R4BT500XTV
C5, C6	multilayer ceramic chip capacitor	62 pF	ATC: ATC100A620FT150XTV
C7, C8	multilayer ceramic chip capacitor	3.3 pF	ATC: ATC100B3R3BT500XTV
C9, C10	multilayer ceramic chip capacitor	7.5 pF	ATC: ATC100B7R5BT500XTV
C11	multilayer ceramic chip capacitor	4.7 pF	ATC: ATC100B4R7BT500XTV
C12, C17	multilayer ceramic chip capacitor	62 pF	ATC: ATC100B620FT500XTV
C13, C18	multilayer ceramic chip capacitor	750 pF	ATC: ATC100B751FT500XTV
C14, C19	multilayer ceramic chip capacitor	10 nF	Murata: GRM188R71H103KA01D
C15, C20	multilayer ceramic chip capacitor	100 nF	Murata: GRM31C5C1E104JA01L
C16, C21	multilayer ceramic chip capacitor	10 μF	Murata: GRM319R71H104KA01D
C22	multilayer ceramic chip capacitor	56 pF	ATC: ATC100B560FT500XTV
C23	electrolytic capacitor	470 μF, 63 V	Nichicon: UVZ1J471MHD1TO
R1, R2	SMD resistor	1 kΩ	0603
R3, R4	SMD resistor	5.1 Ω	0603
R5, R6	SMD resistor	3.9 Ω	0603
R_sh	SMD resistor	10 mΩ	Ohmite: FC4L110R010FER

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7.4 Graphical data



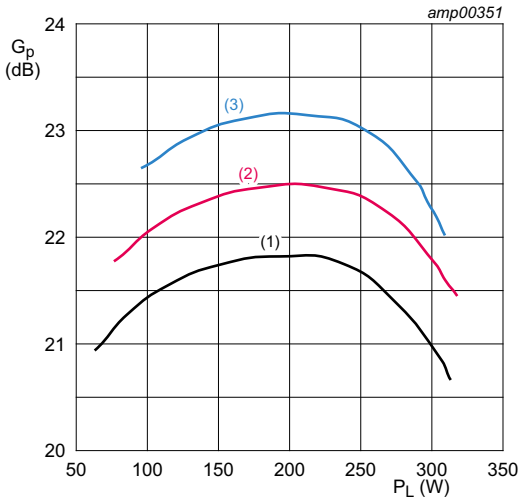
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 3. Output power as a function of input power; typical values



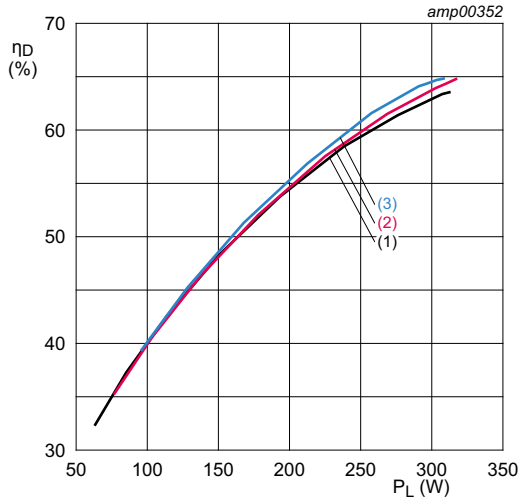
V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

(3) f = 1090 MHz

Fig 4. Power gain as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1060 MHz

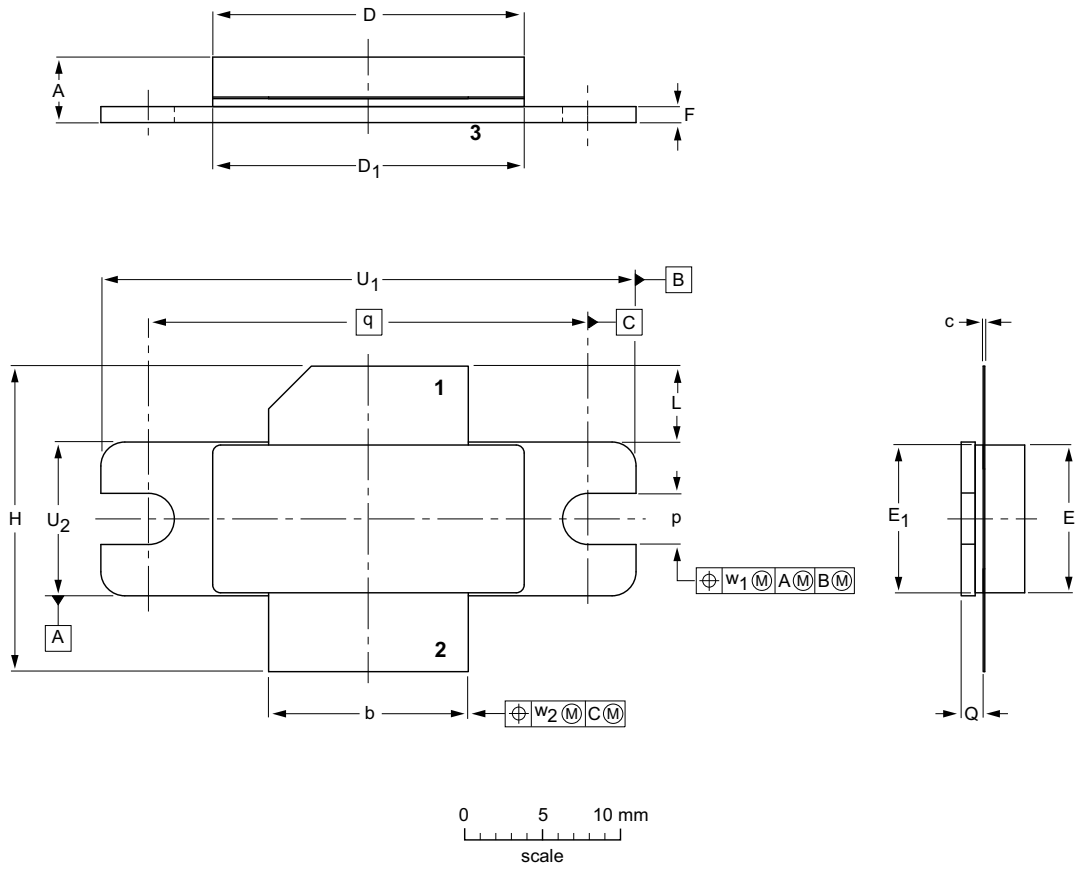
(3) f = 1090 MHz

Fig 5. Drain efficiency as a function of output power; typical values

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8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

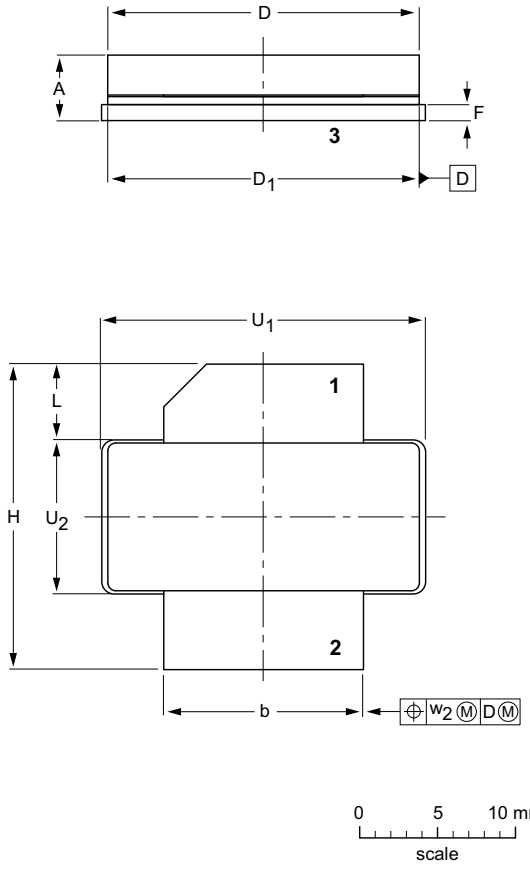
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 6. Package outline SOT502A

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Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

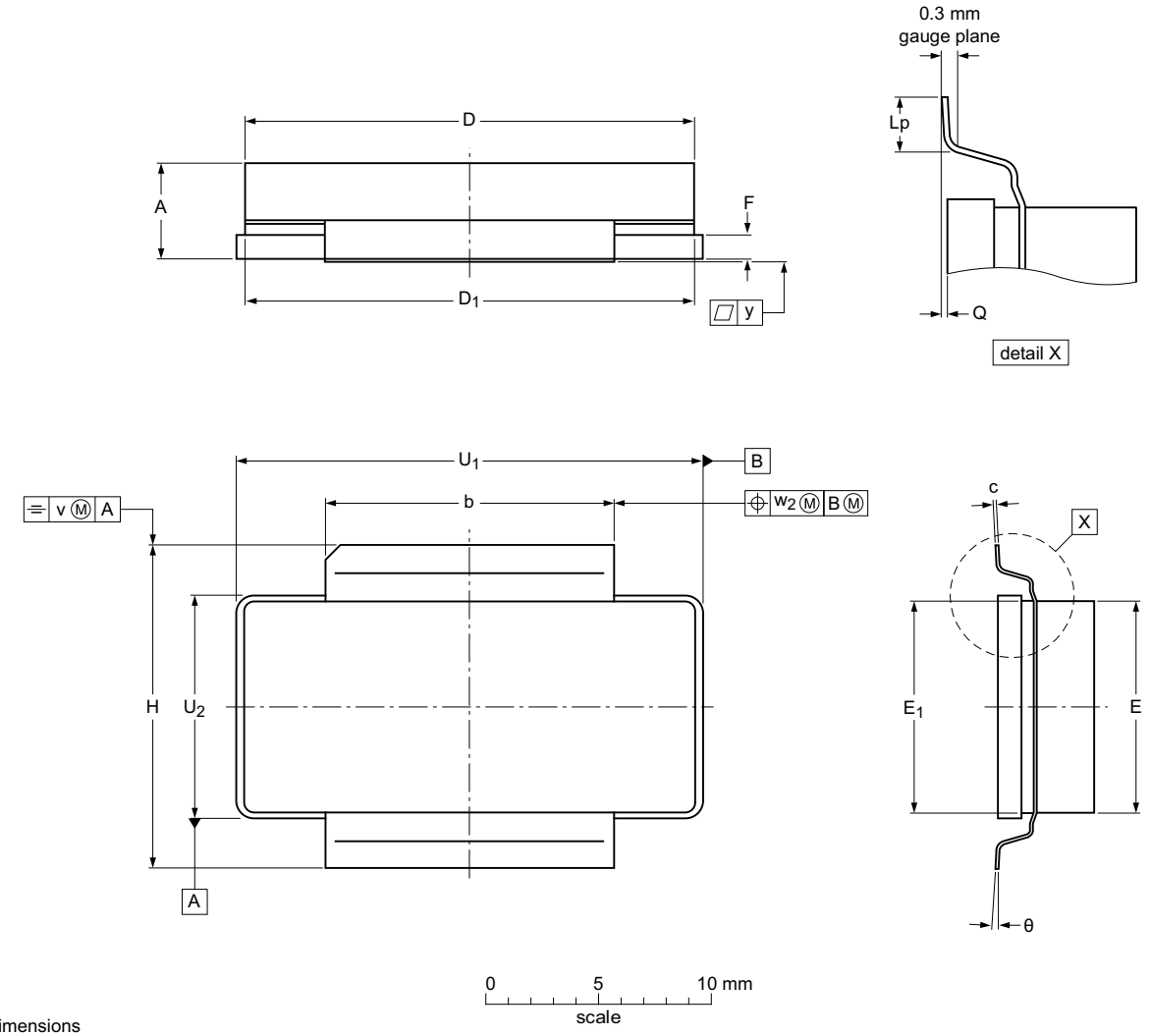
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 7. Package outline SOT502B

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Earless flanged ceramic package; 2 leads **SOT502E**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	θ
mm	max	4.72	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	0.195	20.70	9.91	0.25	0.25	0.15	7°
	nom																	
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	0.055	20.45	9.65				0°
inches	max	0.185	0.505	0.006	0.788	0.786	0.375	0.375	0.045	0.563	0.055	0.008	0.815	0.390	0.010	0.010	0.006	7°
	nom																	
	min	0.135	0.495	0.003	0.772	0.774	0.365	0.365	0.035	0.555	0.039	0.002	0.805	0.380				0°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

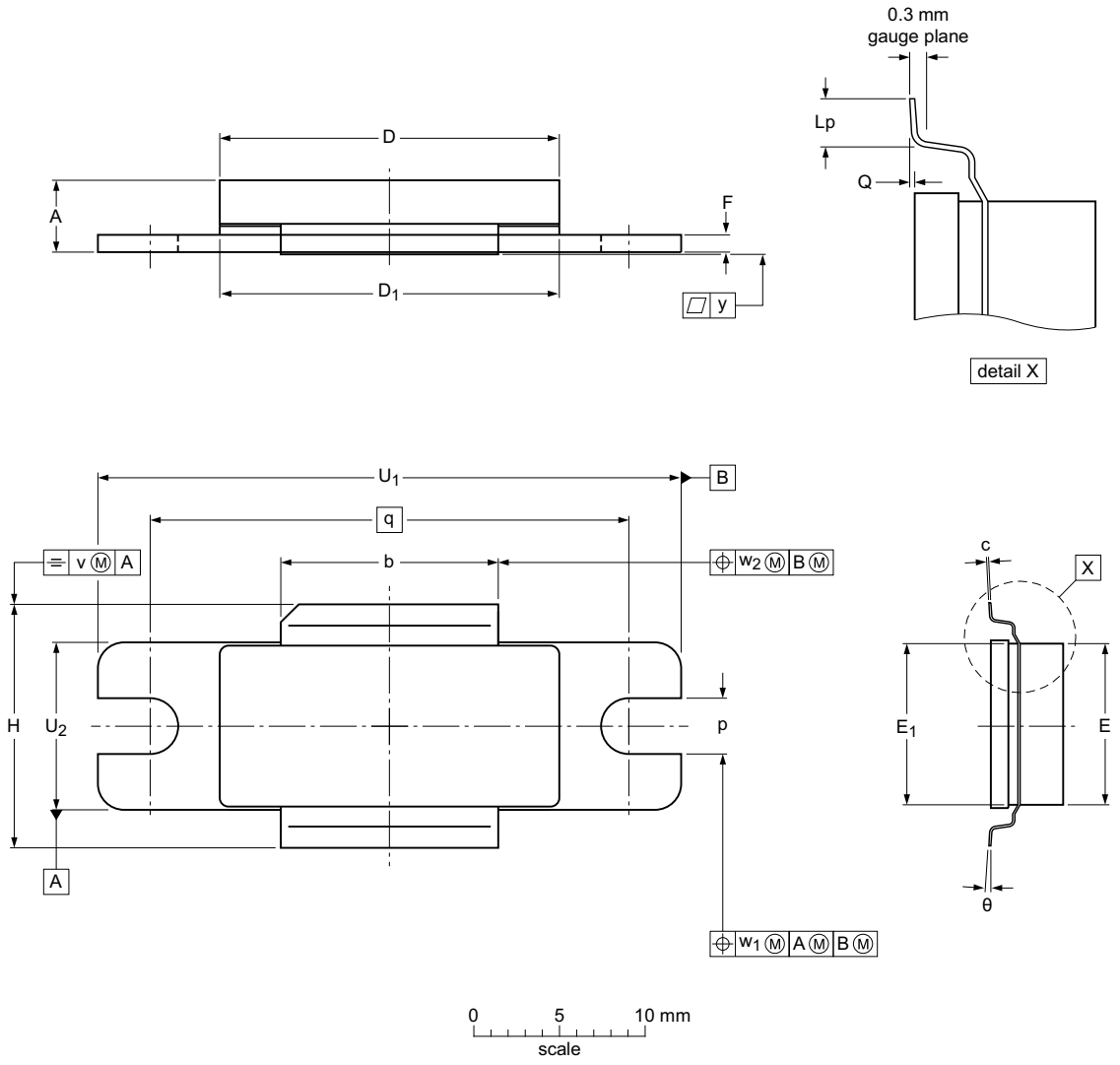
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502E						~~12-05-14~~ 12-05-30

Fig 8. Package outline SOT502E

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Eared flanged ceramic package; 2 leads; 2 mounting holes **SOT502F**



Dimensions (mm are the original dimensions)

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	p	Q	q	U_1	U_2	v	w_1	w_2	θ	U1
mm	max	4.70	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	3.38	0.195		34.16	9.91				7°	
	nom													27.94			0.25	0.25	0.25		0.15
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	3.12	0.055		33.91	9.65				0°	

sot502f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502F						~~14-02-19~~ 14-03-14

Fig 9. Package outline SOT502F

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9G1011L-300_LS-300_L-300G_LS-300G v.1	20170725	Product data sheet		-

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12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 25 July 2017
Document identifier: BLA9G1011L-300_LS-300_L-300G_LS-300G

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