BLC10G19XS-551AV

Power LDMOS transistor

AMPLEON

Rev. 1 — 6 March 2020 **Product data sheet**

1. Product profile

1.1 General description

550 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1930 MHz to 2000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 30 V; I_{Dq} = 370 mA (main); $V_{GS(amp)peak}$ = 0.85 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1930 to 2000	30	50	15	50.5	–31 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

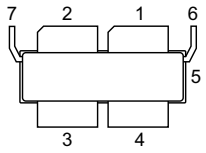
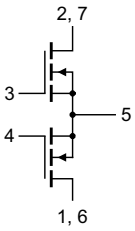
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1930 MHz to 2000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G19XS-551AV	-	air cavity plastic earless flanged package; 6 leads	SOT1258-5

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 370 mA (main); $V_{GS(amp)peak}$ = 0.85 V; T_{case} = 80 °C		
		P_L = 87 W	0.24	K/W
		P_L = 110 W	0.22	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 370 mA	-	2.0	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	33.49	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 6.3 A	-	17	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 6.3 A	-	73	126.67	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 380 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 1900 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	64	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 13.3 A	-	34	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 13.3 A	-	37.5	65.26	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1932.5 MHz; f_2 = 1997.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 370 mA (main); $V_{GS(amp)peak}$ = 0.85 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1930 MHz to 2000 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 107.2 W	14	15	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 107.2 W	-	−14	−8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 107.2 W	46	50.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 107.2 W	-	−31	−26	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 µs; δ = 10 %; f = 2000 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V; T_{case} = 25 °C; in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	500	570	-	W

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7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G19XS-551AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V; f = 1930 MHz; P_L = 195 W (5 dB OBO); 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1930	1.4 – j4.2	1.6 – j3.3	276	59.4	15.7
1960	1.6 – j4.4	1.6 – j3.3	275	58.6	15.8
1990	2.0 – j4.7	1.6 – j3.3	263	57.5	15.9
Maximum drain efficiency load					
1930	1.4 – j4.2	3.6 – j1.96	166	70.1	18.5
1960	1.6 – j4.5	3.6 – j1.96	163	70.2	18.4
1990	2.0 – j4.7	3.0 – j2.42	182	68.7	18.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1600 mA (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1930	1.4 – j4.6	1.0 – j3.7	497	56.2	16.6
1960	1.9 – j4.8	1.5 – j3.1	502	59.0	17.2
1990	2.3 – j5.2	1.4 – j3.4	493	55.5	17.1
Maximum drain efficiency load					
1930	1.4 – j4.6	1.6 – j3.3	430	62.7	17.7
1960	1.9 – j4.8	2.0 – j2.6	421	62.8	17.9
1990	2.3 – j5.2	2.1 – j3.0	437	61.7	18.0

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

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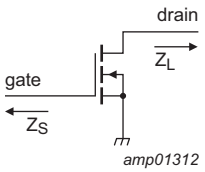
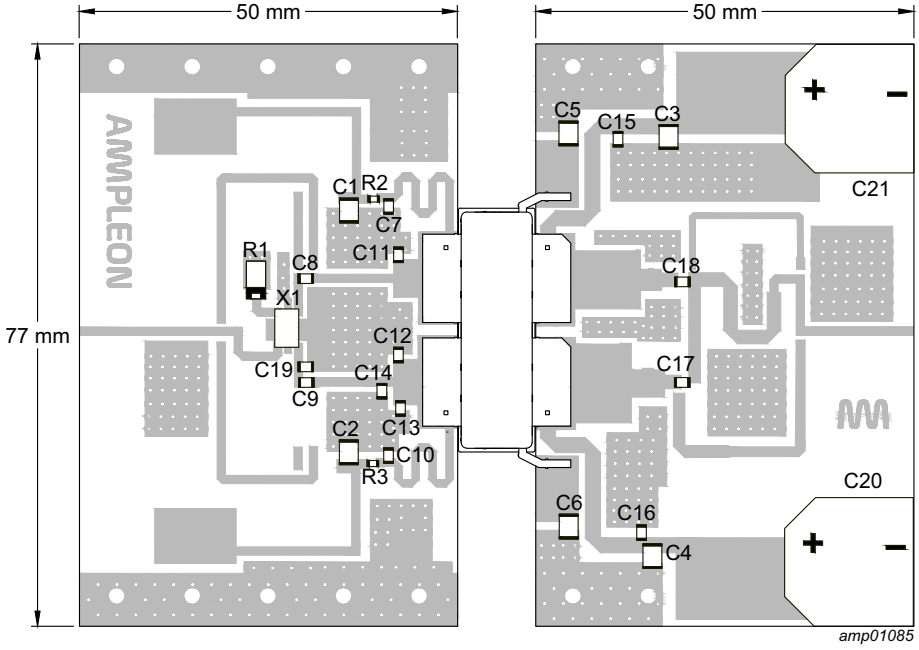


Fig 1. Definition of transistor impedance

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm; thickness copper plating = 35 μm both sides.

See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	10 μF, 50 V [1]	
C5, C6	multilayer ceramic chip capacitor	1 μF, 50 V [1]	
C7, C8, C9, C10	multilayer ceramic chip capacitor	15 pF [2]	
C11, C12	multilayer ceramic chip capacitor	2.0 pF [2]	
C13	multilayer ceramic chip capacitor	0.5 pF [2]	
C14	multilayer ceramic chip capacitor	0.8 pF [2]	
C15, C16, C17	multilayer ceramic chip capacitor	15 pF [3]	
C18	multilayer ceramic chip capacitor	3.3 pF [3]	
C19	multilayer ceramic chip capacitor	1 pF [2]	
C20, C21	electrolytic capacitor	1000 μF, 100 V	
R1	resistor	50 Ω	SMD 1206
R2, R3	resistor	5.6 Ω	SMD 0805
X1	hybrid coupler		X3C20F1-02S

[1] Murata or capacitor of same quality.

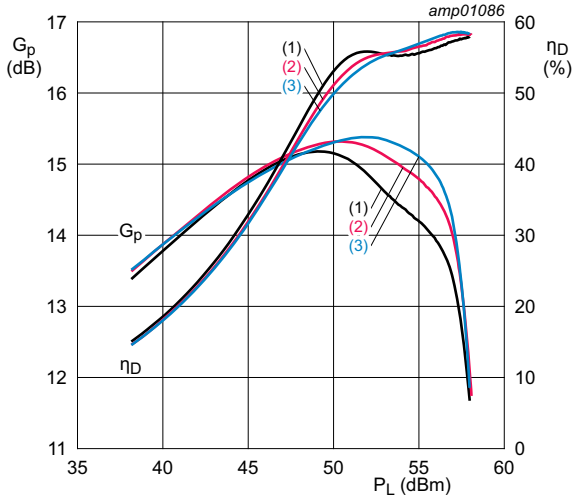
[2] American Technical Ceramics type 600F or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

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7.4 Graphical data

7.4.1 Pulsed CW



V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V; t_p = 100 μs; δ = 10 %.

(1) f = 1930 MHz

(2) f = 1965 MHz

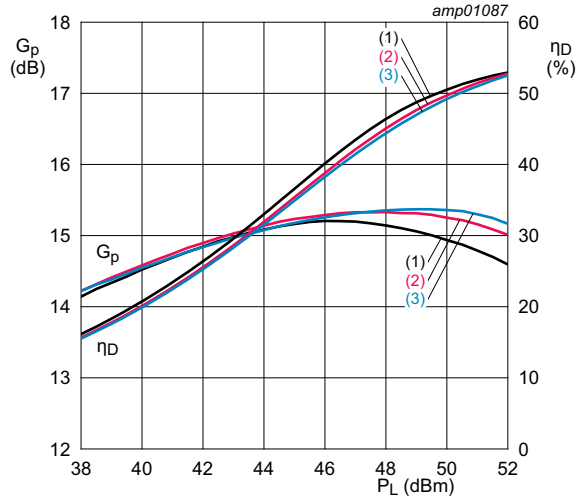
(3) f = 2000 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

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7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.



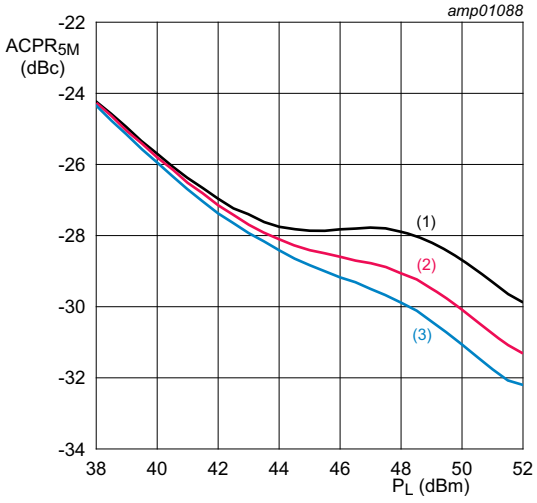
V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V.

(1) f = 1930 MHz

(2) f = 1965 MHz

(3) f = 2000 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



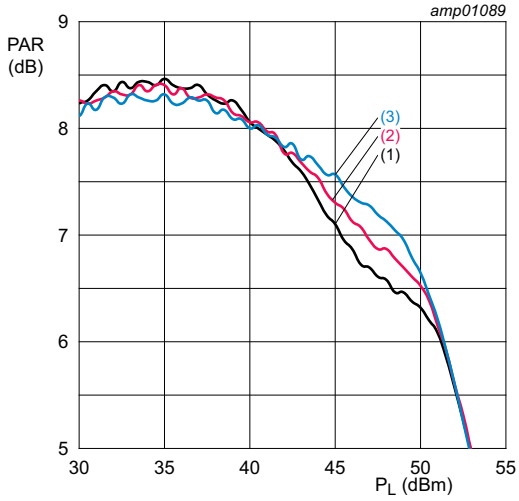
V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V.

(1) f = 1930 MHz

(2) f = 1965 MHz

(3) f = 2000 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V.

(1) f = 1930 MHz

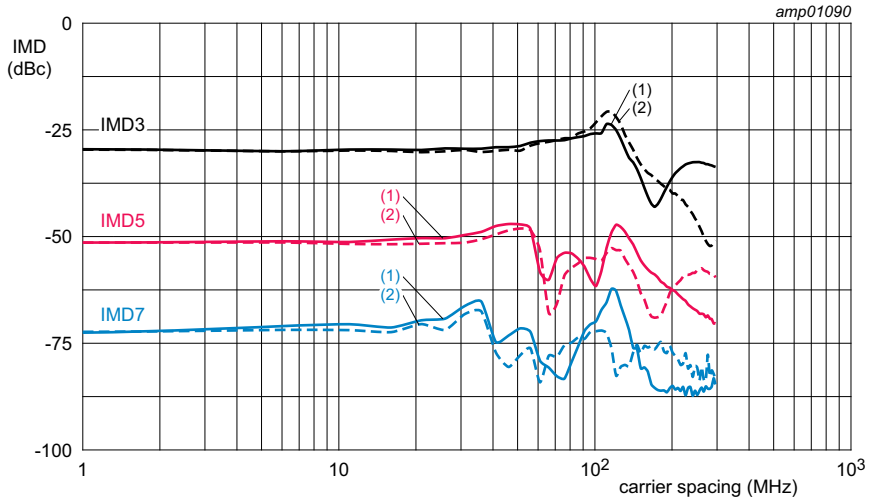
(2) f = 1965 MHz

(3) f = 2000 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

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7.4.3 2-Tone VBW



V_{DS} = 30 V; I_{Dq} = 370 mA; $V_{GS(amp)peak}$ = 0.85 V; f = 1965 MHz

(1) IMD low

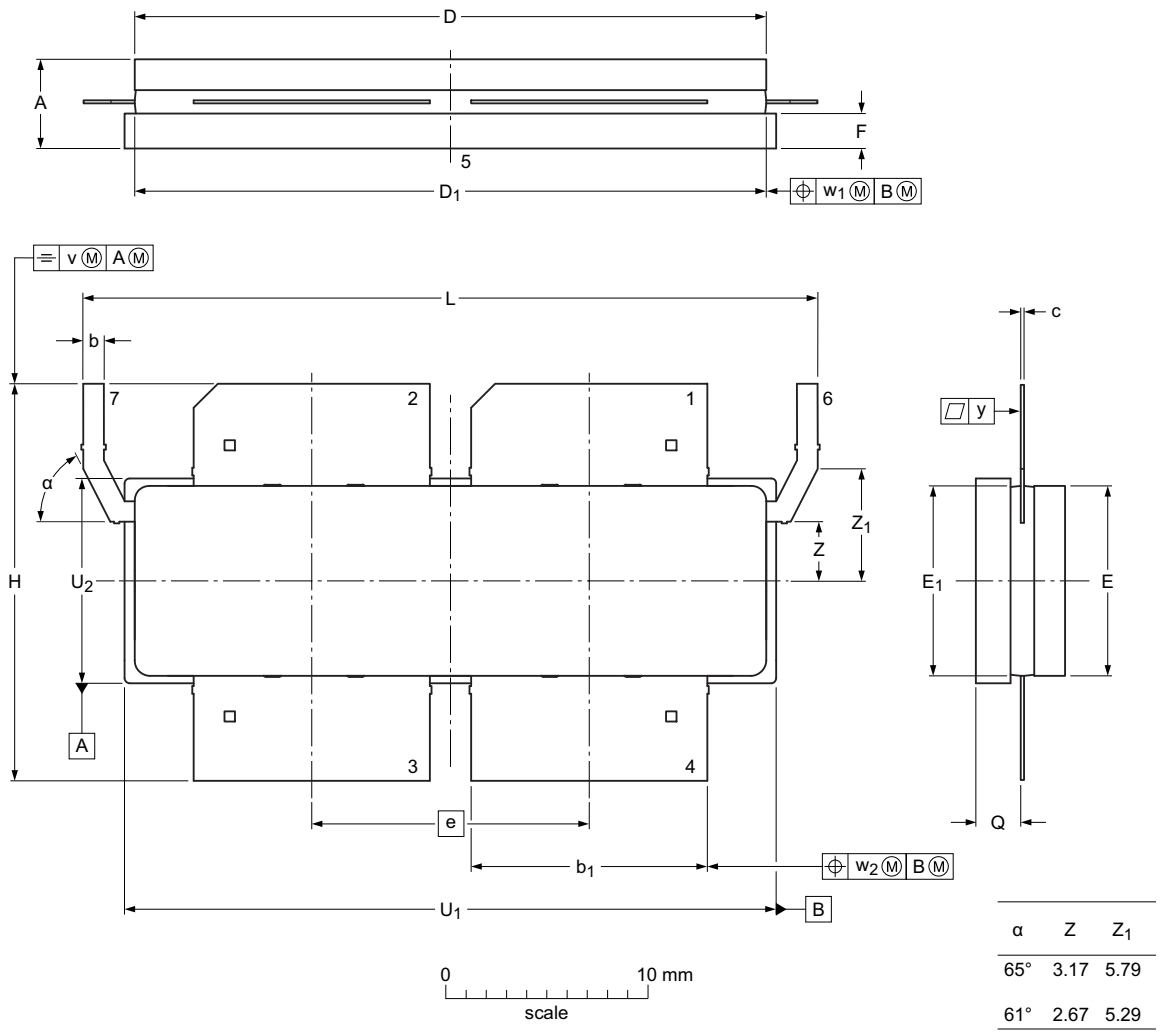
(2) IMD high

Fig 7. VBW capability

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8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-5**



α	Z	Z_1
65°	3.17	5.79
61°	2.67	5.29

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50		36.42	1.73	19.71	2.25	32.33	10.23	0.5	0.5	0.5	0.1
	nom									13.72										
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	19.51	2.03	32.13	10.03				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-5_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-5						18-10-01

Fig 8. Package outline SOT1258-5

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G19XS-551AV v.1	20200306	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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