BLC10G27XS-400AVT

Power LDMOS transistor

AMPLEON

Rev. 1 — 24 June 2021 **Product data sheet**

1. Product profile

1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2496 MHz to 2690 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 28 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.9 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2496 to 2690	28	63	14.7	46.2	–31.5 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

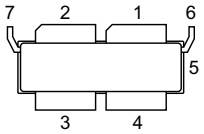
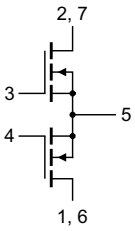
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2496 MHz to 2690 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G27XS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.9 V; T_{case} = 80 °C		
		P_L = 63 W	0.27	K/W
		P_L = 79 W	0.24	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.44 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 144 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 700 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	27	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.2 A	-	15	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 5.04 A	-	84	155.8	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.62 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 262 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1310 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	47	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 13.1 A	-	29	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 9.17 A	-	46	90.1	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2492.5 MHz; f_2 = 2687.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 700 mA (main); $V_{GS(amp)peak}$ = 1.2 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2490 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 56.2 W	12.4	13.3	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 56.2 W	-	–11	–7	dB
η_D	drain efficiency	$P_{L(AV)}$ = 56.2 W	41	45	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 56.2 W	-	–28	–24	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2492.5 MHz; f_2 = 2687.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 700 mA (main); $V_{GS(amp)peak}$ = 1.2 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency from 2490 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 90 W	6.2	6.8	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 90 W	368	430	-	W

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7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G27XS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 750 mA (main); $V_{GS(amp)peak}$ = 0.9 V; f = 2500 MHz; P_L = 169 W (5 dB OBO); with 1-carrier W-CDMA; 100 % clipping.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 720 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	2.1 – j5.2	2.4 – j4.6	182	57.0	14.8
2600	3.6 – j5.4	2.2 – j4.5	182	55.6	14.7
2700	5.5 – j3.9	2.2 – j4.5	182	56.3	14.9
Maximum drain efficiency load					
2500	2.6 – j5.3	5.3 – j3.9	124	64.5	16.8
2600	4.2 – j5.0	4.1 – j3.2	134	64.1	16.6
2700	5.4 – j2.6	3.3 – j2.5	126	63.7	17.0

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1310 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	1.4 – j4.8	3.2 – j4.2	339	56.5	14.6
2600	2.5 – j5.2	3.1 – j4.3	331	54.6	14.6
2700	4.4 – j4.5	3.1 – j4.2	318	53.8	14.8
Maximum drain efficiency load					
2500	1.5 – j4.8	3.0 – j1.9	258	64.44	16.5
2600	2.7 – j5.1	2.5 – j2.2	249	62.13	16.5
2700	4.4 – j4.0	2.1 – j2.6	244	60.28	16.5

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

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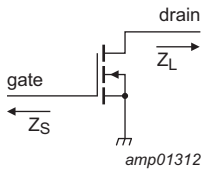


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 720 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2500	2.6 – j4.6	2.7 – j5.4	161	36.6	17.4
2600	3.6 – j4.8	2.5 – j4.9	168	35.1	17.4
2700	5.1 – j3.3	2.4 – j4.4	167	35.1	17.9

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 56 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 720 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2500	2.6 – j4.6	5.6 – j3.0	110	45.6	19.5
2600	3.6 – j4.8	5.7 – j3.2	102	50.4	19.3
2700	5.1 – j3.3	5.8 – j3.3	99	48.0	18.6

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 56 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 1310 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2500	1.4 – j4.6	3.3 – j4.5	321	24.2	17.0
2600	2.3 – j5.0	3.1 – j4.1	317	24.5	17.3
2700	4.1 – j4.6	2.8 – j3.6	304	25.9	17.9

[1] Z_S and Z_L defined in Figure 1.

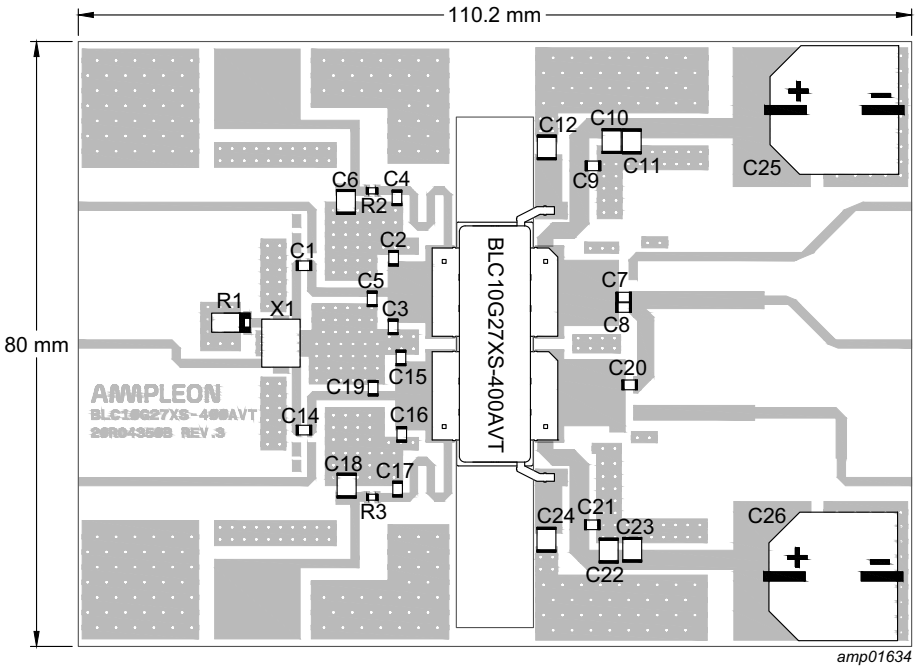
[2] At $P_{L(AV)}$ = 56 W.

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Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
2500	1.0 – j3.0
2600	0.6 – j0.8
2700	0.4 + j0.4

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 15 for a list of components.

Fig 2. Component layout for asymmetrical Doherty production test circuit

Table 15. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C4, C14, C17	multilayer ceramic chip capacitor	6.8 pF	Murata: HiQ 0805
C2, C3	multilayer ceramic chip capacitor	0.5 pF	Murata: HiQ 0805
C5	multilayer ceramic chip capacitor	1.2 pF	Murata: HiQ 0805
C6, C10, C11, C12, C18, C22, C23, C24	multilayer ceramic chip capacitor	10 μF, 100 V, X7S	Murata: 1210
C7, C8	multilayer ceramic chip capacitor	2.4 pF	Murata: HiQ 0805
C9, C21	multilayer ceramic chip capacitor	8.2 pF	Murata: HiQ 0805
C15, C16	multilayer ceramic chip capacitor	0.9 pF	Murata: HiQ 0805
C19	multilayer ceramic chip capacitor	0.6 pF	Murata: HiQ 0805

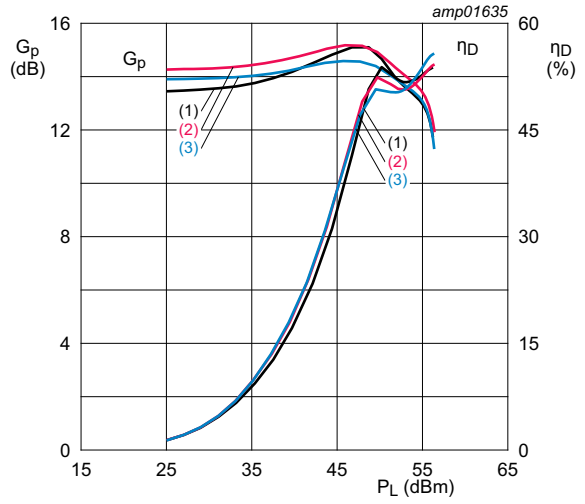
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Table 15. List of components *...continued*
For test circuit see Figure 2.

Component	Description	Value	Remarks
C20	multilayer ceramic chip capacitor	5.6 pF	Murata: HiQ 0805
C25, C26	electrolytic capacitor	470 μF, 63 V	Panasonic: EEVFK1J471M
R1	resistor	50 Ω, 16 W	Anaren: C16A50Z4
R2, R3	resistor	4.7 Ω, 1 %	SMD 0805
X1	hybrid coupler	2 dB	Anaren: X3C25P1-02S

7.5 Graphical data

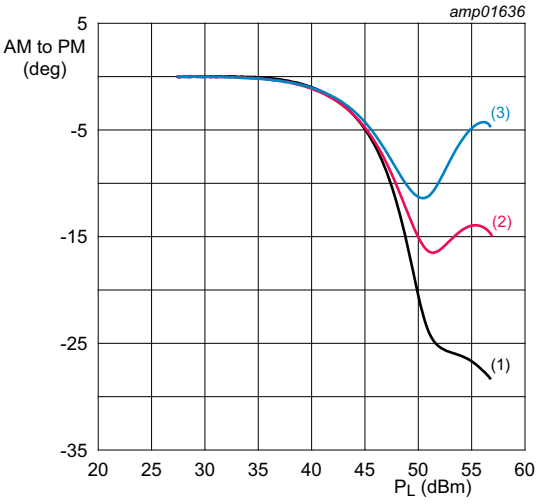
7.5.1 Pulsed CW



V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V; t_p = 100 μs; δ = 10 %.

(1) f = 2490 MHz
(2) f = 2590 MHz
(3) f = 2690 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V; t_p = 100 μs; δ = 10 %.

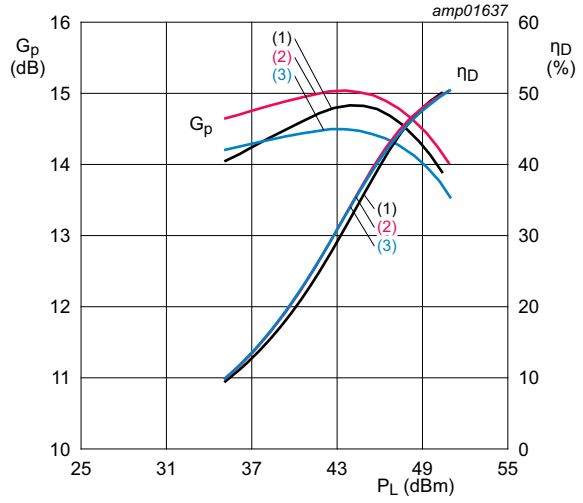
(1) f = 2490 MHz
(2) f = 2590 MHz
(3) f = 2690 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

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7.5.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; test model 1; PAR = 9.9 dB at 0.01 % probability on CCDF.



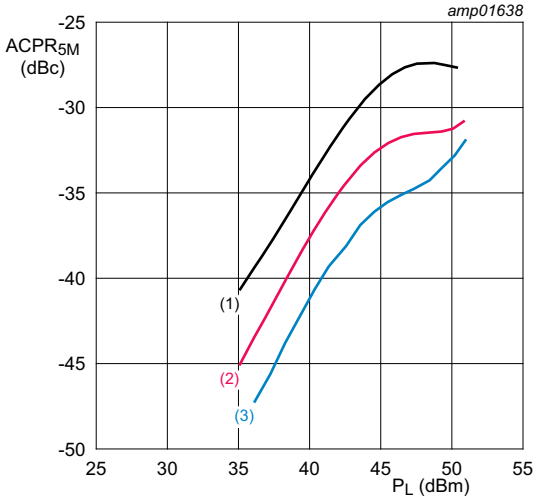
T_{case} = 25 °C; V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V.

(1) f = 2490 MHz

(2) f = 2590 MHz

(3) f = 2690 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



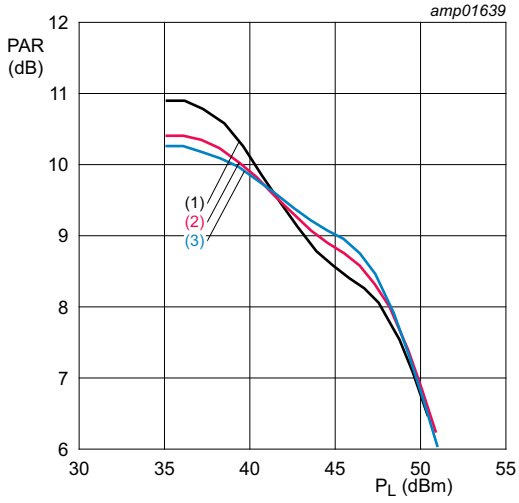
T_{case} = 25 °C; V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V.

(1) f = 2490 MHz

(2) f = 2590 MHz

(3) f = 2690 MHz

Fig 6. Adjacent channel power ratio as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V.

(1) f = 2490 MHz

(2) f = 2590 MHz

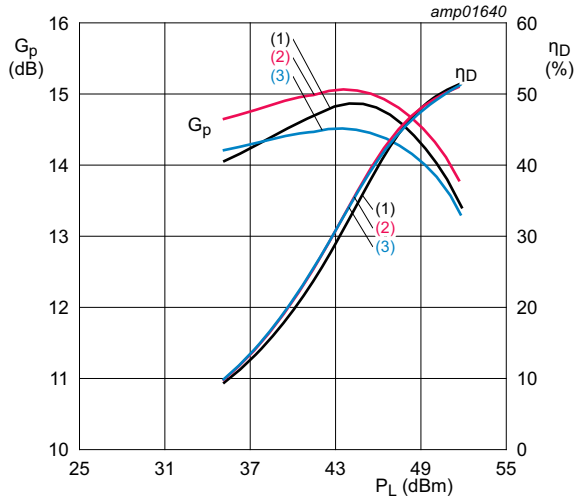
(3) f = 2690 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

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7.5.3 1-Carrier LTE

Test signal: 1-carrier LTE 10 MHz; PAR = 6.8 dB at 0.01 % probability on CCDF.



T_{case} = 25 °C; V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V.

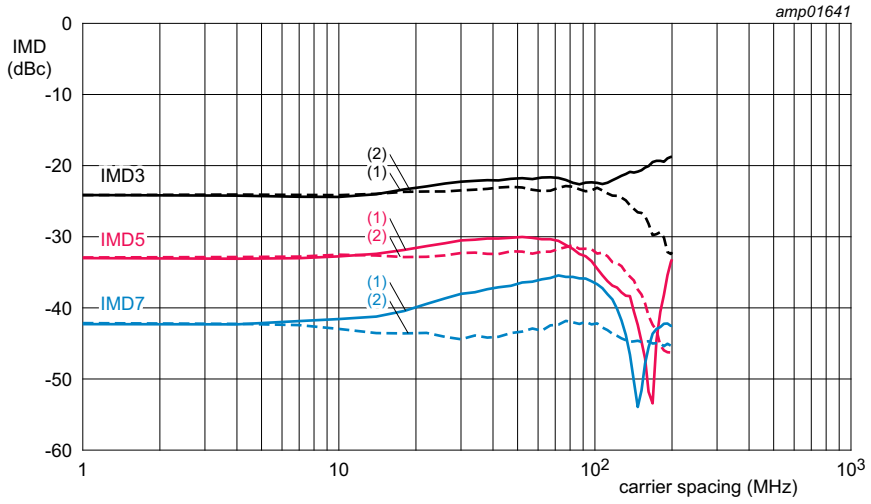
(1) f = 2490 MHz

(2) f = 2590 MHz

(3) f = 2690 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values

7.5.4 2-Tone VBW



V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V; P_L = 48.0 dBm; f = 2590 MHz.

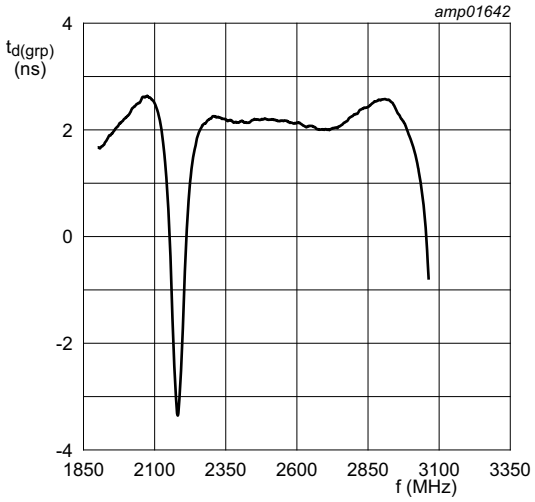
(1) IMD low

(2) IMD high

Fig 9. VBW capability

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7.5.5 Group delay



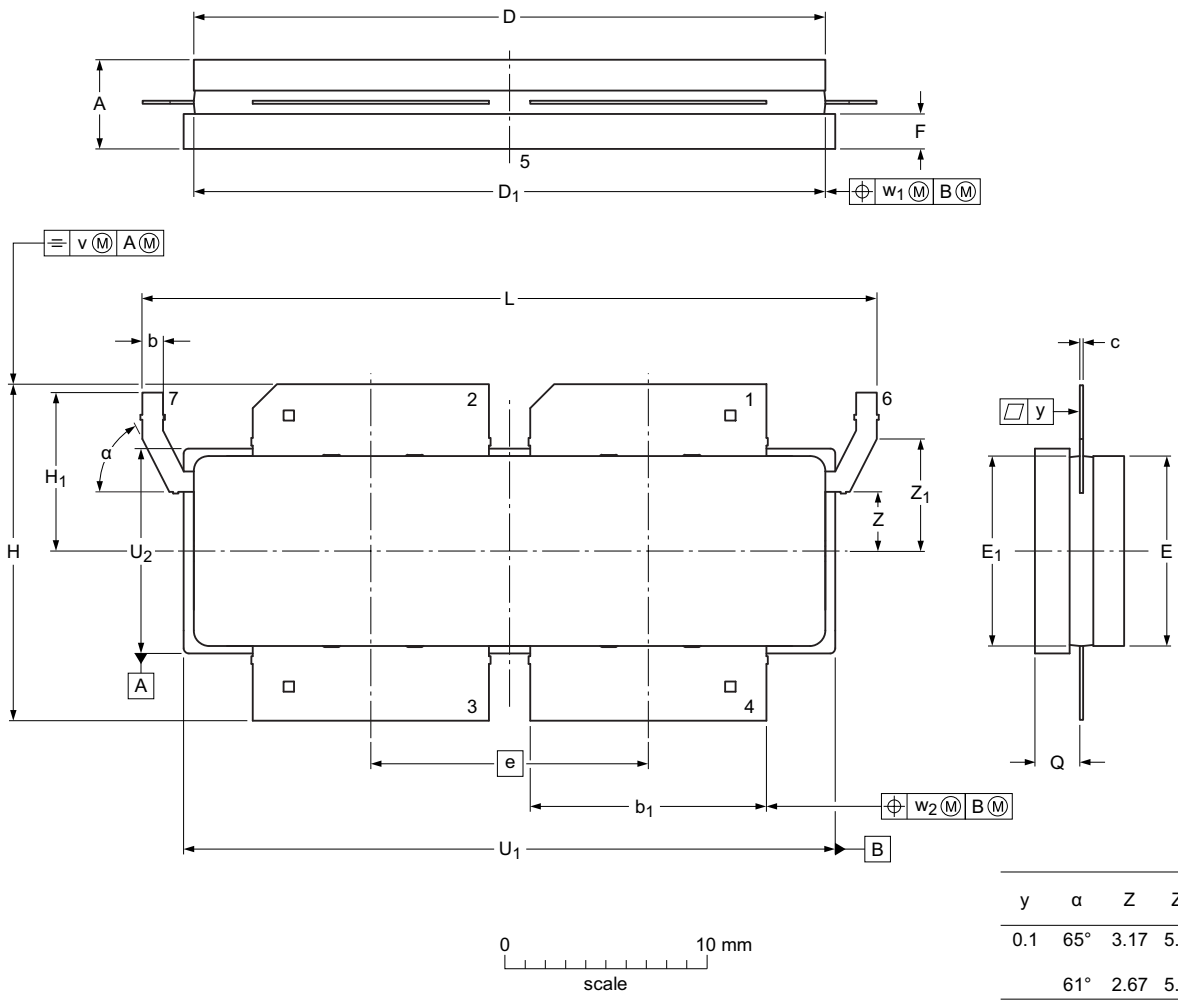
V_{DS} = 28 V; V_{GS1} = 2.18 V; I_{Dq1} = 750 mA; V_{GS2} = 0.90 V; P_L = 8.4 dBm.

Fig 10. Group delay time as a function of frequency; typical values

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8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-4**



y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50	13.72	36.42	1.73	16.71	8.12	2.25	32.33	10.23	0.5	0.5	0.5
	nom																			
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	16.51	7.62	2.03	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-4						17-08-31

Fig 11. Package outline SOT1258-4

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G27XS-400AVT v.1	20210624	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
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Date of release: 24 June 2021
Document identifier: BLC10G27XS-400AVT

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