BLC2425M10LS500P

Power LDMOS transistor

AMPLEON

Rev. 2 — 21 March 2019 **Product data sheet**

1. Product profile

1.1 General description

500 W LDMOS based power transistor suitable for use in a variety of commercial and consumer cooking, industrial, scientific and medical applications at frequencies from 2400 MHz to 2500 MHz.

The BLC2425M10LS500P is designed for high-power CW applications and is assembled in a high performance plastic package.

Table 1. Typical performance

RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C in a class-AB application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	500	15.0	67.5
CW pulsed [1]	2450	32	500	15.0	67

[1] t_p = 100 µs; δ = 10 %

1.2 Features and benefits

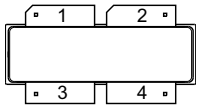
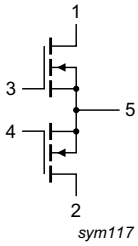
- High efficiency
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Input and output internally matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as commercial and consumer cooking, industrial, scientific and medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
flange	source		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC2425M10LS500P	-	air cavity plastic earless flanged package; 4 leads	SOT1250-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 75 °C; P_L = 500 W	0.17	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C, per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 32 V; I_D = 20 mA	1.75	2.2	2.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	4.2	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	59.3	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	40	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15.2 A	-	21	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.64 A	-	45.5	-	mΩ

Table 7. RF characteristics

Test signal: CW pulsed at 2450 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 10 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 500 W	13.2	14.5	-	dB
RL_{in}	input return loss	P_L = 500 W	-	–18	–5	dB
η_D	drain efficiency	P_L = 500 W	64	67	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLC2425M10LS500P is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 500 W (CW); f = 2450 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data half device. Typical values unless otherwise specified. I_{Dq} = 20 mA; V_{DS} = 32 V.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
2400	2.95 – j6.51	2.3 – j2.6
2450	4.50 – j6.95	2.1 – j2.4
2500	5.58 – j5.66	2.2 – j2.2

[1] Z_S and Z_L defined in Figure 1.

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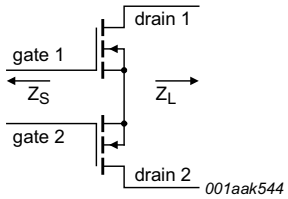
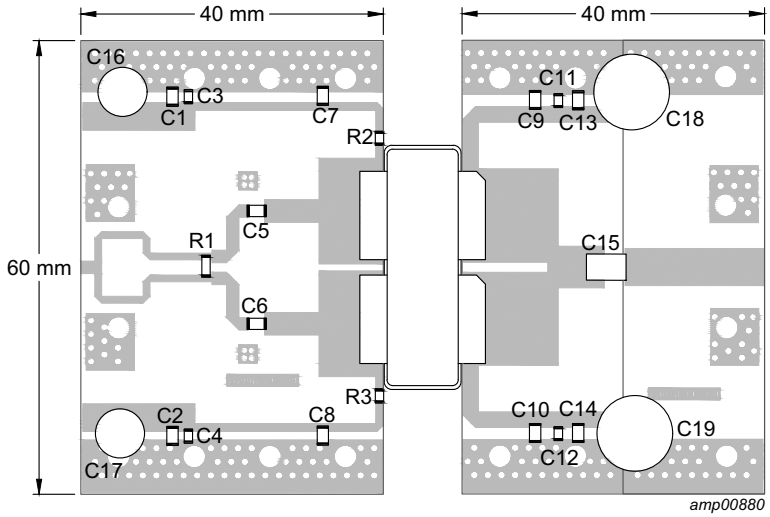


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers TC350 // RT/Duroid 5880 (outer right output side); thickness = 0.762 mm // 1.5748 mm; top/bottom copper.

See Table 9 for a list of components.

Fig 2. Component layout for production test circuit

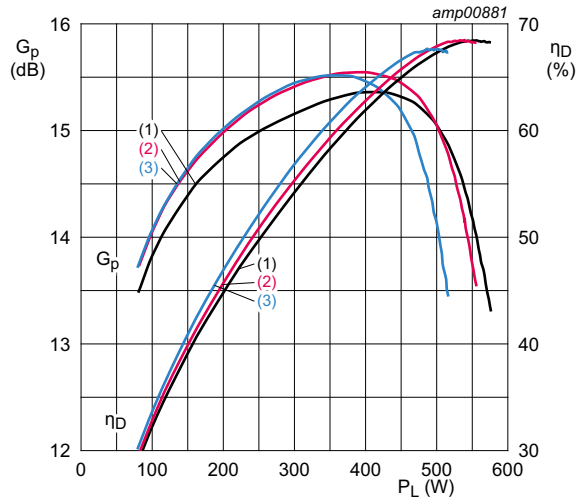
Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1 µF, 50 V	SMD 1210
C3, C4, C11, C12	multilayer ceramic chip capacitor	1 nF, 50 V	SMD 0805
C5, C6, C7, C8	multilayer ceramic chip capacitor	22 pF	ATC 800A
C9, C10	multilayer ceramic chip capacitor	22 pF	ATC 800B
C13, C14	multilayer ceramic chip capacitor	4.7 µF, 50 V	SMD 1210
C15	mica capacitor	12 pF	MIN02
R1	resistor	100 Ω	SMD 1206
R2, R3	resistor	10 Ω	SMD 0603
C16, C17	electrolytic capacitor	22 µF, 63 V	
C18, C19	electrolytic capacitor	470 µF, 63 V	

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7.4 Graphical data



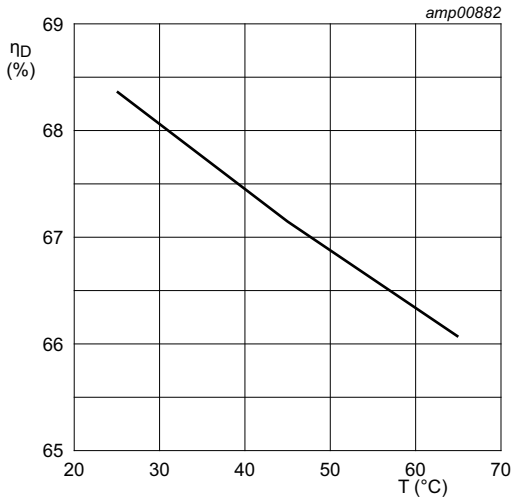
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

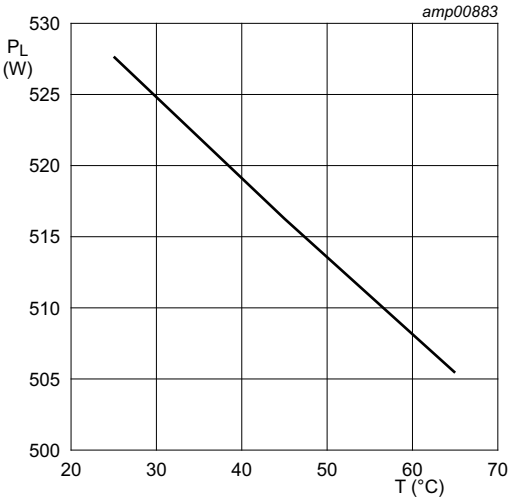
(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



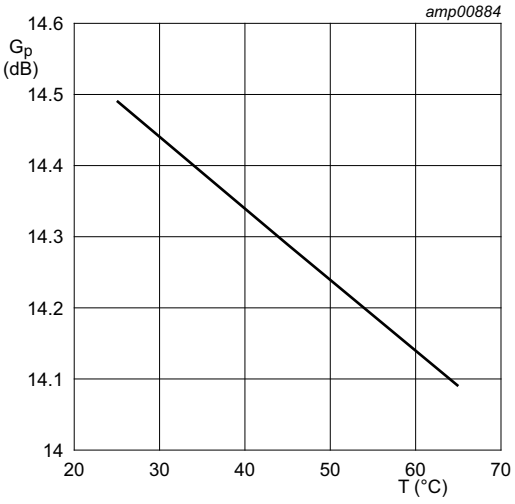
V_{DS} = 32 V; I_{Dq} = 20 mA: f = 2450 MHz; at $P_{L(1dB)}$.

Fig 4. Drain efficiency as a function of temperature; typical values



V_{DS} = 32 V; I_{Dq} = 20 mA: f = 2450 MHz; at $P_{L(1dB)}$.

Fig 5. Output power as a function of temperature; typical values



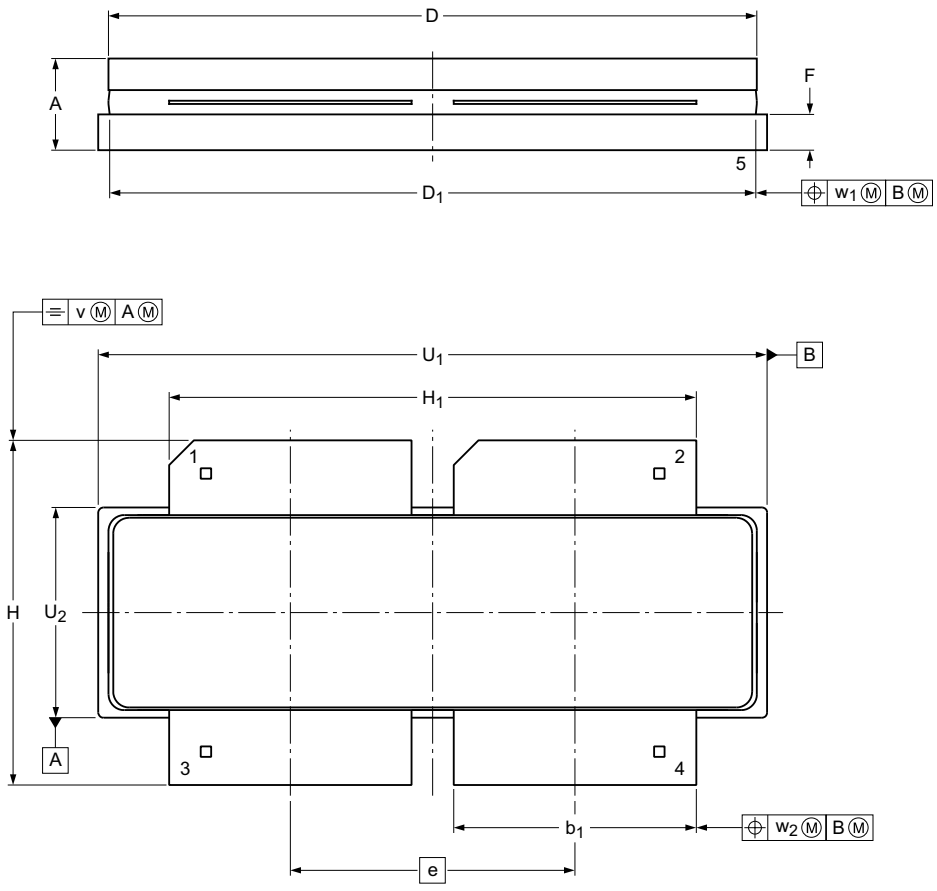
V_{DS} = 32 V; I_{Dq} = 20 mA: f = 2450 MHz; at $P_{L(1dB)}$.

Fig 6. Power gain as a function of temperature; typical values

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8. Package outline

Plastic earless flanged cavity package; 4 leads **SOT1250-1**



Dimensions (mm dimensions are derived from the original inch dimension)

Unit		A	b_1	c	D	D_1	E	E_1	e	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2	y
mm	max	4.65	11.79	0.18	31.44	31.34	9.60	9.50		1.83	16.71	25.50	2.33	32.33	10.23	0.50	0.50	0.50	0.10
	nom								13.72										
	min	4.18	11.58	0.13	31.04	31.14	9.20	9.30		1.63	16.51	25.30	2.13	32.13	10.03				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1250-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1250-1						~~13-09-03~~ 16-05-20

Fig 7. Package outline SOT1250-1

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC2425M10LS500P v.2	20190321	Product data sheet	-	BLC2425M10LS500P v.1
Modifications	• Table 9 on page 4: corrected value C18 and C19			
BLC2425M10LS500P v.1	20190114	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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