BLC9G20LS-120VT

Power LDMOS transistor

Rev. 2 — 5 July 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

120 W LDMOS power transistor with enhanced video bandwidth for base station applications at frequencies from 1805 MHz to 1995 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	700	28	30	18.5	31	–31 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

1.2 Features and benefits

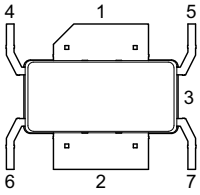
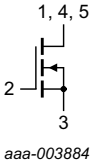
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable enhanced video bandwidth performance (75 MHz typical)
- Designed for broadband operation (1805 MHz to 1995 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1995 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		
4	video decoupling		
5	video decoupling		
6	n.c.		
7	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20LS-120VT	-	air cavity plastic earless flanged package; 6 leads	SOT1271-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 30 W	0.47	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 120 mA	1.5	1.9	3.1	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 700 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	25	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 6 A	-	4.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 4.2 A	-	0.12	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; 3GPP test model 1 with 64 DPCH; PAR = 8.4 dB at 0.01 % probability on the CCDF; f_1 = 1807.5 MHz; f_2 = 1812.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 700 mA; T_{case} = 25 °C; unless otherwise specified; in a water cooled class-AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 30 W	17.8	18.5	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 30 W	29	31	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 30 W	-	−14	−9	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 30 W	-	−31	−29	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; RF performance at V_{DS} = 28 V; I_{Dq} = 700 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB test circuit at a frequency of 1877.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 59 W	4.00	4.67	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 59 W	145	172	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLC9G20LS-120VT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 700 mA; P_L = 100 W (CW); f = 1805 MHz.

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7.2 Impedance information

Table 9. Typical impedance of device

Measured load-pull data of device; I_{Dq} = 700 mA; V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1805	1.1 – j5.7	1.3 – j2.9	189.6	61.8	15.7
1840	1.4 – j6.2	1.3 – j2.9	191.7	63.1	15.8
1880	1.8 – j6.7	1.3 – j2.9	189.9	61.6	16.0
1930	2.7 – j7.8	1.3 – j3.2	185.6	61.3	16.0
1960	3.8 – j8.4	1.3 – j3.2	182.3	61.2	16.5
1990	5.4 – j9.1	1.3 – j3.2	180.4	61.6	16.7
Maximum drain efficiency load					
1805	1.1 – j5.7	2.6 – j1.7	129.2	73.6	18.3
1840	1.4 – j6.2	2.6 – j1.7	127.3	74.7	18.6
1880	1.8 – j6.7	2.2 – j1.8	133.3	74.2	18.5
1930	2.7 – j7.8	2.2 – j1.8	123.5	72.8	19.0
1960	3.8 – j8.4	2.0 – j2.1	135.1	72.1	18.8
1990	5.4 – j9.1	2.0 – j2.1	129.5	71.8	19.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

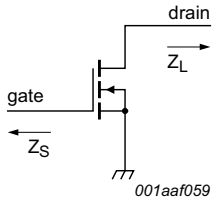
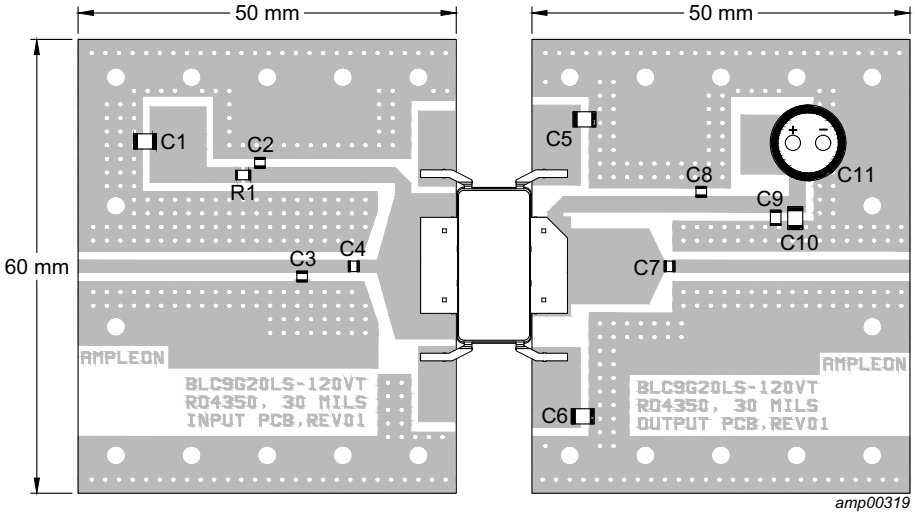


Fig 1. Definition of transistor impedance

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350 with a thickness of 0.76 mm. See Table 10 for a list of components.

Fig 2. Component layout

Table 10. List of components

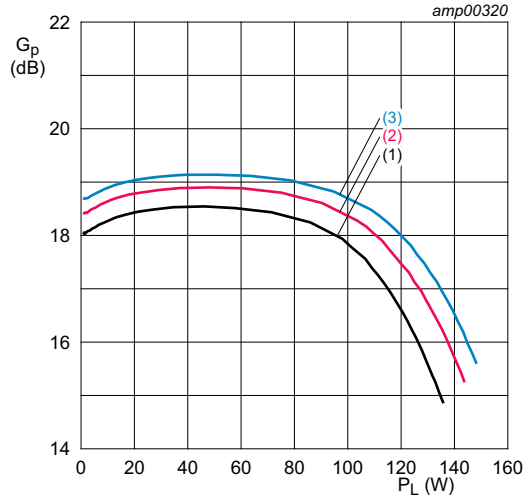
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C2	multilayer ceramic chip capacitor	43 pF	ATC 800A
C3	multilayer ceramic chip capacitor	1.3 pF	ATC 800A
C4	multilayer ceramic chip capacitor	2.7 pF	ATC 800A
C5	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C6	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C7	multilayer ceramic chip capacitor	1.5 pF	ATC 800A
C8	multilayer ceramic chip capacitor	43 pF	ATC 800A
C9	multilayer ceramic chip capacitor	220 nF	Murata
C10	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata
C11	electrolytic capacitor	470 μF, 63 V	
R1	chip resistor	4.7 Ω	SMD 0805

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7.4 Graphical data

7.4.1 Pulsed CW



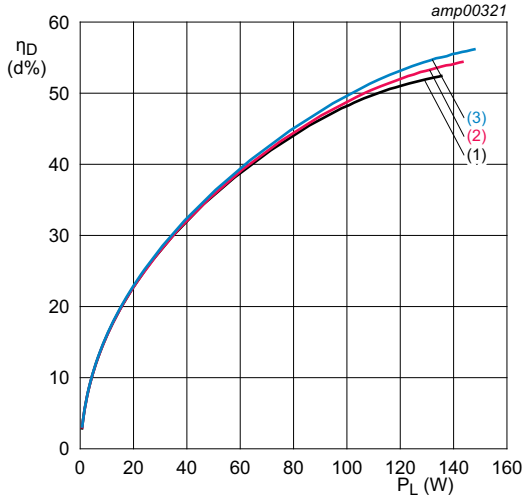
V_{DS} = 28 V; I_{Dq} = 700 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 3. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1810 MHz

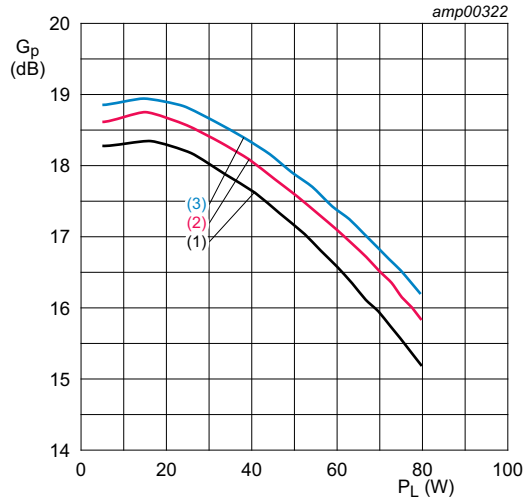
(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 4. Drain efficiency as a function of output power; typical values

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7.4.2 IS-95



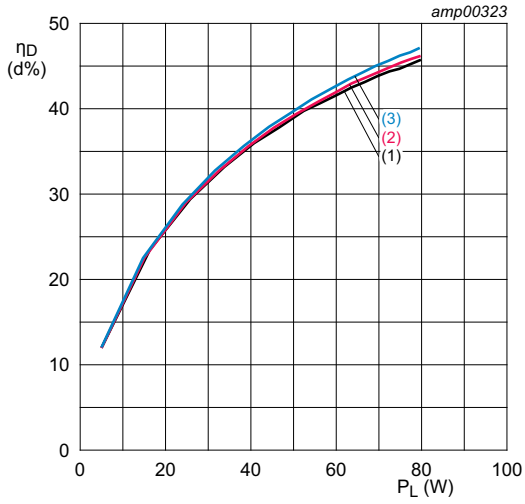
V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 5. Power gain as a function of output power; typical values



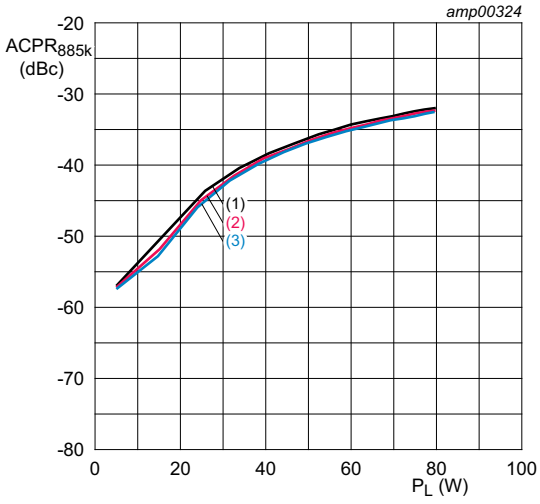
V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 6. Drain efficiency as a function of output power; typical values



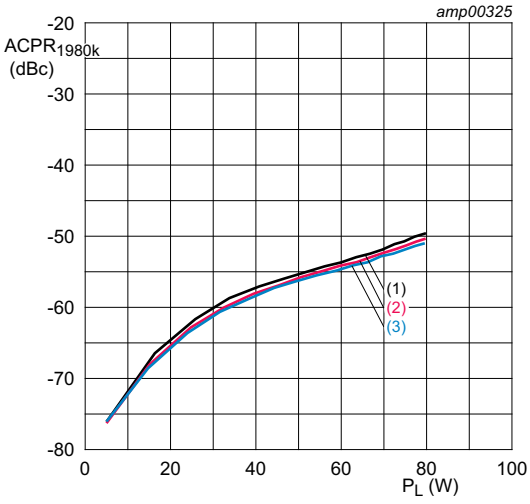
V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 7. Adjacent channel power ratio (885 kHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA.

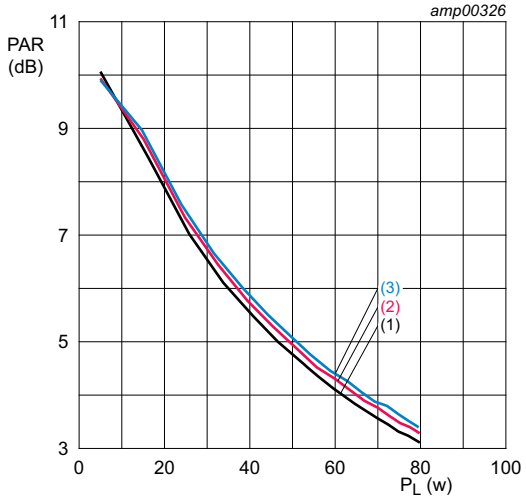
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 8. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values

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V_{DS} = 28 V; I_{Dq} = 700 mA.

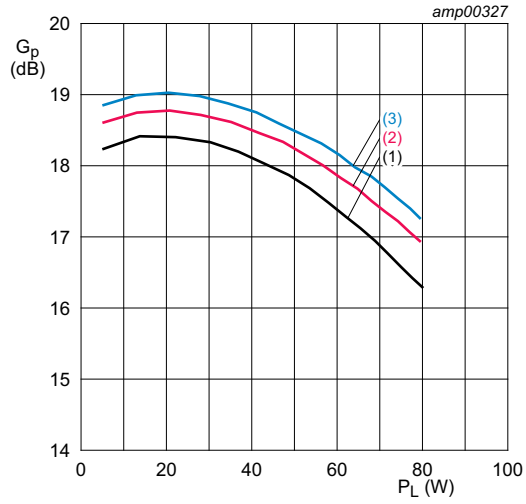
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 9. Peak-to-average power ratio as a function of output power; typical values

7.4.3 1-Carrier W-CDMA



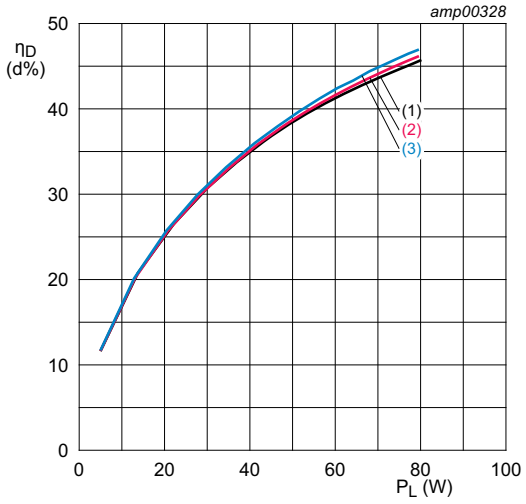
V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 10. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA.

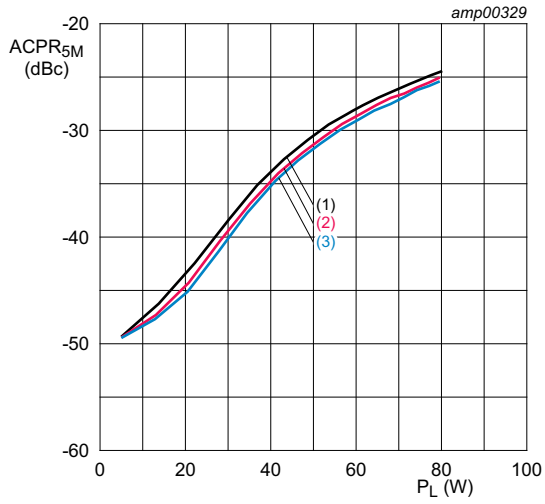
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 11. Drain efficiency as a function of output power; typical values

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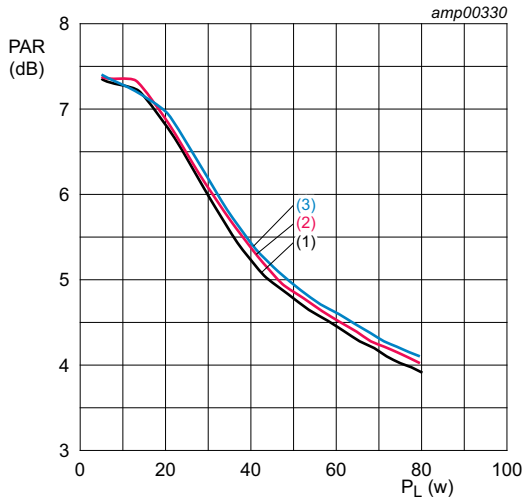
V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 12. Adjacent channel power ratio (5 M) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA.

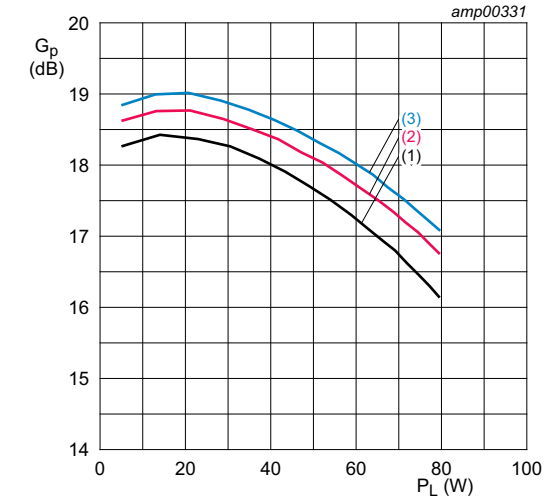
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 13. Peak-to-average power ratio as a function of output power; typical values

7.4.4 2-Carrier W-CDMA



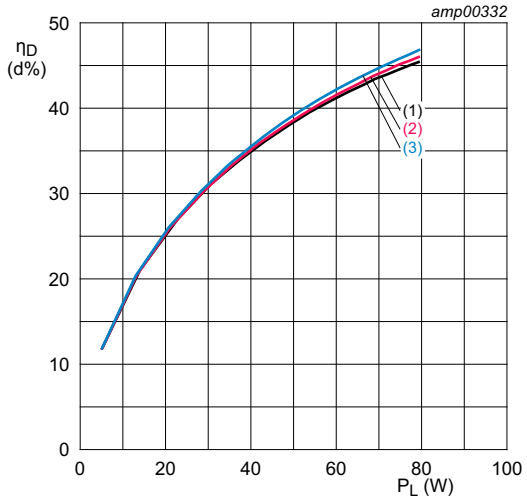
V_{DS} = 28 V; I_{Dq} = 700 mA; 5 MHz spacing.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 14. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA; 5 MHz spacing.

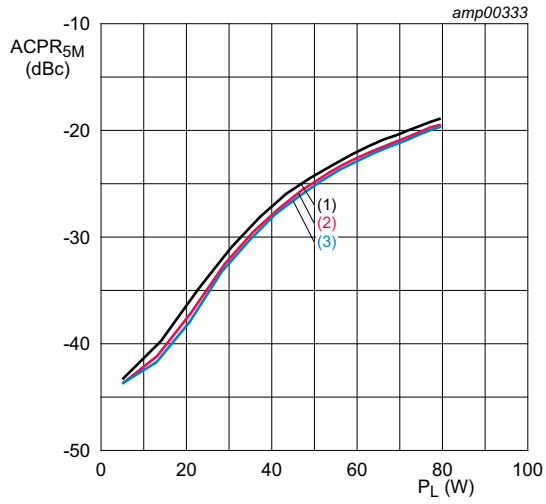
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 15. Drain efficiency as a function of output power; typical values

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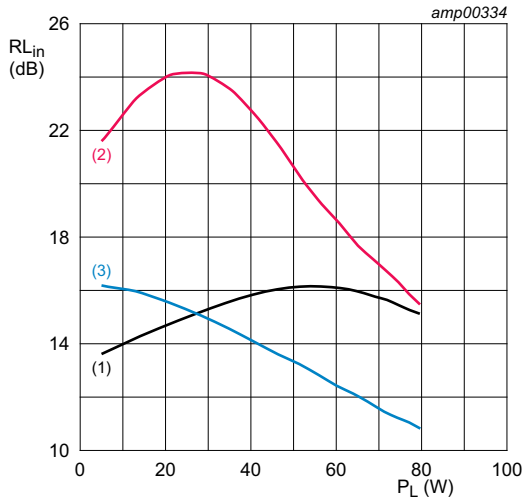
V_{DS} = 28 V; I_{Dq} = 700 mA; 5 MHz spacing.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 16. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 700 mA; 5 MHz spacing.

(1) f = 1810 MHz

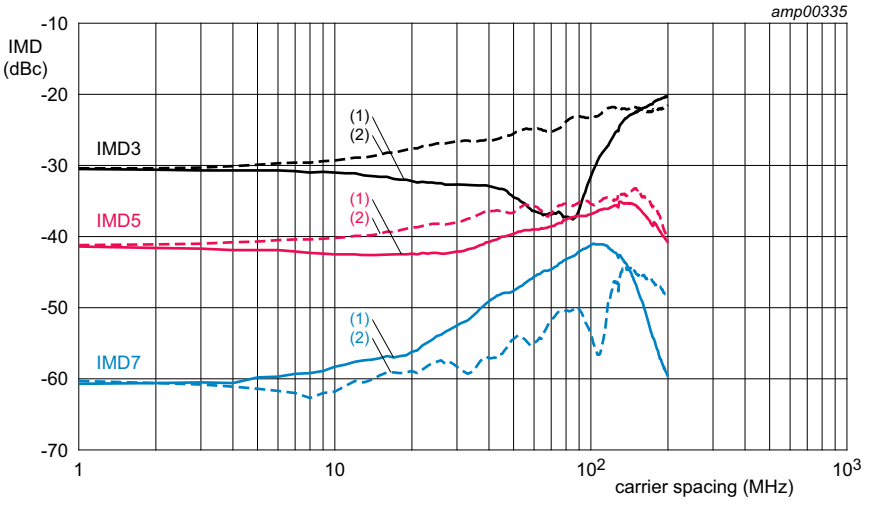
(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 17. Input return loss as a function of output power; typical values

7.4.5 2-Tone VBW

The BLC9G20LS-120VT shows 85 MHz (typical) video bandwidth (IMD third-order intermodulation inflection point) in a class-AB test circuit in the 1805 MHz to 1880 MHz band at V_{DS} = 28 V and I_{Dq} = 700 mA.



V_{DS} = 28 V; I_{Dq} = 700 mA.

(1) IMD low

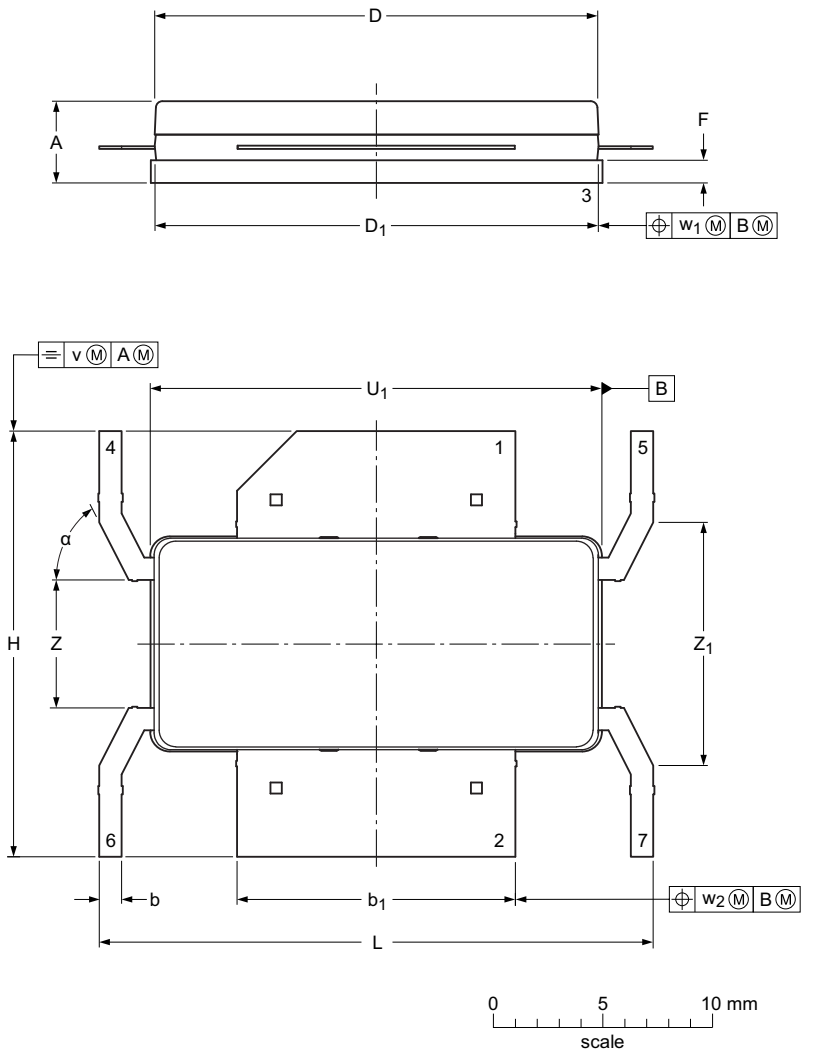
(2) IMD high

Fig 18. VBW capability in class-AB test circuit

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8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1271-2**



Z_1	α
11.19	65°
10.99	61°

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	F	H	L	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y	Z
mm	max	4.01	1.14	12.80	0.18	20.42	20.37	9.80	9.75	1.14	19.53	25.40	1.68	20.70	9.91	0.50	0.50	0.50	0.10	5.94
	nom																			
	min	3.40	0.89	12.60	0.13	20.12	20.17	9.50	9.55	0.94	19.33	25.20	1.45	20.50	9.70					5.74

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1271-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1271-2						17-04-13

Fig 19. Package outline SOT1271-2

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20LS-120VT v.2	20180705	Product data sheet	-	LC9G20LS-120VT v.1
Modifications	• Table 2 on page 2: table corrected			
BLC9G20LS-120VT v.1	20170523	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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