BLF0910H9LS600

Power LDMOS transistor

Rev. 2 — 22 June 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 600 W LDMOS power transistor for industrial applications at frequency of 915 MHz.

The BLF0910H9LS600 is designed for high-power CW applications and is assembled in a high performance ceramic package.

Table 1. Typical performance

RF performance at V_{DS} = 50 V; I_{Dq} = 90 mA in a class-AB application circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	915	50	600	19.8	68.5

1.2 Features and benefits

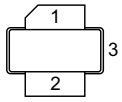
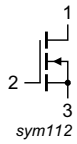
- High efficiency
- Easy power control
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (900 MHz to 930 MHz)
- Internally input matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial applications in the 915 MHz ISM band

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF0910H9LS600	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	106	V
V_{GS}	gate-source voltage	–6	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 600 W	0.174	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4 mA	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 400 mA	1.5	1.9	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	70	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 20 A	-	30.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 14 A	-	0.0575	-	Ω

Table 7. RF characteristics

Test signal: CW; f = 915 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 90 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 600 W	17.7	18.6	-	dB
RL_{in}	input return loss	P_L = 600 W	-	–17.7	–9.0	dB
η_D	drain efficiency	P_L = 600 W	62.0	65.7	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF0910H9LS600 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 90 mA; P_L = 600 W (CW); tested in band with soft power ramp up across predefined integer phase steps.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull Z_S and Z_L device impedances; I_{Dq} = 90 mA; V_{DS} = 50 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
915	1.5 – 1.6j	0.45 + 0.2j

[1] Z_S and Z_L defined in Figure 1.

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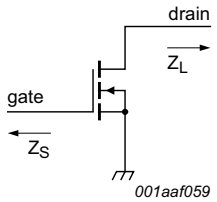
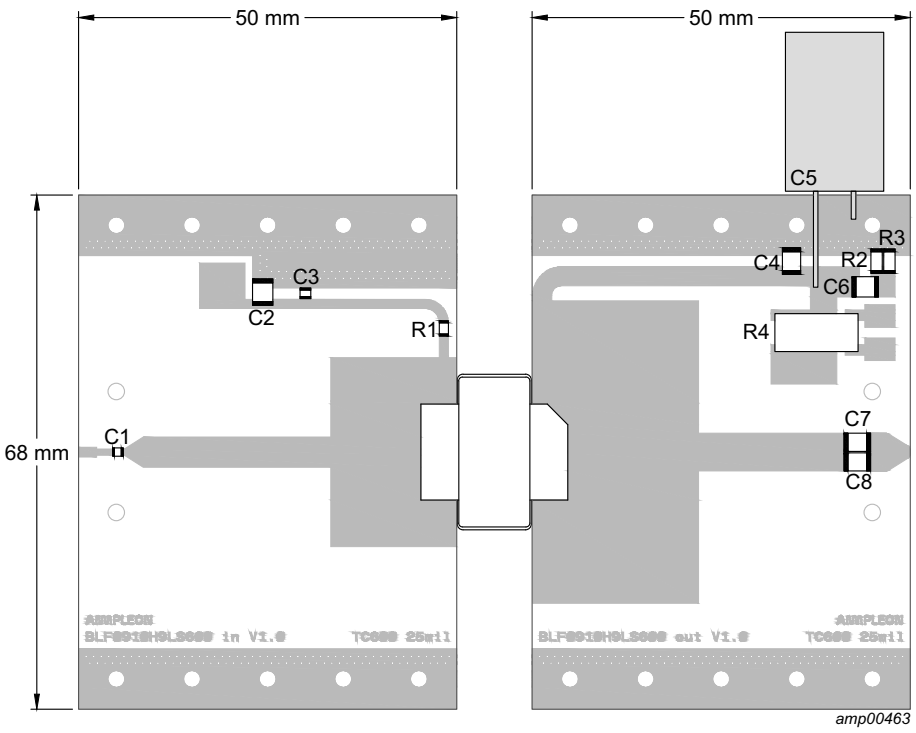


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers TC600; thickness = 0.635 mm; ε_r = 6.15.

See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 2.

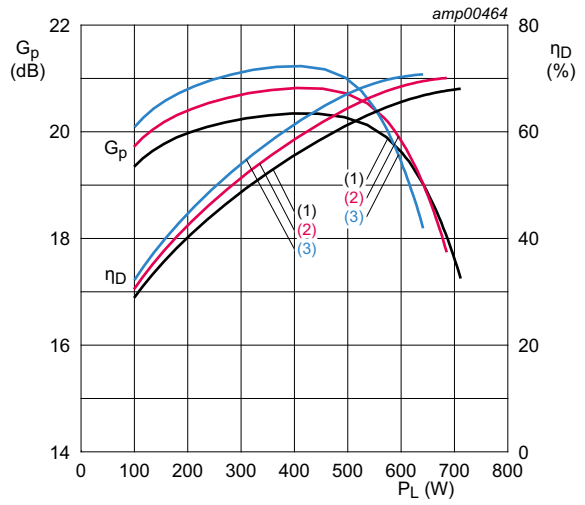
Component	Description	Value	Remarks
C1, C3	multilayer ceramic chip capacitor	100 pF	ATC100A101JW150XT
C2, C6	multilayer ceramic chip capacitor	4.7 μF, 100 V	C3225X7S2A475K200AE
C4, C7, C8	multilayer ceramic chip capacitor	51 pF	ATC100B510FW500XT
C5	electrolytic capacitor	470 μF, 63 V	MAL203858471E3

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Table 9. List of components *...continued*
For test circuit see Figure 2.

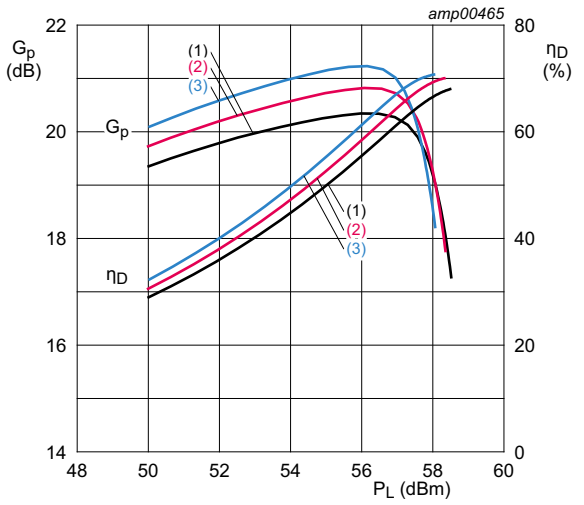
Component	Description	Value	Remarks
R1	chip resistor	10 Ω	MCMR06X10R0FTL
R2, R3	chip resistor	6.2 Ω	MC0125W120616R20
R4	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER

7.4 Graphical data



V_{DS} = 50 V; I_{Dq} = 90 mA.
(1) f = 902 MHz
(2) f = 915 MHz
(3) f = 928 MHz

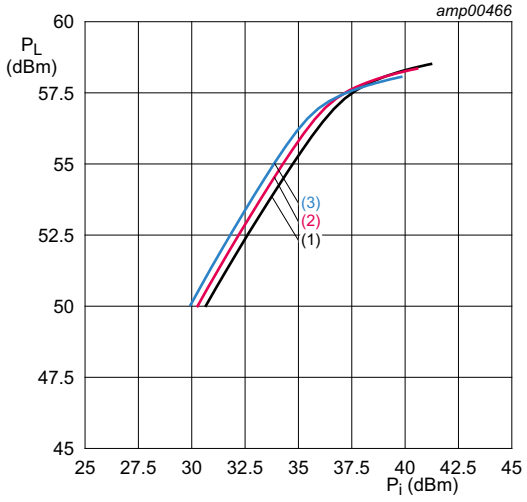
Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 90 mA.
(1) f = 902 MHz
(2) f = 915 MHz
(3) f = 928 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values

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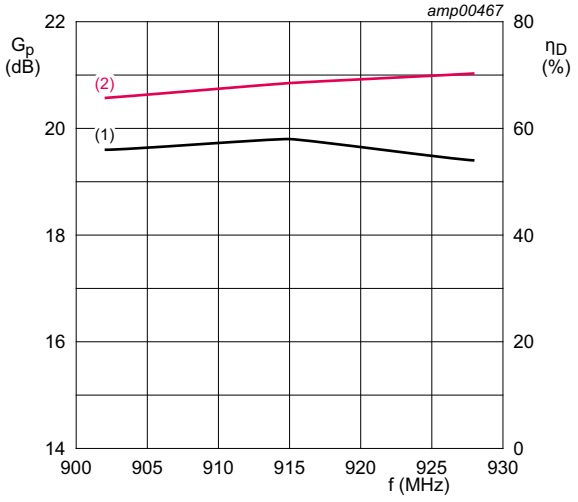
V_{DS} = 50 V; I_{Dq} = 90 mA.

(1) f = 902 MHz

(2) f = 915 MHz

(3) f = 928 MHz

Fig 5. Output power as a function of input power; typical values



V_{DS} = 50 V; I_{Dq} = 90 mA; P_L = 600 W.

(1) G_p

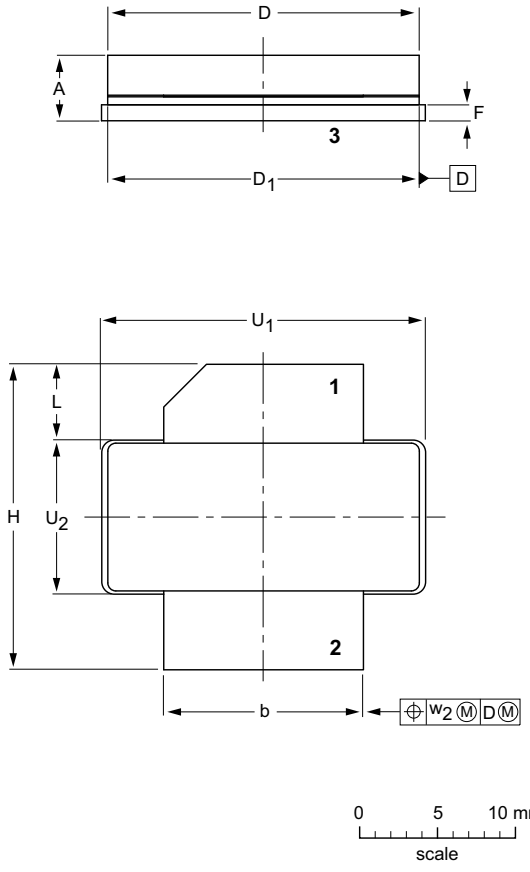
(2) η_D

Fig 6. Power gain and drain efficiency as a function of frequency; typical values

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8. Package outline

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 7. Package outline SOT502B

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF0910H9LS600 v.2	20180622	Product data sheet	-	BLF0910H9LS600 v.1
Modifications:	• Table 4 on page 2: value ‘drain-source voltage’ updated • Table 6 on page 3: value ‘drain-source breakdown voltage’ updated			
BLF0910H9LS600 v.1	20180108	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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