BLF13H9L750P; BLF13H9LS750P

Power LDMOS transistor

Rev. 1 — 20 September 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

750 W LDMOS power transistor in SOT539 push pull package for accelerator applications at a frequency of 1.3 GHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 µs; δ = 10 %; I_{Dq} = 200 mA; in a class-AB demo circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(GHz)	(V)	(W)	(dB)	(%)
pulsed RF	1.3	50	750	19	62
CW	1.3	50	700	17	62.5

1.2 Features and benefits

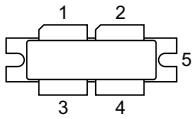
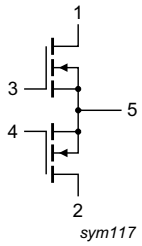
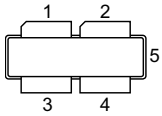
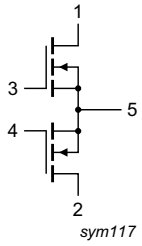
- High efficiency
- Excellent ruggedness
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Accelerator applications at the frequency of 1.3 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF13H9L750P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF13H9LS750P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF13H9L750P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF13H9LS750P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	108	V
V_{GS}	gate-source voltage	–8	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal impedance from junction to case	T_{case} = 85 °C; P_L = 650 W	0.15	K/W
$Z_{th(j\text{-}case)}$	transient impedance from junction to case	T_{case} = 85 °C; P_L = 750 W		
		t_p = 100 μs; δ = 10 %	0.045	K/W
		t_p = 200 μs; δ = 10 %	0.048	K/W
		t_p = 300 μs; δ = 10 %	0.049	K/W
		t_p = 100 μs; δ = 20 %	0.056	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	41	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	-	90	-	mΩ

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 750 W	16.6	19	-	dB
η_D	drain efficiency	P_L = 750 W	55	62	-	%
RL_{in}	input return loss	P_L = 750 W	-	−10	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 750 W	-	0.0	0.3	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		650	700	-	W
$P_{L(2dB)}$	output power at 2 dB gain compression		-	800	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLF13H9L750P and BLF13H9LS750P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 200 mA; P_L = 750 W; t_p = 300 μs; δ = 10 %.

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7.2 Impedance information

Table 8. Typical impedance (one section)

f	Z_S [1]	Z_L [1]
(GHz)	(Ω)	(Ω)
1.3	3.1 – j5.5	0.95 – j0.5

[1] Z_S and Z_L defined in Figure 1.

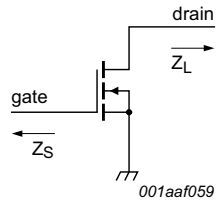
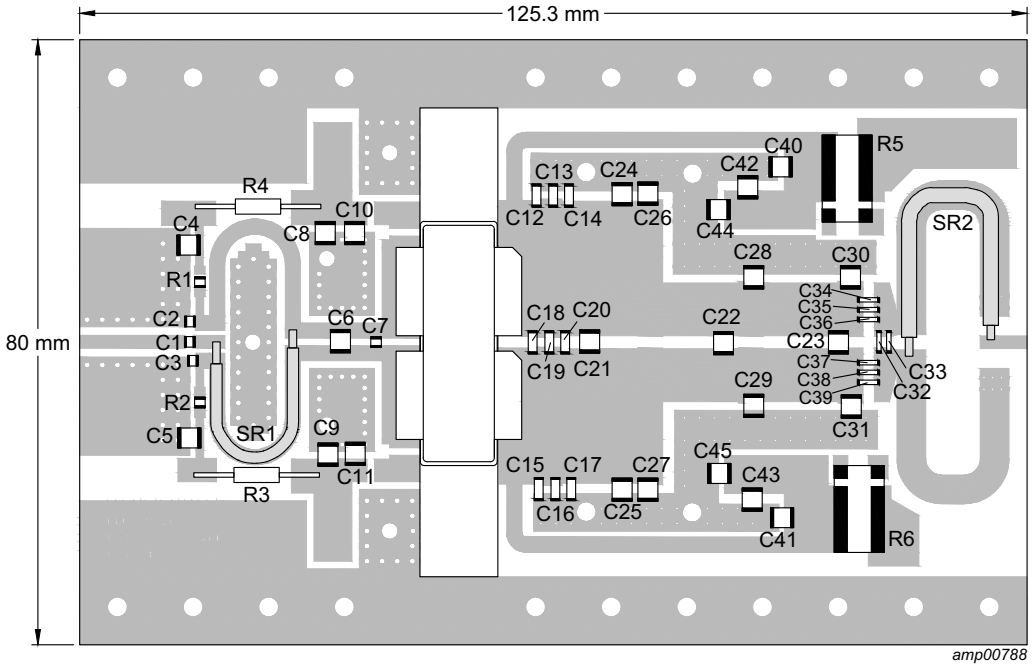


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.48; thickness = 0.762 mm; thickness copper plating = 35 μm.
See Table 9 for a list of components.

Fig 2. Component layout for application circuit

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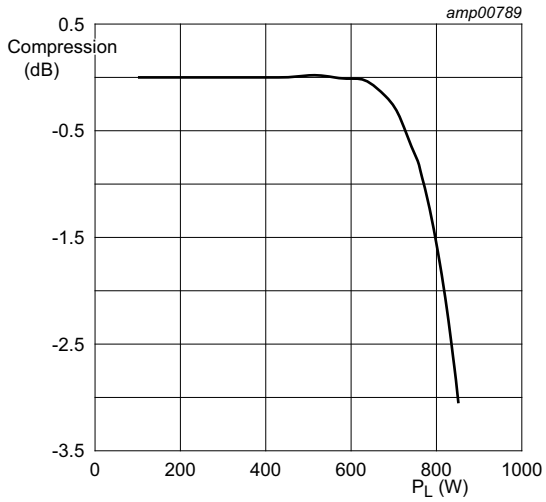
Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C34, C35, C36	multilayer ceramic chip capacitor	62 pF	ATC 800B
C2, C3	multilayer ceramic chip capacitor	43 pF	ATC 800B
C4, C5	multilayer ceramic chip capacitor	4.7 μF	TDK: C4532X7R1E475MT020U
C6	multilayer ceramic chip capacitor	4.3 pF	ATC 800B
C7	multilayer ceramic chip capacitor	3.6 pF	ATC 800B
C8, C9, C42, C43	multilayer ceramic chip capacitor	1.0 nF	ATC 100B
C10, C11, C44, C45	multilayer ceramic chip capacitor	10 μF	Murata: GRM55DR61H106KA88L
C12, C13, C15, C16, C23	multilayer ceramic chip capacitor	2.0 pF	ATC 800B
C14, C17, C26, C27	multilayer ceramic chip capacitor	0.5 pF	ATC 800B
C18, C19	multilayer ceramic chip capacitor	2.2 pF	ATC 800B
C20	multilayer ceramic chip capacitor	1.9 pF	ATC 800B
C21, C22, C28, C29	multilayer ceramic chip capacitor	1.0 pF	ATC 100B
C24, C25	multilayer ceramic chip capacitor	0.3 pF	ATC 100B
C30, C31	multilayer ceramic chip capacitor	2.4 pF	ATC 800B
C32	multilayer ceramic chip capacitor	0.7 pF	ATC 800B
C33	multilayer ceramic chip capacitor	1.3 pF	ATC 800B
C37, C38, C39, C40, C41	multilayer ceramic chip capacitor	62 pF	ATC 800B
SR1	coax	25 Ω, 34 mm	
SR2	coax	35 Ω, 34 mm	UT-141C-35-TP
R1, R2	resistor	5.1 Ω	SMD 0603
R3, R4	resistor	100 Ω, 0.6 W	
R5, R6	resistor	10 mΩ	FC4L110R010FER

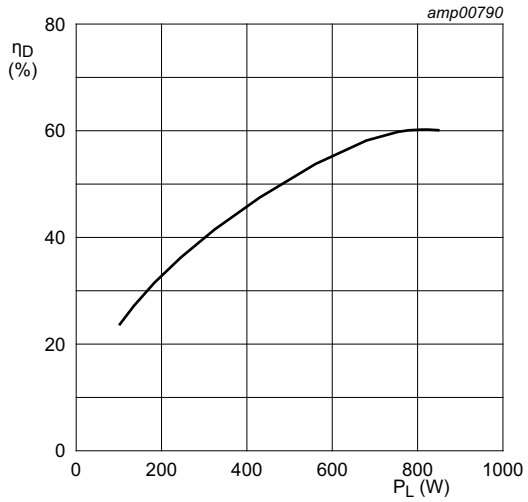
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7.4 Graphical data



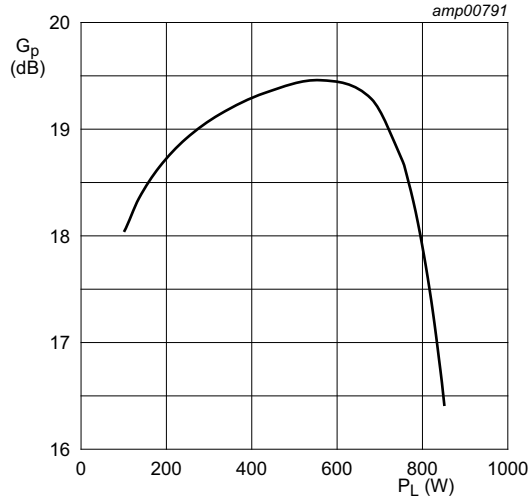
V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %.

Fig 3. Compression as a function of output power; typical values



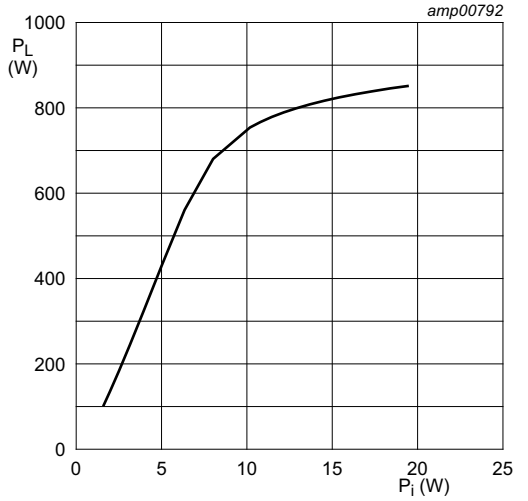
V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %.

Fig 4. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %.

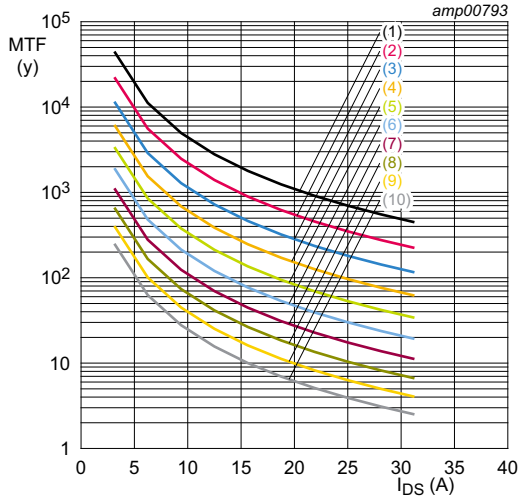
Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %.

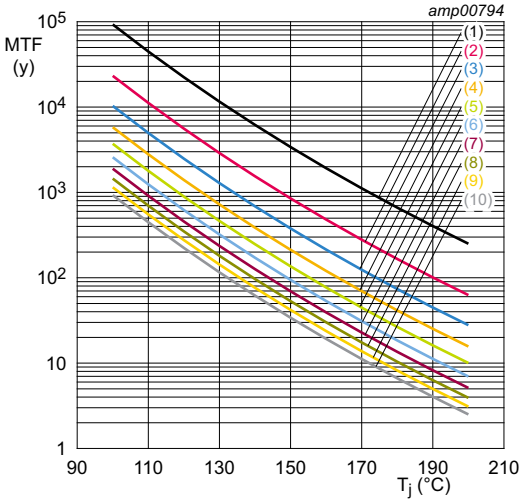
Fig 6. Output power as a function of input power; typical values

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(1) T_j = 110 °C
(2) T_j = 120 °C
(3) T_j = 130 °C
(4) T_j = 140 °C
(5) T_j = 150 °C
(6) T_j = 160 °C
(7) T_j = 170 °C
(8) T_j = 180 °C
(9) T_j = 190 °C
(10) T_j = 200 °C

Fig 7. MTF as a function of drain-source current; typical values



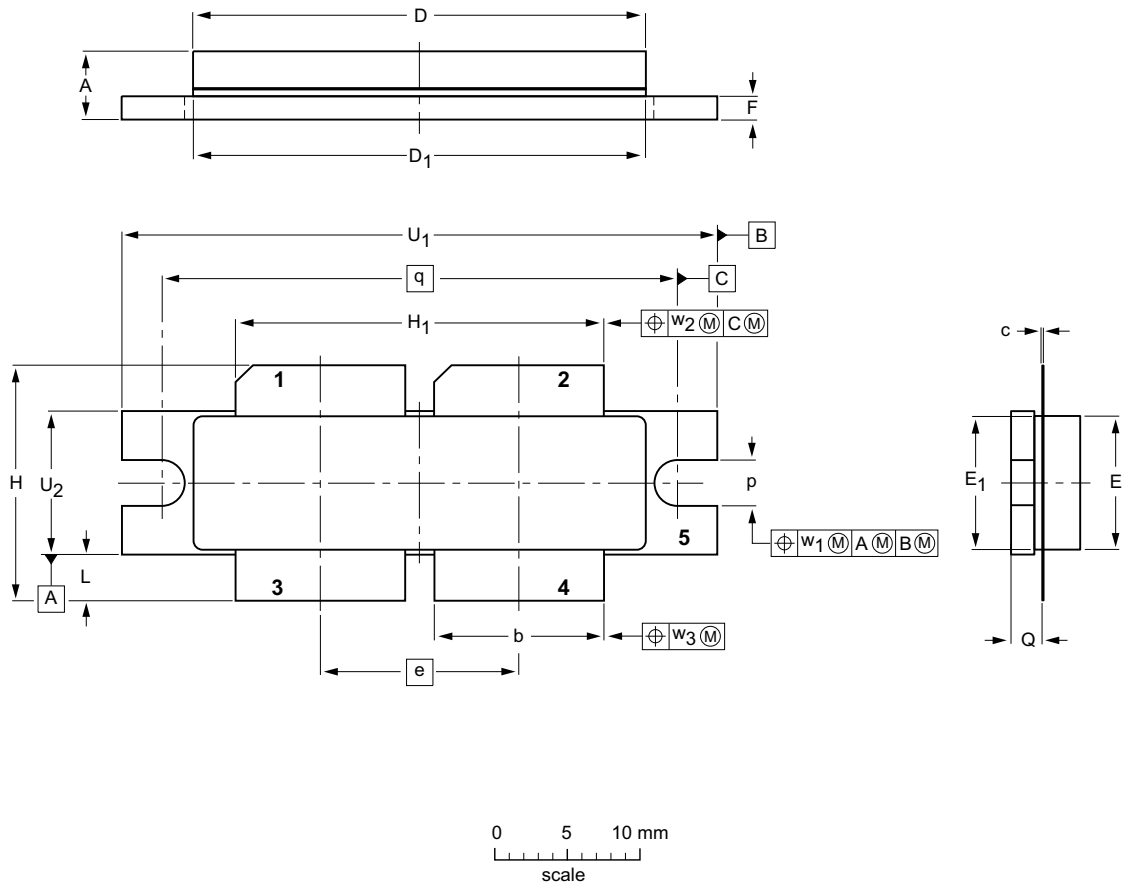
(1) I_{DS} = 3.13 A
(2) I_{DS} = 6.25 A
(3) I_{DS} = 9.38 A
(4) I_{DS} = 12.50 A
(5) I_{DS} = 15.63 A
(6) I_{DS} = 18.75 A
(7) I_{DS} = 21.88 A
(8) I_{DS} = 25.00 A
(9) I_{DS} = 28.13 A
(10) I_{DS} = 31.25 A

Fig 8. MTF as a function of junction temperature; typical values

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8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

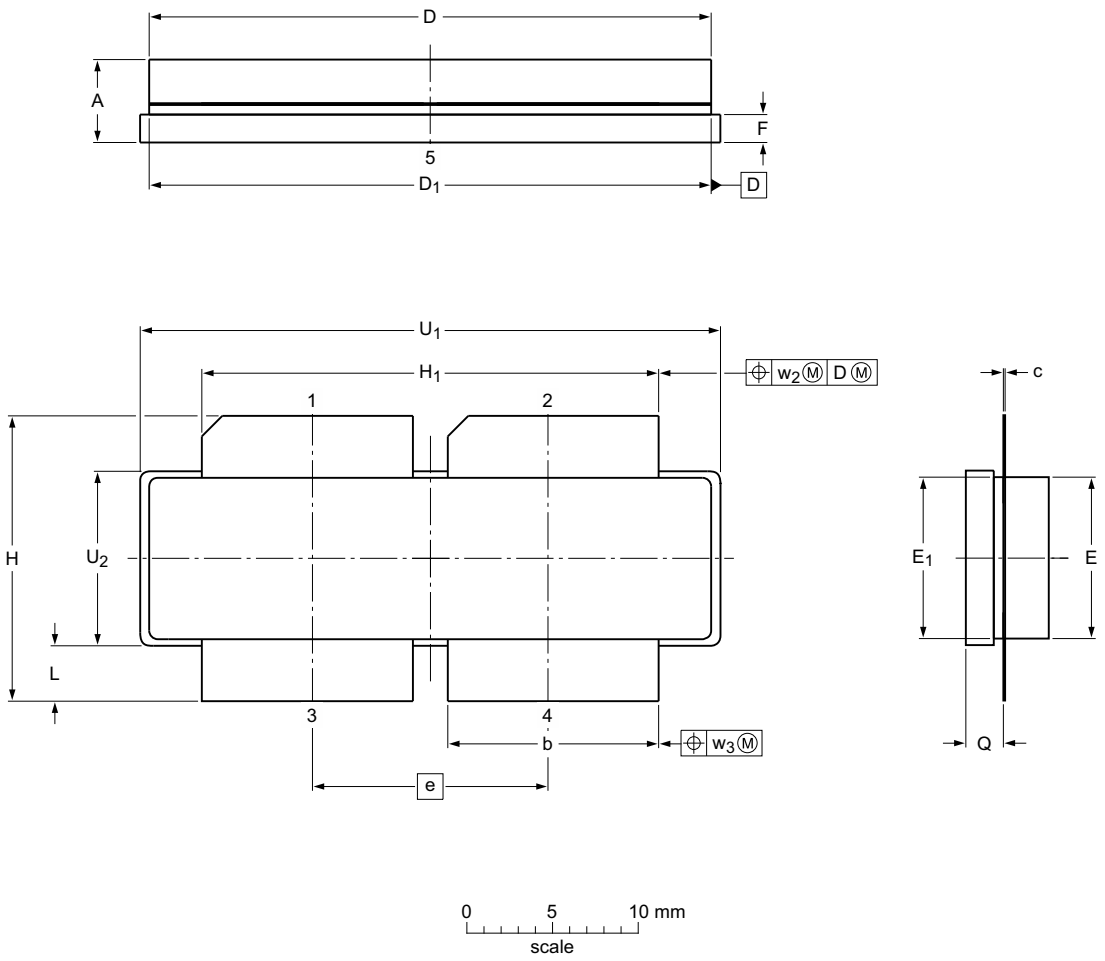
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 9. Package outline SOT539A

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Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 10. Package outline SOT539B

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF13H9L750P_13H9LS750P v.1	20180920	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

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14. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
2 Pinning information 2
3 Ordering information 2
4 Limiting values 2
5 Thermal characteristics 3
6 Characteristics 3
7 Test information 3
7.1 Ruggedness in class-AB operation 3
7.2 Impedance information 4
7.3 Test circuit 4
7.4 Graphical data 6
8 Package outline 8
9 Handling information 10
10 Abbreviations 10
11 Revision history 10
12 Legal information 11
12.1 Data sheet status 11
12.2 Definitions 11
12.3 Disclaimers 11
12.4 Trademarks 12
13 Contact information 12
14 Contents 13

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Date of release: 20 September 2018
Document identifier: BLF13H9L750P_13H9LS750P

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