BLF944P

Power LDMOS transistor

Rev. 1 — 7 September 2023

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 135 W LDMOS transistor for non cellular communication and industrial applications. The excellent ruggedness of this device makes it ideal for mobile NCC and ISM applications in the frequency range from HF to 1300 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	860	32	135	20.3	67

1.2 Features and benefits

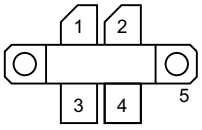
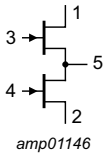
- Designed for broadband operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Non cellular communication applications
- Industrial, scientific and medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1228A	BLF944PU	9349 606 51112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	106	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; V_{DS} = 32 V; P_L = 135 W	0.45	K/W

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6. Characteristics

Table 6. DC characteristics

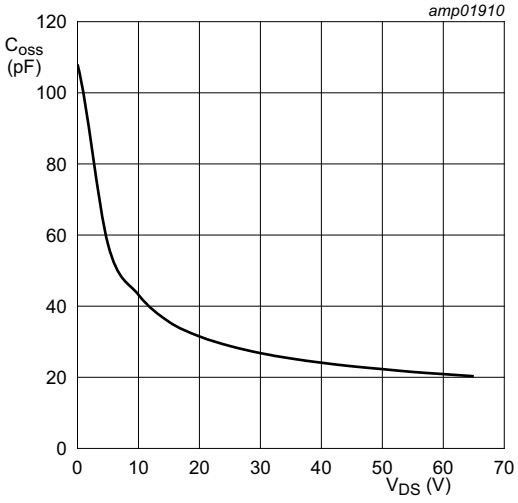
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.67 mA	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 67mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 120 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	11.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.35 A	-	0.30	-	Ω

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	0.42	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	74	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	26	-	pF



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

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Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 860 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 240 mA; T_{case} = 25 °C; unless otherwise specified in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 135 W	19.3	20.3	-	dB
RL_{in}	input return loss	P_L = 135 W	-	–9	–6	dB
η_D	drain efficiency	P_L = 135 W	63	67	-	%

7. Test information

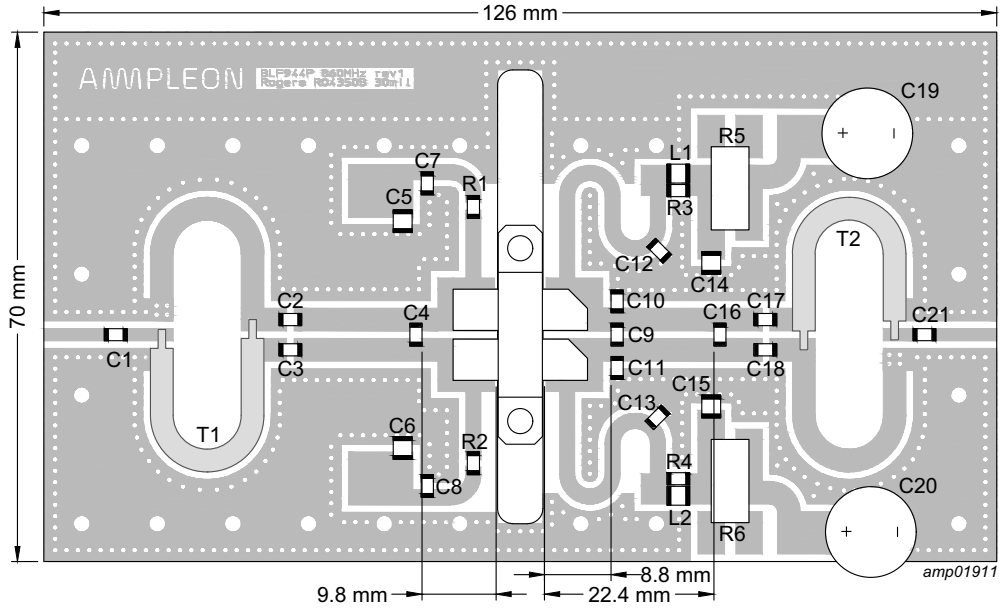
7.1 Ruggedness in class-AB operation

The BLF944P is capable of withstanding a load mismatch corresponding to VSWR = 40 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 240 mA; P_L = 135 W; f = 860 MHz; pulsed CW (t_p = 100 μs; δ = 20 %).

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7.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.762 mm.

See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	20 pF [1][2]	
C2, C3	multilayer ceramic chip capacitor	6.8 pF [1][2]	
C4	multilayer ceramic chip capacitor	16 pF [1][2]	
C5, C6	multilayer ceramic chip capacitor	4.7 μF, 50 V	
C7, C8, C12, C13	multilayer ceramic chip capacitor	100 pF [1][2]	
C9	multilayer ceramic chip capacitor	13 pF [1][2]	
C10, C11	multilayer ceramic chip capacitor	3.6 pF [1][2]	
C14, C15	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C16	multilayer ceramic chip capacitor	4.3 pF [1][2]	
C17, C18	multilayer ceramic chip capacitor	9.1 pF [1][2]	
C19, C20	electrolytic capacitor	470 μF, 63 V	
C21	multilayer ceramic chip capacitor	56 pF [1][2]	
L1, L2	air core inductor	13 nH	Coilcraft: 1508-13N
R1, R2	chip resistor	560 Ω	SMD 1206
R3, R4	chip resistor	6.8 Ω	SMD 1206
R5, R6	chip resistor	0.01 Ω	FC4L110R010FER
T1, T2	semi rigid coax	50 Ω, 38 mm	

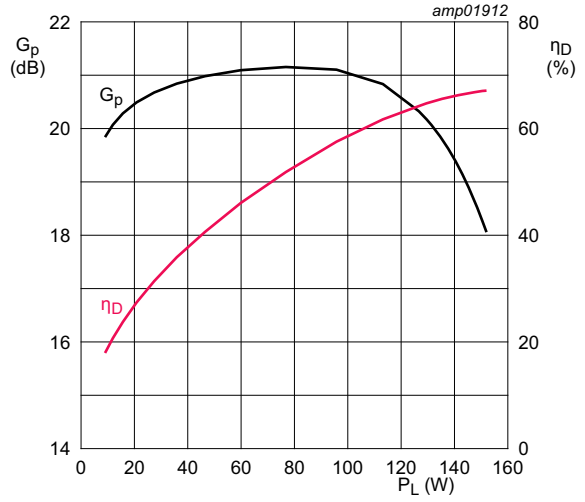
[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Vertical mounted.

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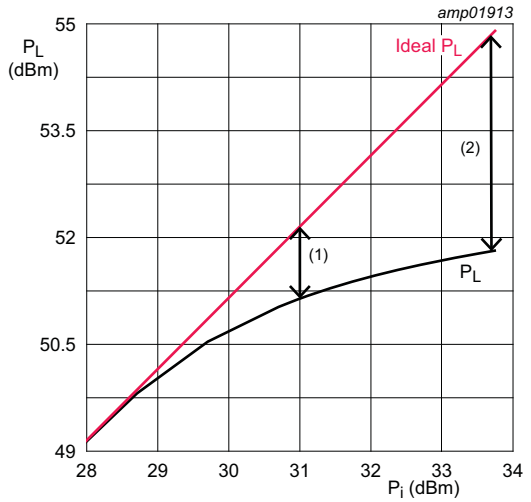
7.3 Graphical data

7.3.1 Pulsed CW performance measured in production RF test circuit



V_{DS} = 32 V; I_{Dq} = 240 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

Fig 3. Power gain and drain efficiency as function of output power; typical values



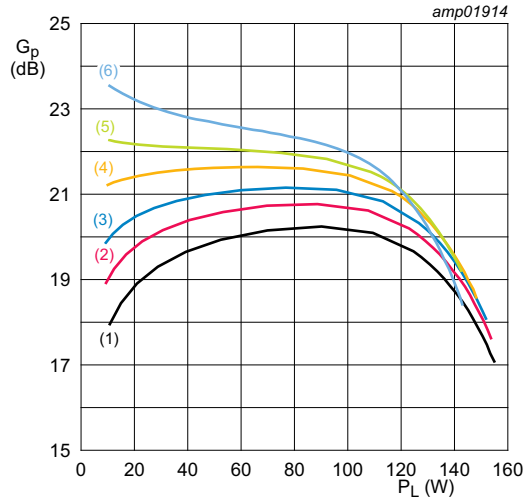
V_{DS} = 32 V; I_{Dq} = 240 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 51.1 dBm (130 W)

(2) $P_{L(3dB)}$ = 51.8 dBm (151 W)

Fig 4. Output power as a function of input power; typical values

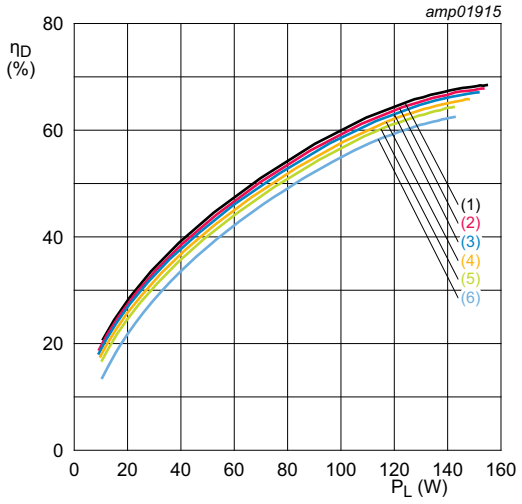
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V_{DS} = 32 V; f = 860 MHz; t_p = 100 µs; δ = 20 %.

(1) I_{Dq} = 20 mA
(2) I_{Dq} = 100 mA
(3) I_{Dq} = 240 mA
(4) I_{Dq} = 600 mA
(5) I_{Dq} = 1000 mA
(6) I_{Dq} = 2000 mA

Fig 5. Power gain as a function of output power; typical values

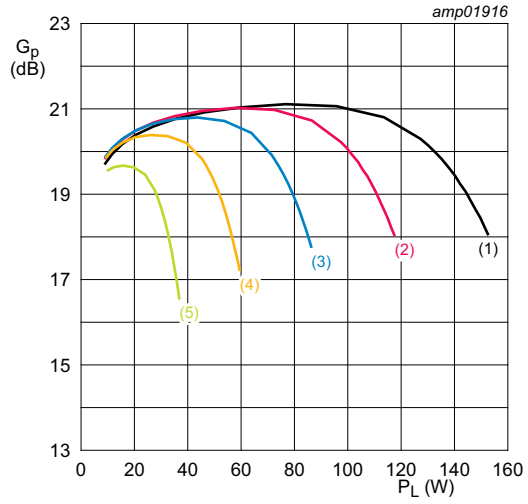


V_{DS} = 32 V; f = 860 MHz; t_p = 100 µs; δ = 20 %.

(1) I_{Dq} = 20 mA
(2) I_{Dq} = 100 mA
(3) I_{Dq} = 240 mA
(4) I_{Dq} = 600 mA
(5) I_{Dq} = 1000 mA
(6) I_{Dq} = 2000 mA

Fig 6. Drain efficiency as a function of output power; typical values

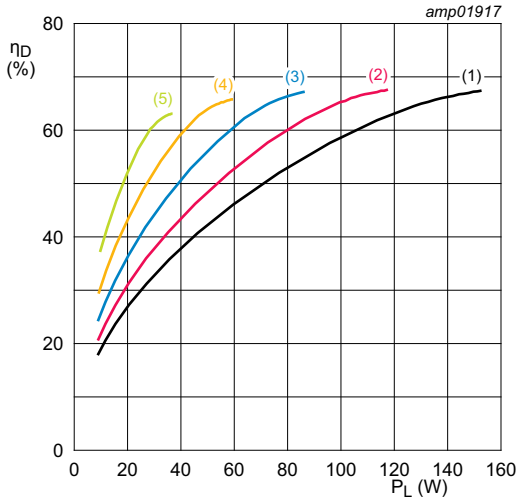
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I_{Dq} = 240 mA; f = 860 MHz; t_p = 100 µs; δ = 20 %.

(1) V_{DS} = 32 V
(2) V_{DS} = 28 V
(3) V_{DS} = 24 V
(4) V_{DS} = 20 V
(5) V_{DS} = 16 V

Fig 7. Power gain as a function of output power; typical values

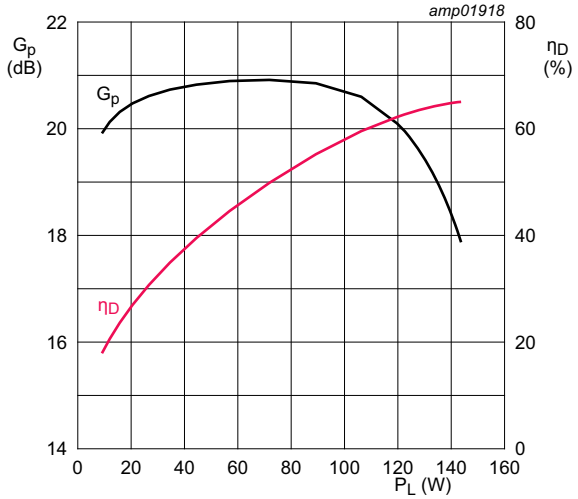


I_{Dq} = 240 mA; f = 860 MHz; t_p = 100 µs; δ = 20 %.

(1) V_{DS} = 32 V
(2) V_{DS} = 28 V
(3) V_{DS} = 24 V
(4) V_{DS} = 20 V
(5) V_{DS} = 16 V

Fig 8. Drain efficiency as a function of output power; typical values

7.3.2 CW performance measured in production RF test circuit



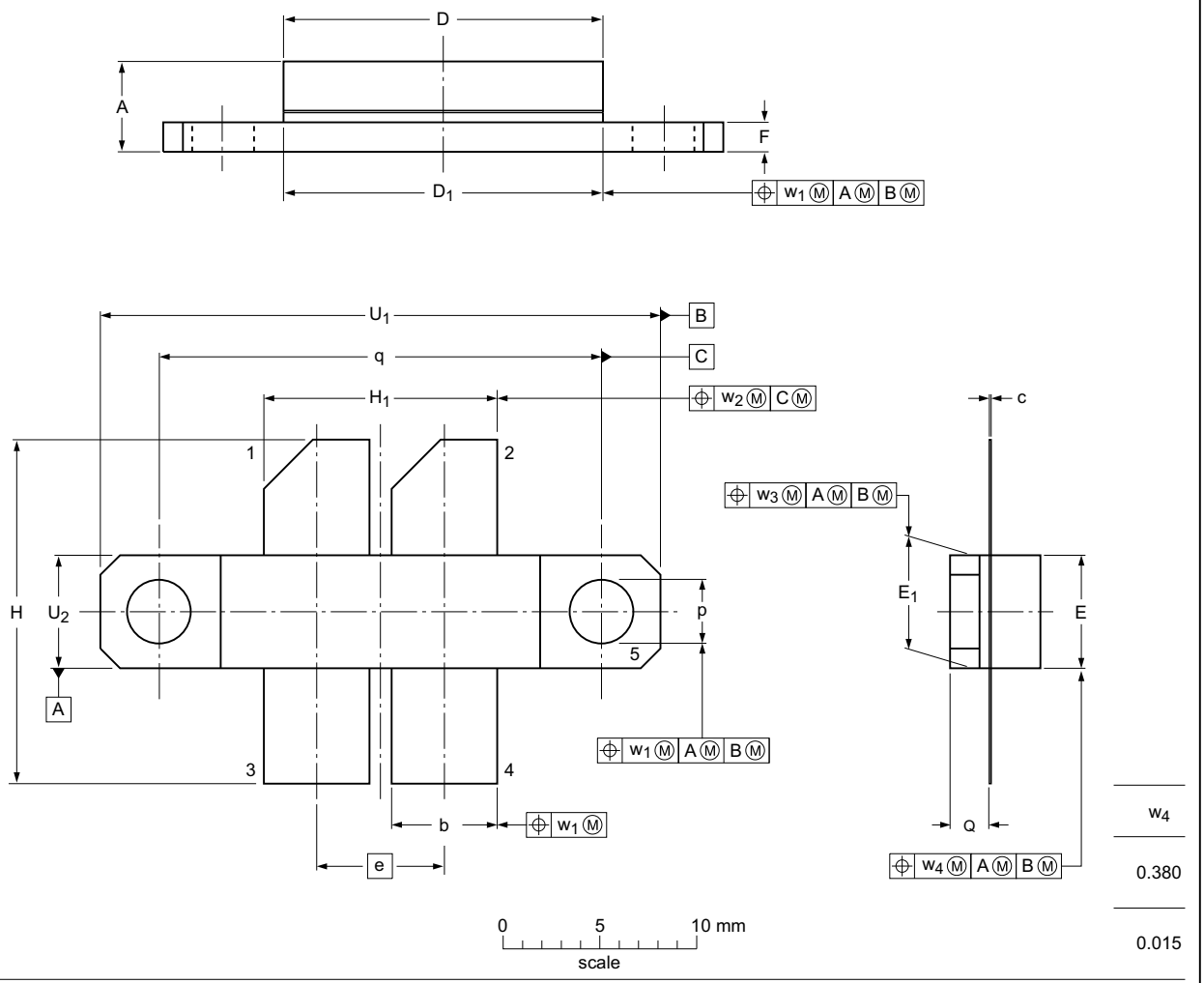
V_{DS} = 32 V; I_{Dq} = 240 mA; f = 860 MHz.

Fig 9. Power gain and drain efficiency as function of output power; typical values

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8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1228A**



	w4
	0.380
	0.015

Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q(2)	q	U_1	U_2	w_1	w_2	w_3
mm	max	5.2	5.59	0.15	16.66	16.69		5.92	5.97	1.65	18.29	12.19	3.43	2.21		29.08	5.97			
	nom						6.60								22.86			0.25	0.51	0.125
	min	4.5	5.33	0.08	16.36	16.33		5.77	5.72	1.40	17.27	11.94	3.18	1.96		28.83	5.72			
inches	max	0.205	0.220	0.006	0.656	0.657		0.233	0.235	0.065	0.720	0.480	0.135	0.087		1.145	0.235			
	nom						0.26								0.900			0.01	0.02	0.005
	min	0.177	0.210	0.003	0.644	0.643		0.227	0.225	0.055	0.680	0.470	0.125	0.077		1.135	0.225			

Note
1. Millimeter dimensions are derived from the original inch dimensions.
2. Dimension is measured 0.030 inch (0.76 mm) from body.

sot1228a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1228A						~~12-06-11~~ 13-05-16

Fig 10. Package outline SOT1228A

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
GaN	Gallium Nitride
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
MTF	Median Time to Failure
NCC	Non-Cellular Communication
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF944P v.1	20230907	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 7 September 2023
Document identifier: BLF944P

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