BLF989E; BLF989ES

UHF power LDMOS transistor

AMPLEON

Rev. 3 — 17 February 2022 Product data sheet

1. Product profile

1.1 General description

A 1000 W LDMOS RF power transistor for asymmetrical broadcast Doherty transmitter applications which operates at 180 W DVB-T average power. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications in the frequency range from 400 MHz to 860 MHz.

Table 1. Application information

RF performance at V_{DS} = 50 V in an asymmetrical Doherty application.

Test signal	f	$P_{L(AV)}$	G_p	η_D	IMD_{shldr}	PAR
	(MHz)	(W)	(dB)	(%)	(dBc)	(dB)
DVB-T (8k OFDM) [1]	470 to 620	180	17	50	–38	8
	470 to 700	180	15	48	–37.5	7.5

[1] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

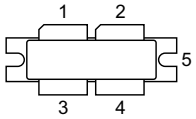
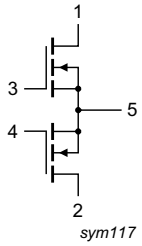
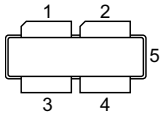
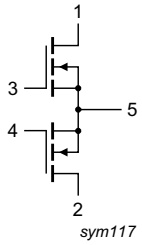
- Designed for asymmetric Doherty operation
- Very high efficiency enabling air cooled high power transmitters
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Broadcast transmitter applications in the UHF band
- Digital broadcasting
- Applicable at frequencies from 400 MHz to 860 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF989E (SOT539AN)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		
BLF989ES (SOT539BN)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT539AN	BLF989EU	9349 602 21112	Tray, 20-fold; non-dry pack	60
SOT539BN	BLF989ESU	9349 602 22112	Tray, 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS(amp)main}$	main amplifier drain-source voltage		-	108	V
$V_{DS(amp)peak}$	peak amplifier drain-source voltage		-	108	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; V_{DS} = 50 V; I_{DS} = 3.5 A (main); I_{DS} = 0 A (peak) [1]	0.28	K/W
		T_{case} = 90 °C; V_{DS} = 50 V; P_L = 180 W; PAR = 8 dB [2]	0.19	K/W

[1] Measured under DC test conditions, with peak section off.

[2] Measured in an ultra-wide Doherty application, using DVB-T (8k OFDM) signal, PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	1.5	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	43	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	-	90	-	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.6 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 360 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	67	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 12.6 A	-	60	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	368	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	69	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.86	-	pF

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Table 7. AC characteristics *…continued*

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak device						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	484	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	107	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.16	-	pF

Table 8. RF characteristics

RF characteristics in Ampleon production test circuit, T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVB-T (8k OFDM), Doherty operation						
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current	peak section: V_{GS} = 1.3 V below $V_{GS(th)}$ (peak)	-	600	-	mA
$P_{L(AV)}$	average output power	f = 550 MHz	-	180	-	W
G_p	power gain	f = 550 MHz	18.6	20	-	dB
η_D	drain efficiency	f = 550 MHz	50	52	-	%
PAR	peak-to-average ratio	f = 550 MHz	6.9	7.4	-	dB

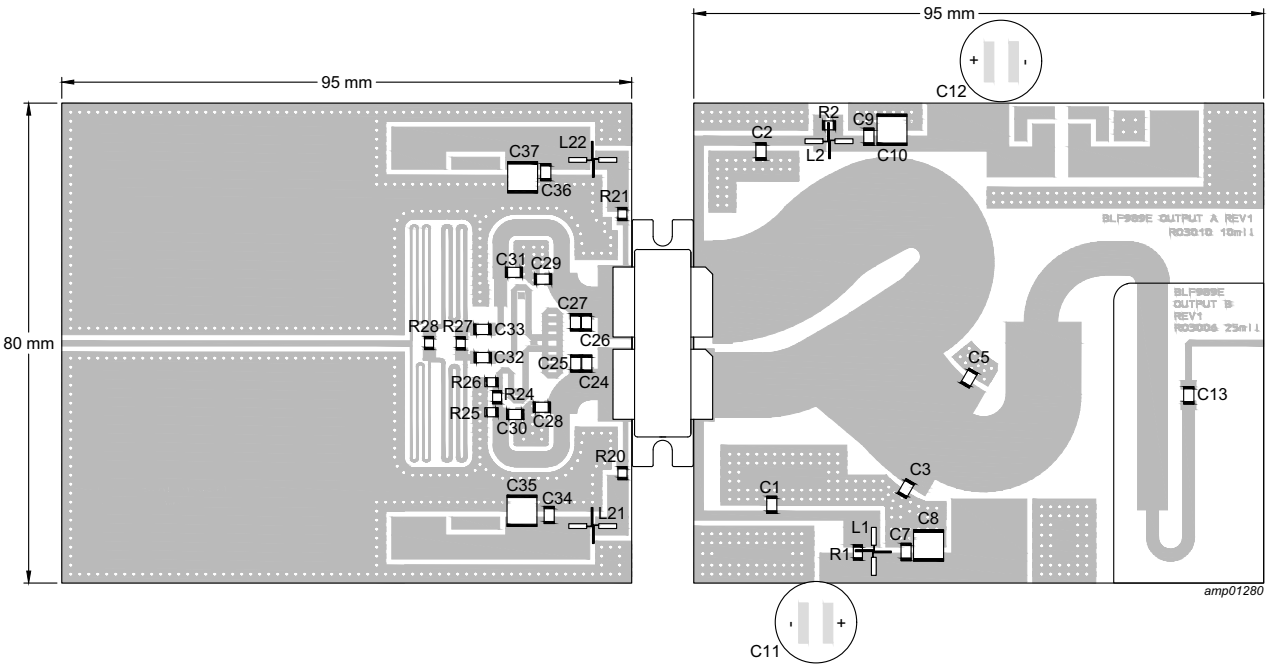
7. Test information

7.1 Ruggedness in Doherty operation

The BLF989E and BLF989ES are capable of withstanding a load mismatch corresponding to VSWR ≥ 40 : 1 through all phases under the following conditions: V_{DS} = 50 V; f = 550 MHz; P_L = 180 W; DVB-T.

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7.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO3006; ε_r = 6.5 F/M; height = 0.635 mm; Cu (top/bottom metallization); thickness copper plating = 29.6 μm; Rogers RO3010; ε_r = 10 F/M; height = 0.254 mm.

See Table 9 for a list of components.

Fig 1. Component layout for production RF test circuit

Table 9. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1, C2, C7, C9, C13	multilayer ceramic chip capacitor	100 pF [1]	ATC 800B
C3	multilayer ceramic chip capacitor	10 pF [1]	ATC 800B
C5	multilayer ceramic chip capacitor	8.2 pF [1]	ATC 800B
C8, C10	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK
C11, C12	electrolytic capacitor	470 μF, 63 V	
L1, L2	one turn inductor	D = 5 mm, d = 1mm	
R1	chip resistor	1 Ω	SMD 1206
R2	chip resistor	5.6 Ω	SMD 1206
C24, C25, C26, C27	multilayer ceramic chip capacitor	20 pF [1]	ATC 800B
C28, C29	multilayer ceramic chip capacitor	10 pF [1]	ATC 800B
C30, C31	multilayer ceramic chip capacitor	5.1 pF [1]	ATC 800B
C32, C33, C34, C36	multilayer ceramic chip capacitor	100 pF [1]	ATC 800B
C35, C37	multilayer ceramic chip capacitor	4.7 μF, 63 V	TDK
L21, L22	one turn inductor	D = 5 mm, d = 1mm	
R20, R21	chip resistor	5.6 Ω	SMD 0805
R25, R26	chip resistor	300 Ω	SMD 1206

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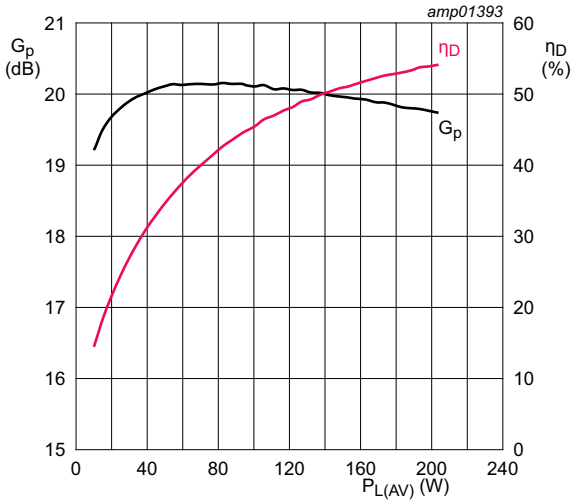
Table 9. List of components *...continued*
See Figure 1 for component layout.

Component	Description	Value	Remarks
R24	chip resistor	18 Ω	SMD 1206
R27	chip resistor	2x510 Ω	SMD 1206
R28	chip resistor	2x180 Ω	SMD 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

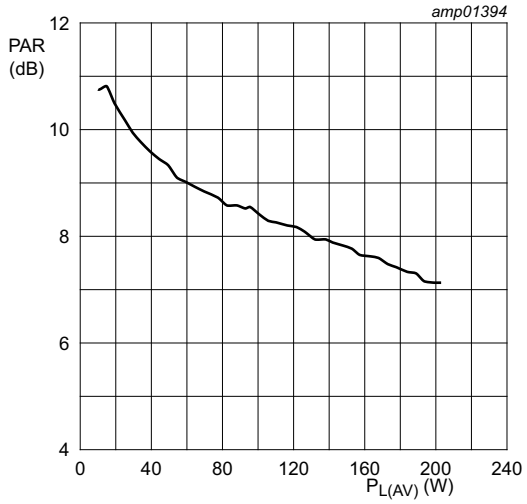
7.3 Graphs

7.3.1 DVB-T in production test circuit



V_{DS} = 50 V; I_{Dq} = 600 mA; measured in a Doherty production test circuit at 550 MHz.

Fig 2. Power gain and drain efficiency as function of average output power; typical values



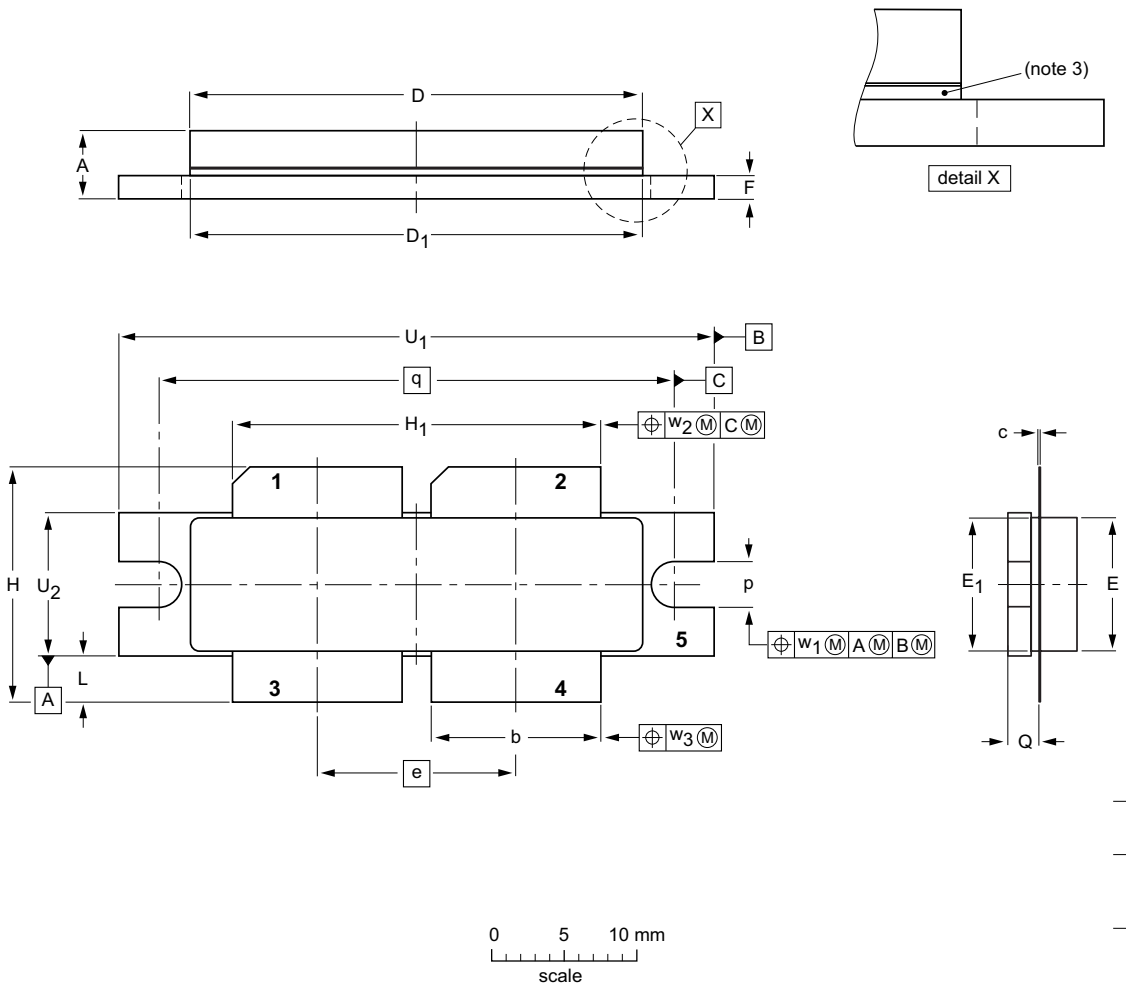
V_{DS} = 50 V; I_{Dq} = 600 mA; measured in a Doherty production test circuit at 550 MHz.

Fig 3. Peak-to-average power ratio as a function of average output power; typical values

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8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539AN**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	p	Q	q[2]	U_1	U_2	w_1	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	3.30	2.26		41.28	10.29			
	nom								13.72							35.56			0.25	0.51	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			0.01
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.130	0.089		1.625	0.405			
	nom								0.54							1.400			0.01	0.02	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.
3. ceramic window frame has a minimum thickness of 0.400 mm.

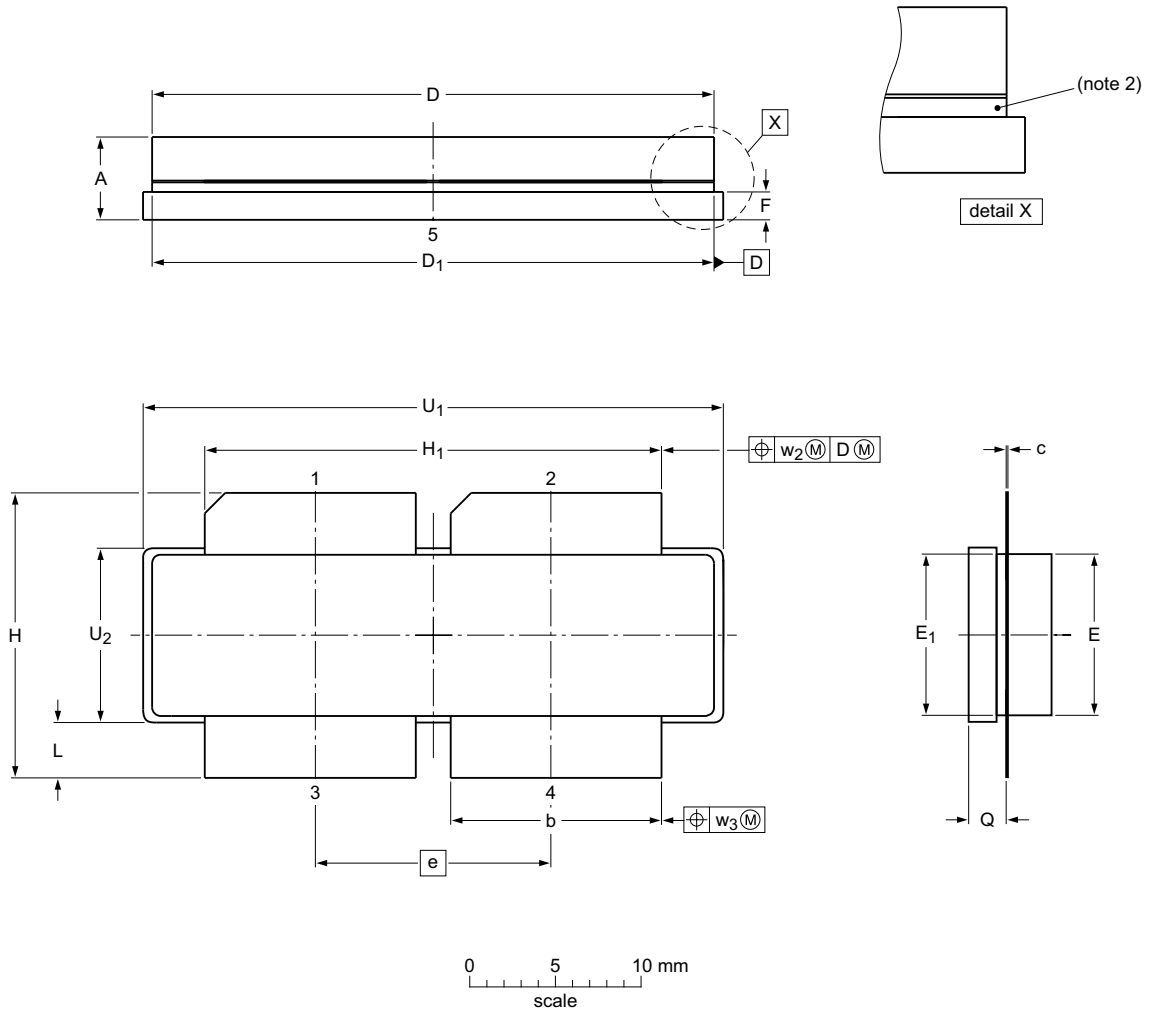
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539AN						20-04-20

Fig 4. Package outline SOT539AN

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Earless flanged balanced ceramic package; 4 leads **SOT539BN**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. ceramic window frame has a minimum thickness of 0.400 mm.

sot539bn_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539BN						20-04-20

Fig 5. Package outline SOT539BN

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF989E_BLF989ES v.3	20220217	Product data sheet	-	BLF989E_BLF989ES v.2
Modifications:	• Section 7.1 on page 4: section updated			
BLF989E_BLF989ES v.2	20210415	Product data sheet	-	BLF989E_BLF989ES v.1
BLF989E_BLF989ES v.1	20200403	Product data sheet	-	-

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12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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