BLL6H0514-25

LDMOS driver transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

25 W LDMOS transistor intended for pulsed applications in the 0.5 GHz to 1.4 GHz range.

Table 1. Application information

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 50 mA; in a class-AB application circuit.

Mode of operation	f	t_p	δ	V_{DS}	P_L	G_p	RL_{in}	η_D	$P_{droop(pulse)}$	t_r	t_f
	(MHz)	(μs)	(%)	(V)	(W)	(dB)	(dB)	(%)	(dB)	(ns)	(ns)
pulsed RF	960 to 1215	128	10	50	25	21	10	58	0.05	8	6
	1200 to 1400	300	10	50	25	19	10	50	0.05	8	6

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

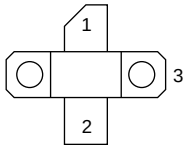
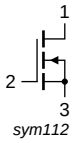
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (0.5 GHz to 1.4 GHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Amplifiers for pulsed applications in the 0.5 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H0514-25	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	2.5	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 25 W		
		t_p = 100 μs; δ = 10 %	0.86	K/W
		t_p = 200 μs; δ = 10 %	1.11	K/W
		t_p = 300 μs; δ = 10 %	1.29	K/W
		t_p = 100 μs; δ = 20 %	1.15	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 630 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 18 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	2.1	2.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	100	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 18 mA	120	150	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 63 mA	-	1500	2750	mΩ

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 128 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA; f = 1.2 GHz; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		25	-	-	W
V_{DS}	drain-source voltage	P_L = 25 W	-	-	50	V
G_p	power gain	P_L = 25 W	20	21	-	dB
RL_{in}	input return loss	P_L = 25 W	10	15	-	dB
η_D	drain efficiency	P_L = 25 W	57	59	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 25 W	-	0	0.3	dB
t_r	rise time	P_L = 25 W	-	20	50	ns
t_f	fall time	P_L = 25 W	-	6	50	ns

6.1 Ruggedness in class-AB operation

The BLL6H0514-25 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA; P_L = 25 W; f = 1.2 GHz; t_p = 128 μs; δ = 10 %.

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7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
950	2.37 + j3.3	6.11 + j11.1
1000	2.44 + j2.65	7.00 + j16.0
1050	2.34 + j2.67	7.39 + j14.2
1100	2.56 + j2.06	7.0 + j16.0
1150	2.54 + j1.70	5.77 + j13.85
1200	2.25 + j1.29	7.39 + j14.2
1300	2.21 + j0.15	6.11 + j11.1
1400	2.46 – j0.52	5.00 + j10.0

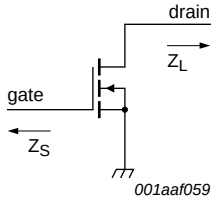


Fig 1. Definition of transistor impedance

7.2 Typical data

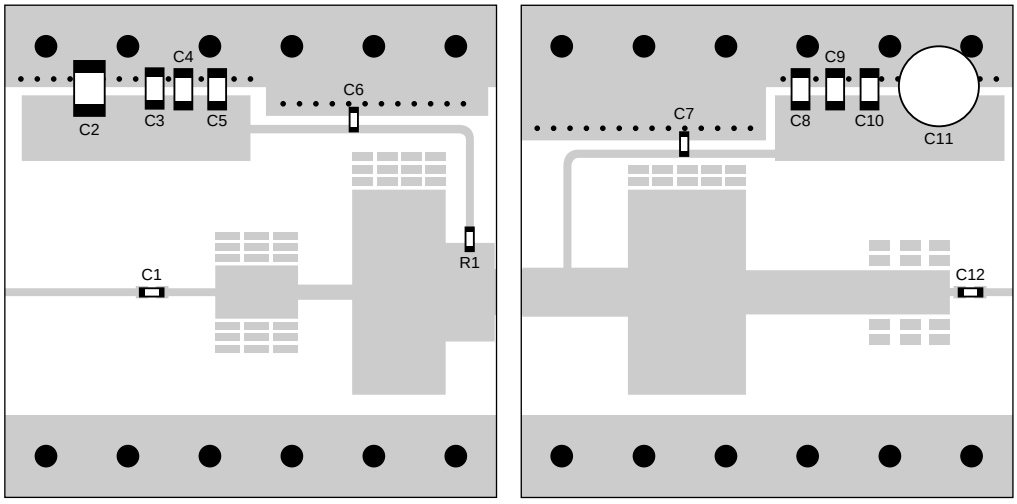
Table 9. Application information

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 50 mA; in a class-AB application circuit.

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7.3 Application circuit



Printed-Circuit Board (PCB) material: Duroid 6006 with ε_r = 6.15 and thickness = 0.64 mm.

See Table 10 for list of components.

Fig 2. Component layout

Table 10. List of components

See Figure 2 for component layout.

Component	Description	Value		Remarks
C1, C6, C7, C12	multilayer ceramic chip capacitor	56 pF	[1]	
C2	multilayer ceramic chip capacitor	10 μF; 25 V		
C3, C4, C8, C9	multilayer ceramic chip capacitor	100 pF	[1]	
C5, C10	multilayer ceramic chip capacitor	1 nF	[2]	
C11	electrolytic capacitor	68 μF; 63 V		
R1	SMD resistor	10 Ω		SMD 0603

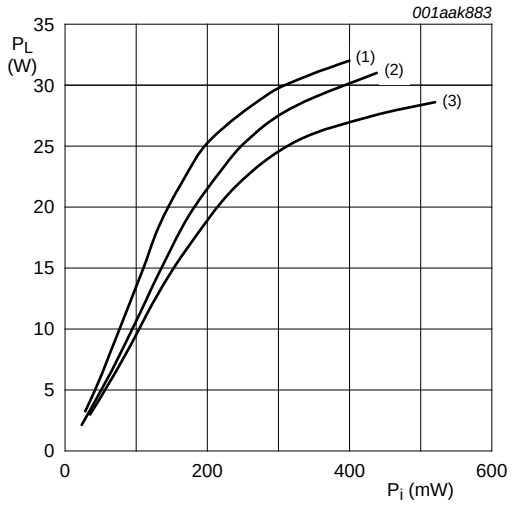
[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

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8. Test information

8.1 Performance curves



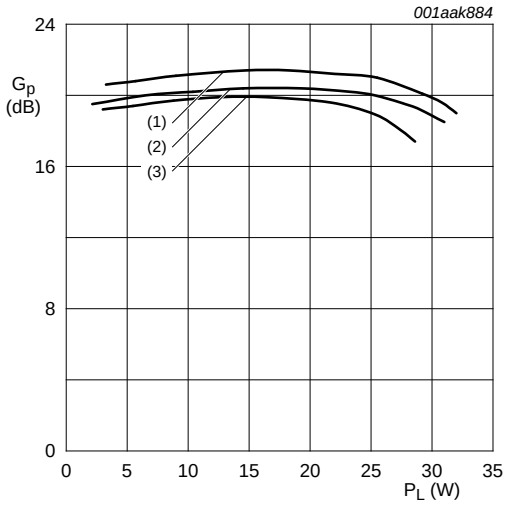
V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 3. Load power as a function of input power; typical values



V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

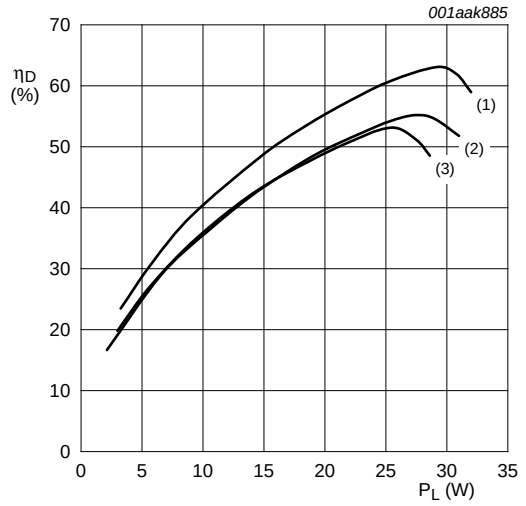
(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 4. Power gain as a function of load power; typical values

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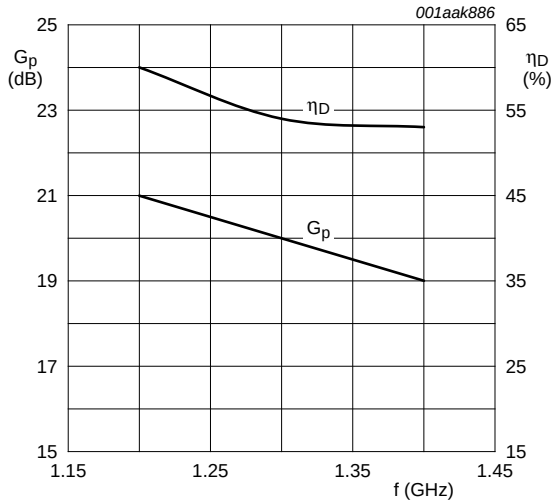
V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

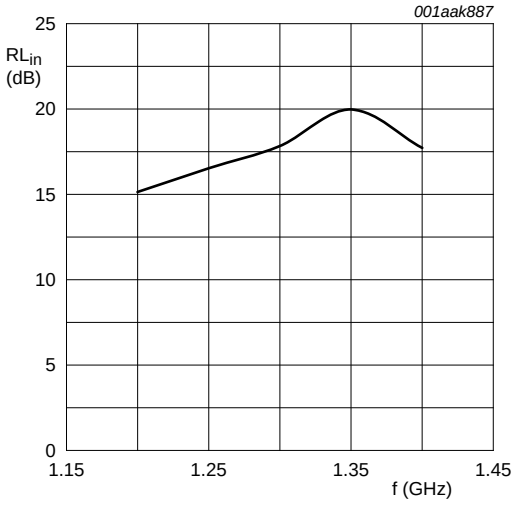
(3) f = 1400 MHz

Fig 5. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

Fig 6. Power gain and drain efficiency as function of frequency; typical values



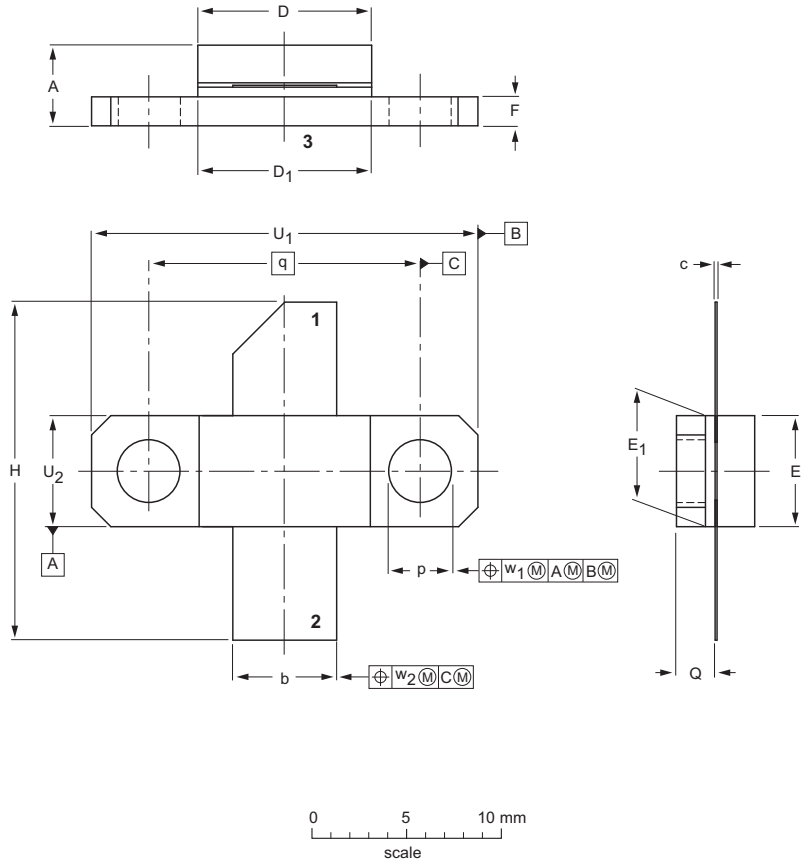
P_L = 25 W; V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

Fig 7. Input return loss as a function of frequency; typical values

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9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-28~~ 12-05-02

Fig 8. Package outline SOT467C

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10. Abbreviations

Table 11. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H0514-25#5	20150901	Product data sheet		BLL6H0514-25_4
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLL6H0514-25_4	20100330	Product data sheet	-	BLL6H0514-25_3
BLL6H0514-25_3	20100223	Product data sheet	-	BLL6H0514-25_2
BLL6H0514-25_2	20090317	Objective data sheet	-	BLL6H0514-25_1
BLL6H0514-25_1	20090305	Objective data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 1 September 2015
Document identifier: BLL6H0514-25#5

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