BLP35M805

Power LDMOS transistor

Rev. 1 — 24 February 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

5 W LDMOS power transistor for broadcast, ISM and A&D applications at frequencies from HF to 3500 MHz.

The BLP35M805 driver is designed for high power CW applications and is assembled in a high performance thermally enhanced plastic package.

Table 1. Typical performance

RF performance at V_{DS} = 32 V; I_{Dq} = 50 mA; T_{case} = 25 °C in a class-AB application circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
CW	2450	50	32	5	20	50
	3500	100	32	5	9.6	33

1.2 Features and benefits

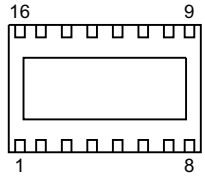
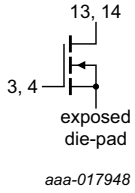
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (HF to 3500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Broadcast, ISM and A&D applications in the frequency range from HF to 3500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol [1]
1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 15, 16	n.c.	 Transparent top view	
3, 4	gate		
13, 14	drain		
exposed die-pad	source [2]		

[1] To be used in single ended applications only.

[2] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP35M805	HVSON16	plastic thermal enhanced very thin small outline package; no leads;16 terminals; body 4 × 6 × 0.85 mm	SOT1371-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 1 W	6.4	K/W

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6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.09 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 9 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	−1.4	-	+1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	1.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 mA	-	80	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V; I_D = 315 mA	-	2	-	Ω

Table 7. RF characteristics

A derivative functional RF test is performed in production. The performance as mentioned below is verified by design and characterization in an Ampleon class-AB application board.

Test signal: pulsed CW; δ = 10%; t_p = 100 μs; V_{DS} = 28 V; I_{Dq} = 55 mA; T_{case} = 25 °C; f = 2140 MHz

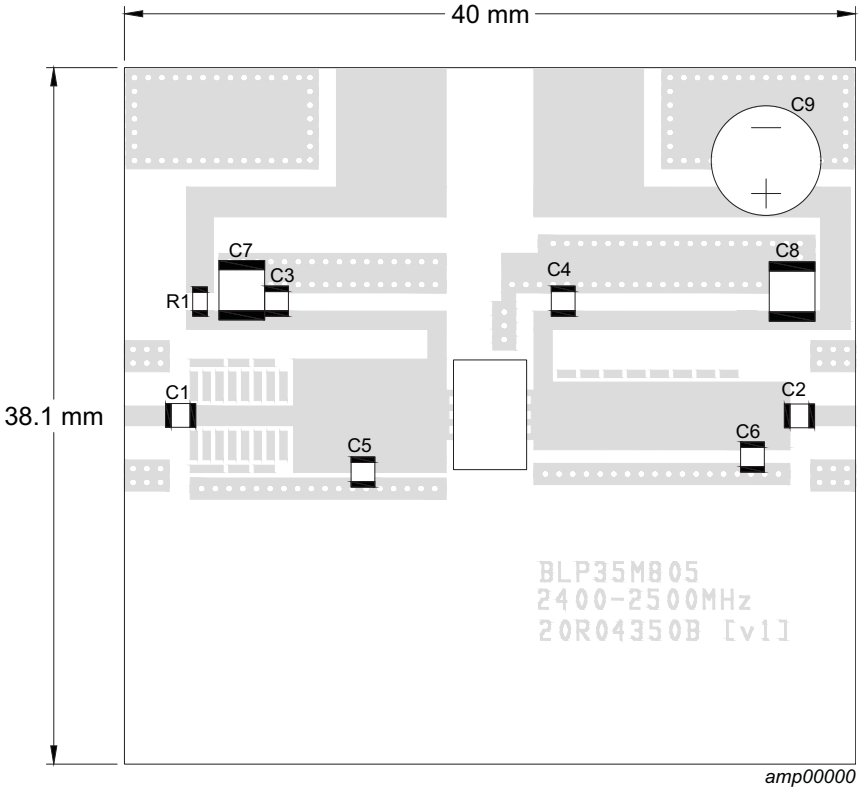
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 0.75 W	17	18	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 0.75 W	15	17	-	%
$P_{L(1dB)}$	output power at 1 dB gain compression		5	-	-	W

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7. Application information

7.1 Application circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 8 for list of components.

Fig 1. Component layout

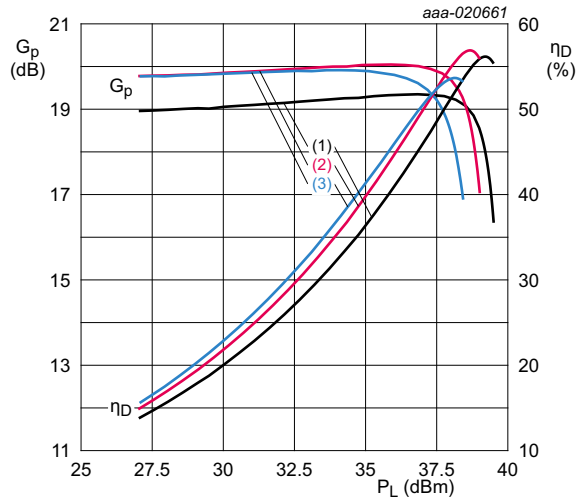
Table 8. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	13 pF	ATC 100A
C5	multilayer ceramic chip capacitor	2.2 pF	ATC 100A
C6	multilayer ceramic chip capacitor	1.4 pF	ATC 100A
C7, C8	multilayer ceramic chip capacitor	1 μF, 50 V	Murata: GRM32RR71H105KA01L
C9	electrolytic capacitor	10 μF, 63 V	
R1	chip resistor	5.1 Ω	SMD 0805

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7.2 Graphical data



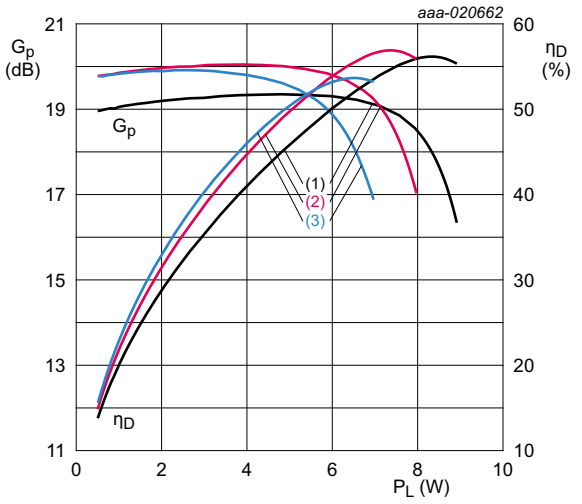
V_{DS} = 32 V; I_{Dq} = 50 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 2. Power gain and drain efficiency as function of output power; typical values



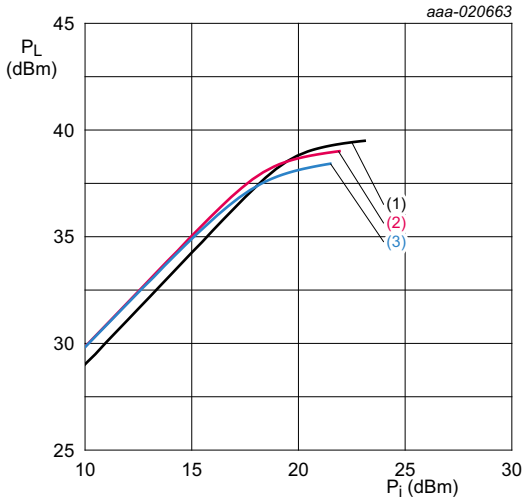
V_{DS} = 32 V; I_{Dq} = 50 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



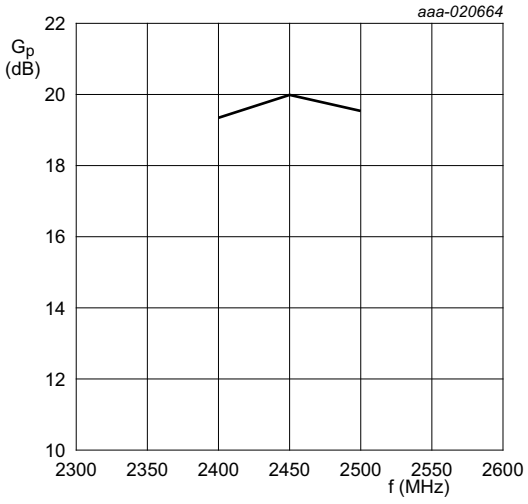
V_{DS} = 32 V; I_{Dq} = 50 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Output power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; P_L = 5 W.

Fig 5. Power gain as a function of frequency; typical values

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8. Test information

8.1 Ruggedness in class-AB operation

The BLP35M805 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 50 mA; P_L = 5 W.

8.2 Impedance information

Table 9. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 55 mA; V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
2400	1.3 – j5.2	4.2 + j1.3
2450	1.3 – j5.6	4.1 + j0.7
2500	1.3 – j6.0	4.0 + j0.1

[1] Z_S and Z_L defined in Figure 6.

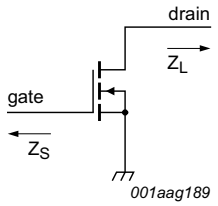
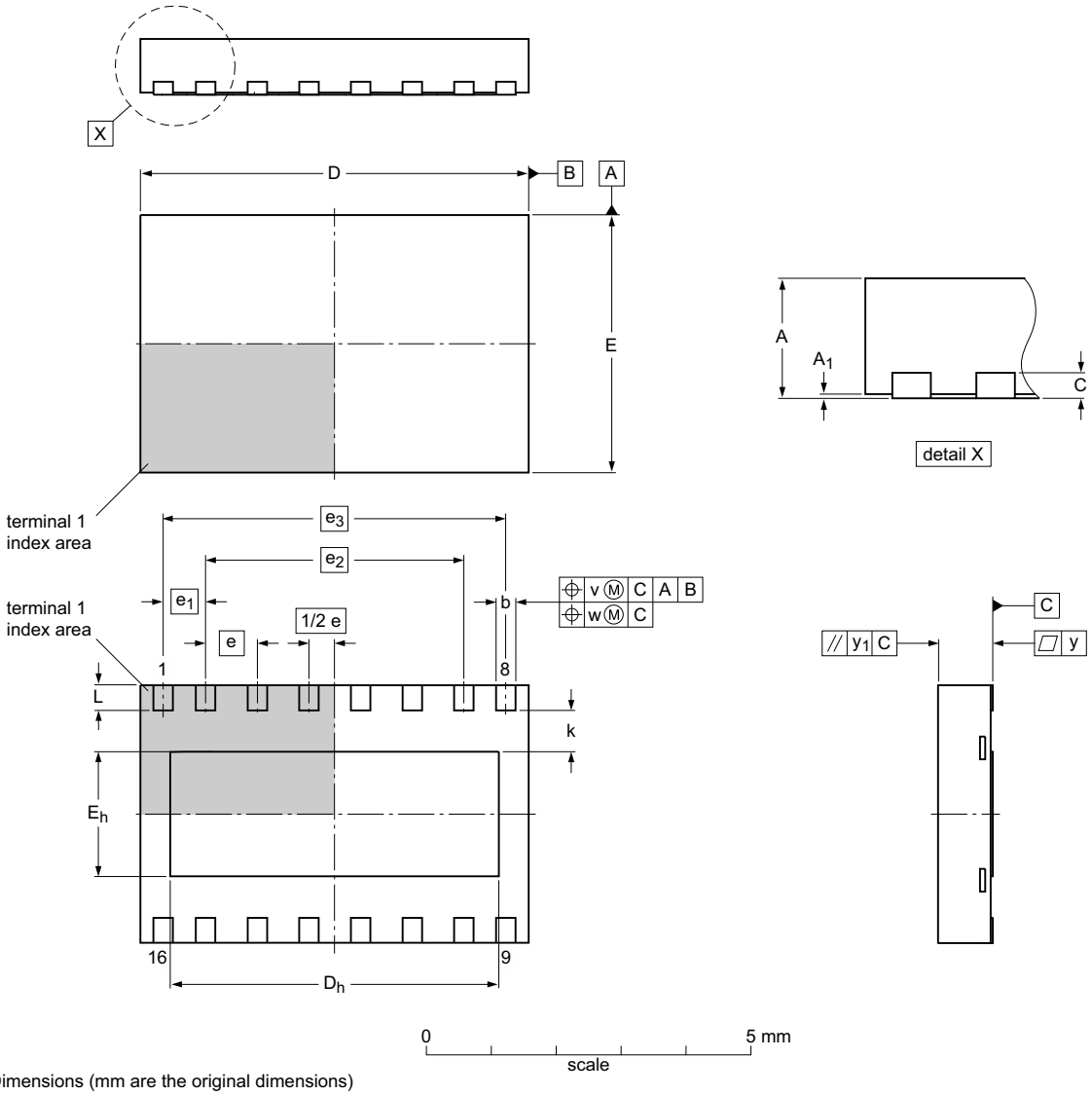


Fig 6. Definition of transistor impedance

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9. Package outline

HVSON16: plastic thermal enhanced very thin small outline package; no leads; 16 terminals; body 4 x 6 x 0.85 mm **SOT1371-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	C	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	e_3	L	k	v	w	y	y_1
	max	1.00	0.05	0.35		6.1	5.2	4.1	2.0					0.5	0.70				
mm	nom	0.85	0.03	0.30	0.2	6.0	5.1	4.0	1.9	0.8	0.65	4.0	5.3	0.4	0.65	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		5.9	5.0	3.9	1.8					0.3	0.60				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1371-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1371-1		MO-229				~~14-05-19~~ 14-08-26

Fig 7. Package outline SOT1371-1 (HVSON16)

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10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
A&D	Aerospace and Defense
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP35M805 v.1	20160224	Product data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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