BLP8G05S-200; BLP8G05S-200G

Power LDMOS transistor

Rev. 2 — 1 October 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base stations applications at frequencies from 400 MHz to 500 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C, I_{Dq} = 2 mA in an application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	440	28	210	21	81

1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Easy power control
- Designed for ISM operation (400 MHz to 500 MHz)
- Input integration for simple board design
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

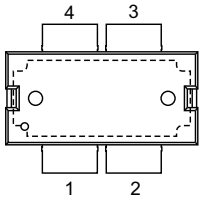
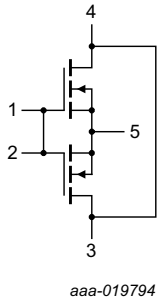
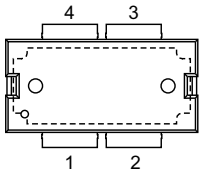
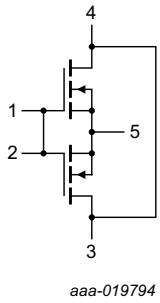
1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 400 MHz to 500 MHz frequency range

2. Pinning information

Table 2. Pinning

All pins must be connected for correct operation and to prevent damage to the device.

Pin	Description	Simplified outline	Graphic symbol
BLP8G05S-200 (SOT1138-2)			
1, 2	gate		
3, 4	drain		
5	source [1]		
BLP8G05S-200G (SOT1204-2)			
1, 2	gate		
3, 4	drain		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP8G05S-200	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1138-2
BLP8G05S-200G	HSOP4	plastic, heatsink small outline package; 4 leads	SOT1204-2

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_{case}	case temperature		-	150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 200 W	0.5	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 320 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	52	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.2 A	-	20	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.2 A	-	0.08	-	Ω

Table 7. RF characteristics

Test signal: CW at 440 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 210 W	19.5	21	-	dB
RL_{in}	input return loss	P_L = 210 W	-	−15	−11	dB
η_D	drain efficiency	P_L = 210 W	73	77	-	%

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7. Test information

7.1 Ruggedness in class-AB operation

The BLP8G05S-200 and BLP8G05S-200G are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 20 mA; P_L = 200 W (CW); f = 440 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 20 mA; V_{DS} = 28 V. Z_S and Z_L defined in Figure 1.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
440	1.5 + j0.7	1.1 + j0.14

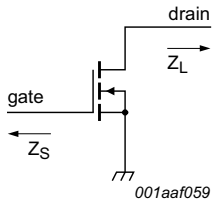
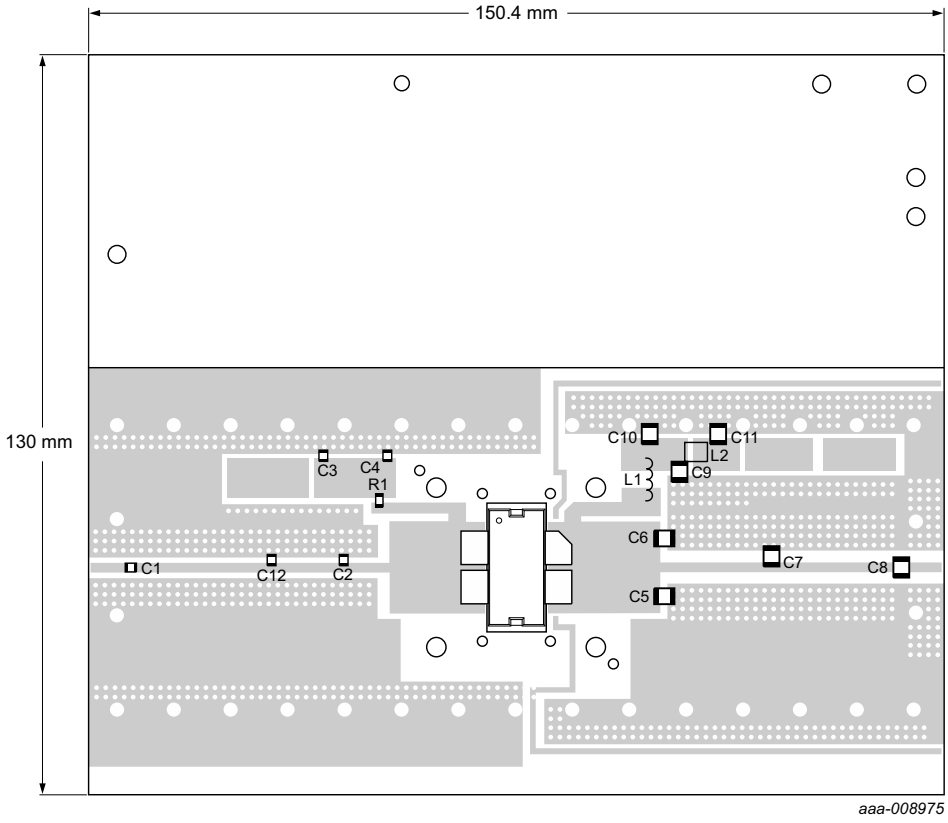


Fig 1. Definition of transistor impedance

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.762 mm.

See Table 9 for list of components.

Fig 2. Component layout for test circuit

Table 9. List of components

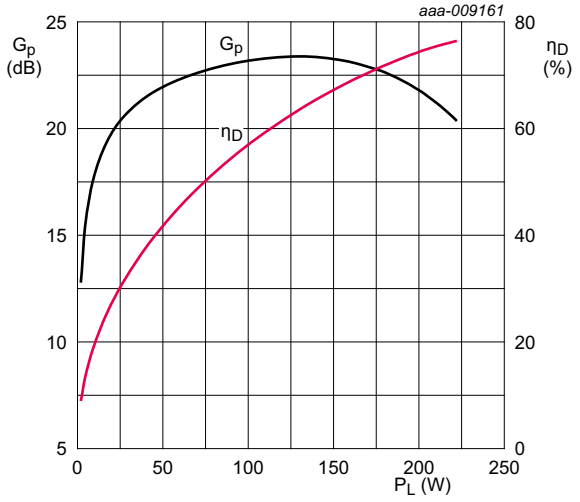
For test circuit, see Figure 2.

Component	Description	Value	Remarks
C1, C3	multilayer ceramic chip capacitor	160 pF	ATC800A
C2	multilayer ceramic chip capacitor	39 pF	ATC800A
C4, C9	multilayer ceramic chip capacitor	910 pF	ATC800B
C5, C6	multilayer ceramic chip capacitor	33 pF	ATC800B
C7	multilayer ceramic chip capacitor	15 pF	ATC800B
C8, C10	multilayer ceramic chip capacitor	130 pF	ATC800B
C11	electrolytic capacitor	220 μF, 63 V	
C12	multilayer ceramic chip capacitor	4.3 pF	ATC800A
R1	chip resistor	10 Ω	Philips: SMD 1206
L1	copper wire	6 turns	
L2	copper foil	-	

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7.4 Graphical data

7.4.1 CW



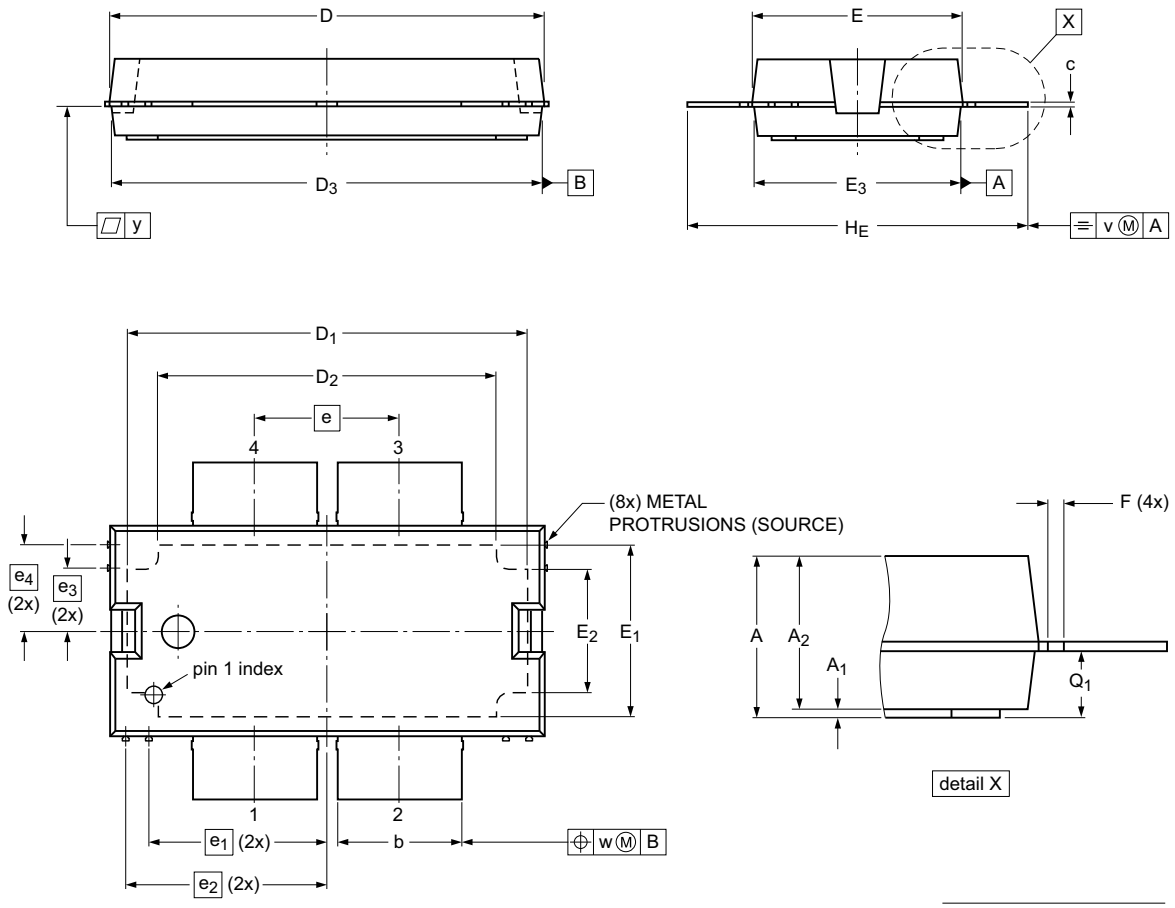
V_{DS} = 28 V; I_{Dq} = 2 mA; f = 440 MHz.

Fig 3. Power gain and drain efficiency as function of output power; typical values

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8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat) **SOT1138-2**



Q_1	v	w	y
1.62			0.1
1.57	0.25	0.25	
1.52			

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	$D^{(1)}$	D_1	D_2	D_3	$E^{(1)}$	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	F	H_E
	max	3.9	0.2	3.65	5.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83							16.16
mm	nom		0.1	3.60	5.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	6.85	8.45	9.55	2.97	4.07	0.4	15.96
	min		0	3.55	5.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73							15.76

Note
1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b do not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

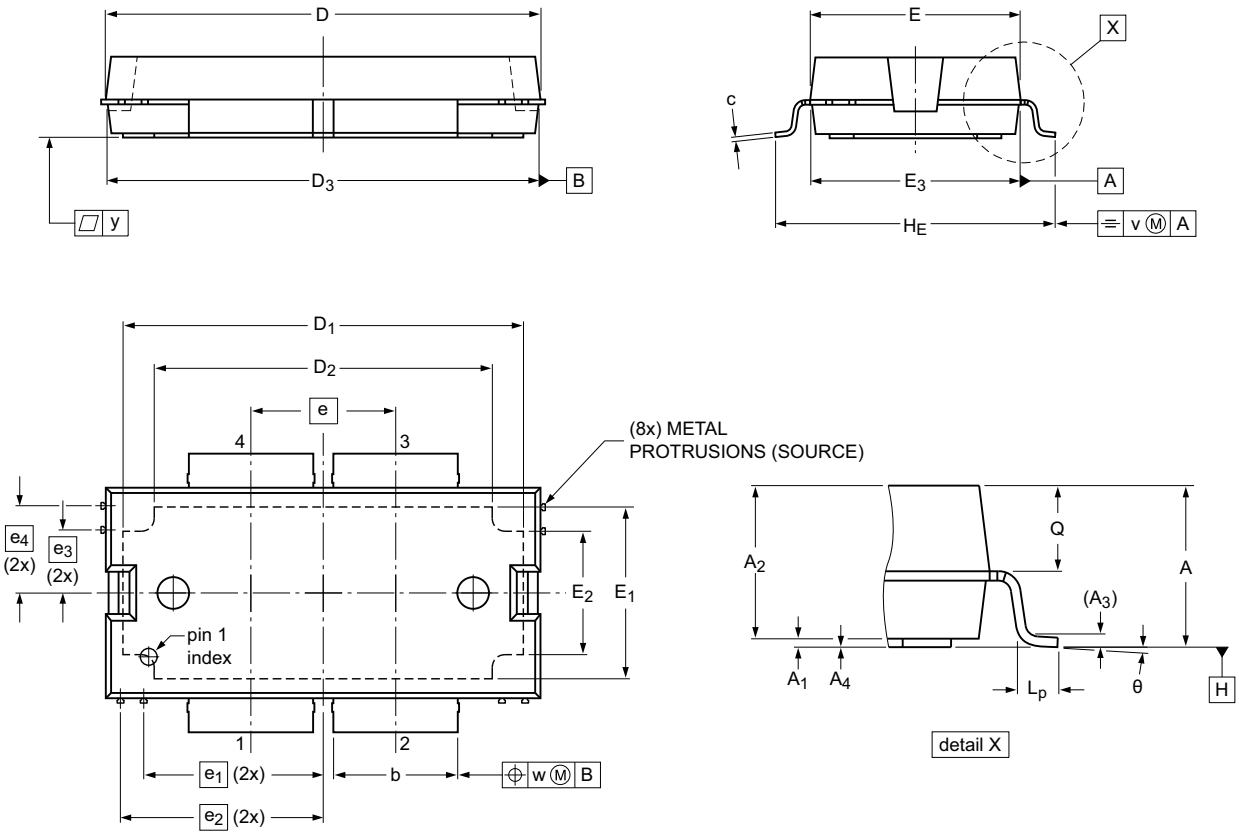
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1138-2						~~15-01-13~~ 15-06-04

Fig 4. Package outline SOT1138-2 (HSOP4F)

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HSOP4: plastic, heatsink small outline package; 4 leads **SOT1204-2**



L_p	Q	v	w	y	θ
1.10	2.07			0.1	7°
0.95	2.02	0.25	0.25		3°
0.80	1.97				0°

Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	A_4	b	c	$D^{(1)}$	D_1	D_2	D_3	$E^{(1)}$	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	H_E
max	3.9	0.2	3.65		0.06	5.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83						13.5
mm nom		0.1	3.60	0.35	0	5.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	6.85	8.45	9.55	2.97	4.07	13.2
min		0	3.55		-0.02	5.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73						12.9

Note
1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b does not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.
3. Dimension A_4 is measured with respect to bottom of the heatsink DATUM H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.

sot1204-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1204-2						~~15-01-14~~ 15-06-04

Fig 5. Package outline SOT1204-2 (HSOP4)

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP8G05S-200_8G05S-200G v.2	20151001	Product data sheet	-	BLP8G05S-200_8G05S-200G v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon • Legal texts have been adapted to the new company name where appropriate			
BLP8G05S-200_8G05S-200G v.1	20150917	Product data sheet	-	-

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