BLP9H10-30G

Power LDMOS transistor

Rev. 1 — 20 July 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

30 W plastic LDMOS power transistor for base station applications at frequencies from 616 MHz to 960 MHz.

Table 1. Typical performance 806 MHz

Typical RF performance at T_{case} = 25 °C in a class-AB demo circuit. V_{DS} = 50 V; I_{Dq} = 100 mA.

Test signal	f	V_{DS}	P_L	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	791 to 821	50	32	19.5	13.8	–47.3 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

Table 2. Typical performance 681 MHz

Typical RF performance at T_{case} = 25 °C in a class-AB demo circuit. V_{DS} = 50 V; I_{Dq} = 100 mA.

Test signal	f	V_{DS}	P_L	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	616 to 746	50	32	20.2	15.1	–49.4 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

Table 3. Typical performance 881.5 MHz

Typical RF performance at T_{case} = 25 °C in a class-AB demo circuit. V_{DS} = 50 V; I_{Dq} = 100 mA.

Test signal	f	V_{DS}	P_L	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	758 to 960	50	31	18.7	12.7	–51.1 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

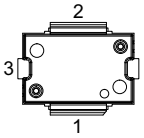
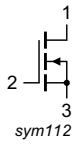
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- High power gain
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- FDD/TDD LTE
- GSM EDGE
- CDMA
- W-CDMA
- MC-GSM
- WiMAX

2. Pinning information

Table 4. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 5. Ordering information

Type number	Package		
	Name	Description	Version
BLP9H10-30G	-	plastic; heatsink small outline package; 2 leads	SOT1483-1

4. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	105	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 80 °C		
		P_L = 1.6 W	2.36	K/W
		P_L = 8.0 W	2.30	K/W

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6. Characteristics

Table 8. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.18 mA	105	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 18 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 100 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	3.0	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.9 A	-	1.4	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 0.63 A	-	1170	1620	mΩ

Table 9. RF characteristics

Test signal: pulsed CW; t_p = 471 μs; δ = 8.6 %; f = 960 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 32 dBm	17.3	18.3	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 32 dBm	-	−25	−15	dB
η_D	drain efficiency	$P_{L(AV)}$ = 32 dBm	10	13.5	-	%
$P_{L(1dB)}$	output power at 1 dB gain compression		43.8	45.2	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression		44.8	45.9	-	dBm

7. Test information

7.1 Ruggedness in class-AB operation

The BLP9H10-30G is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 25 W ($P_{L(1dB)}$); f = 791 MHz; pulsed CW (t_p = 100 μs; δ = 10 %).

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7.2 Impedance information

Table 10. Typical impedance of device per section

Measured load-pull data of main device; I_{Dq} = 100 mA (per section); V_{DS} = 50 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	22.5 – j14.7	18.8 + j11.7	36.3	55.6	15.5
698	24.0 – j12.2	11.7 + j10.4	35.0	52.6	16.0
720	23.7 – j12.0	11.7 + j10.5	36.2	54.4	16.2
746	23.3 – j11.7	11.8 + j10.4	36.7	55.4	16.3
757	23.4 – j11.6	11.3 + j10.0	37.2	55.0	16.2
769	22.9 – j12.6	9.8 + j9.9	37.4	55.7	16.3
790	23.0 – j13.7	12.7 + j9.7	37.2	54.6	16.2
805	23.2 – j13.8	12.8 + j9.7	36.5	54.1	16.1
820	23.1 – j14.4	12.1 + j8.3	36.3	51.9	15.8
869	23.4 – j16.4	12.8 + j9.5	35.7	53.0	15.9
880	23.5 – j16.6	10.5 + j8.7	35.7	53.3	15.9
894	23.9 – j17.4	10.4 + j8.6	35.4	52.8	15.9
925	24.7 – j18.6	10.3 + j8.4	35.5	52.5	15.8
942	25.2 – j19.8	10.1 + j8.4	35.5	52.9	15.7
960	26.0 – j20.8	9.0 + j8.2	36.3	54.4	15.7
Maximum drain efficiency load					
600	22.2 – j14.2	16.3 + j16.4	31.2	58.8	16.5
698	22.5 – j11.0	7.8 + j16.3	26.1	61.3	17.9
720	22.0 – j11.1	7.8 + j16.4	25.7	62.1	18.1
746	21.1 – j10.9	7.9 + j16.4	25.3	61.8	18.2
757	21.7 – j11.8	9.9 + j15.7	29.7	61.5	17.8
769	21.3 – j12.5	7.8 + j15.1	27.7	63.1	18.0
790	21.6 – j13.2	8.1 + j14.3	29.8	63.9	17.8
805	21.5 – j13.2	6.6 + j15.2	24.4	63.1	18.1
820	21.5 – j13.7	7.2 + j13.5	28.8	62.5	17.6
869	22.1 – j15.7	6.5 + j12.7	28.8	61.9	17.4
880	21.7 – j16.6	6.3 + j13.6	26.0	62.5	17.8
894	22.3 – j17.5	6.7 + j13.4	27.1	62.3	17.6
925	22.6 – j18.3	5.4 + j12.5	25.4	62.3	17.9
942	23.1 – j19.4	4.7 + j11.9	25.3	62.2	17.4
960	24.2 – j20.4	4.9 + j11.0	28.1	62.6	17.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

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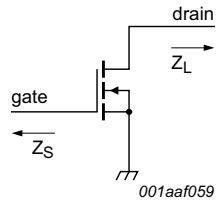
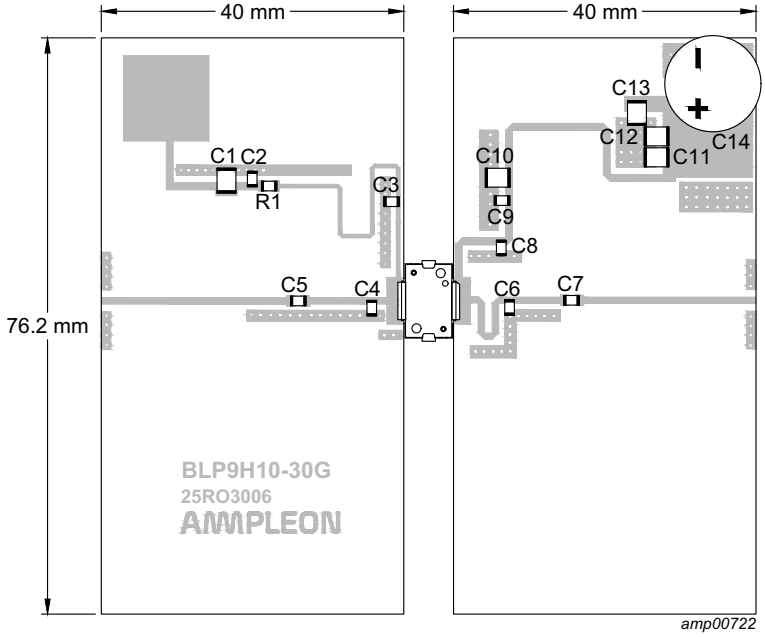


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

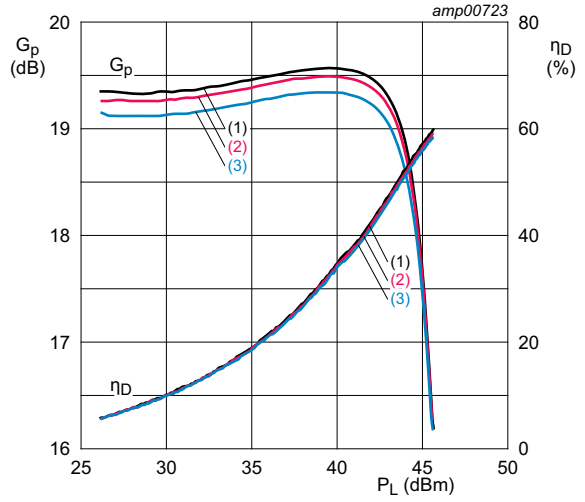
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C10, C11, C12, C13	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata: Hi-Q SMD 1210
C2, C9	multilayer ceramic chip capacitor	100 nF, 100 V	Murata: Hi-Q SMD 0805
C3, C5, C7, C8	multilayer ceramic chip capacitor	82 pF	Murata: Hi-Q SMD 0805
C4	multilayer ceramic chip capacitor	7.5 pF	Murata: Hi-Q SMD 0805
C6	multilayer ceramic chip capacitor	3.0 pF	Murata: Hi-Q SMD 0805
C14	electrolytic capacitor	470 μF, 100 V	
R1	resistor	4.7 Ω, 1 %	SMD 0805

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7.4 Graphical data

7.4.1 Pulsed CW



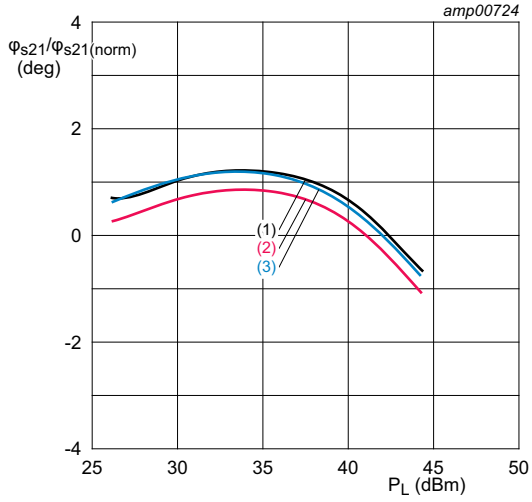
V_{DS} = 50 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 10 %.

(1) f = 791 MHz

(2) f = 803 MHz

(3) f = 821 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA; t_p = 100 μs; δ = 10 %.

(1) f = 791 MHz

(2) f = 803 MHz

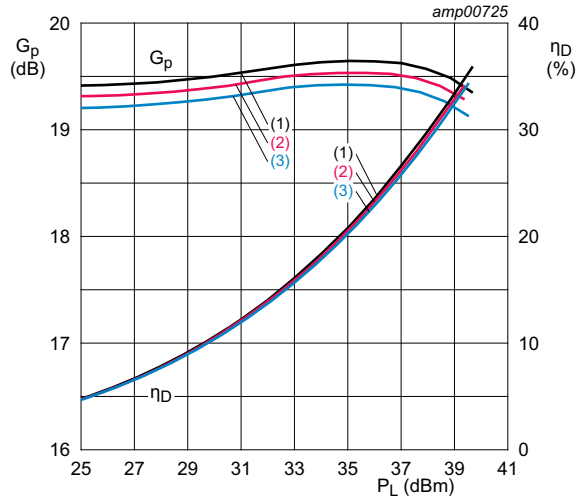
(3) f = 821 MHz

Fig 4. Normalized phase response (AM to PM) as a function of output power; typical values

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7.4.2 1-Carrier W-CDMA

Test model 1; PAR = 9.9 dB at 0.01 % probability on CCDF.



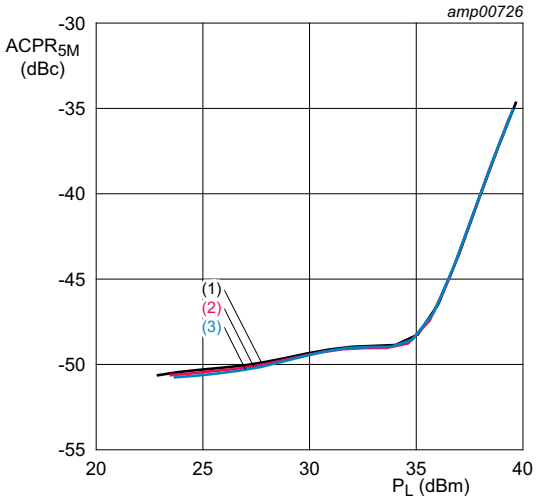
V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 791 MHz

(2) f = 803 MHz

(3) f = 821 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



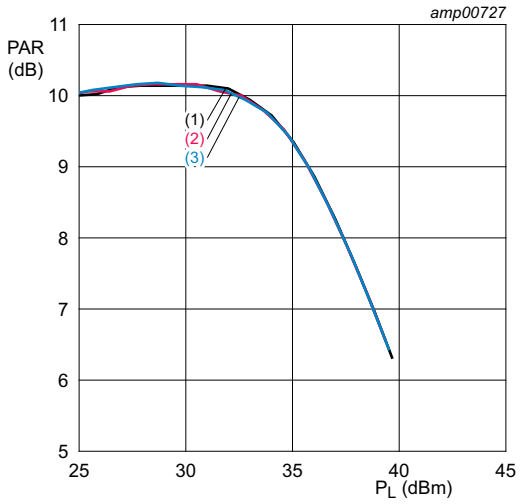
V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 791 MHz

(2) f = 803 MHz

(3) f = 821 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 791 MHz

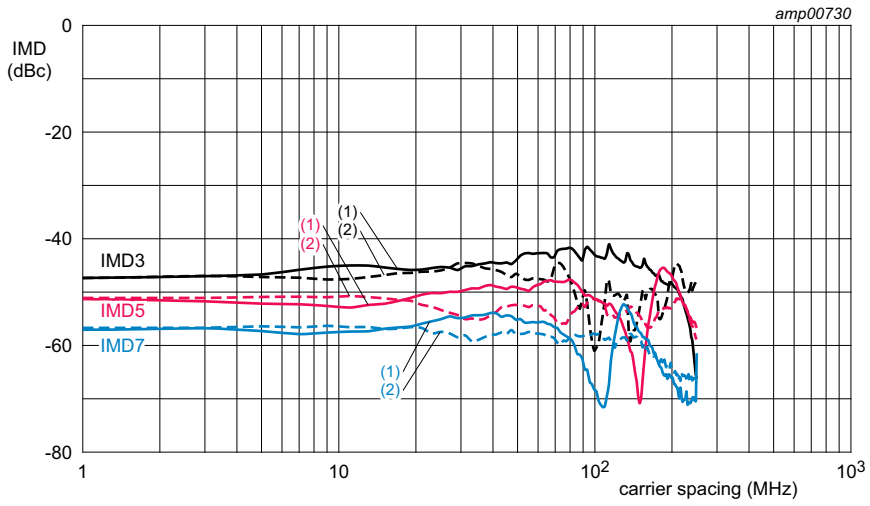
(2) f = 803 MHz

(3) f = 821 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

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7.4.3 2-Tone VBW



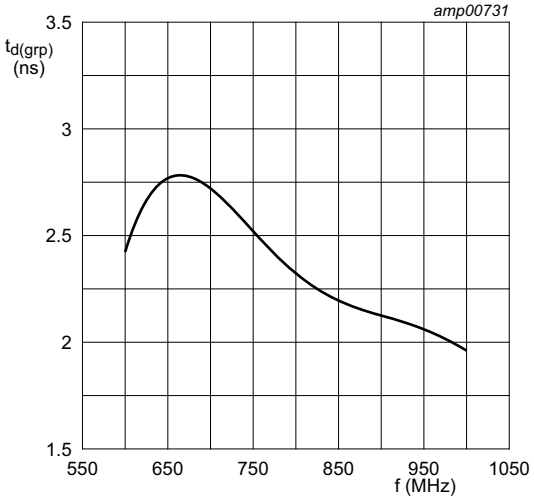
V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) IMD low

(2) IMD high

Fig 8. VBW capability

7.4.4 Group delay



V_{DS} = 50 V; I_{Dq} = 100 mA.

Fig 9. Group delay time as a function of frequency; typical values

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8. Package outline

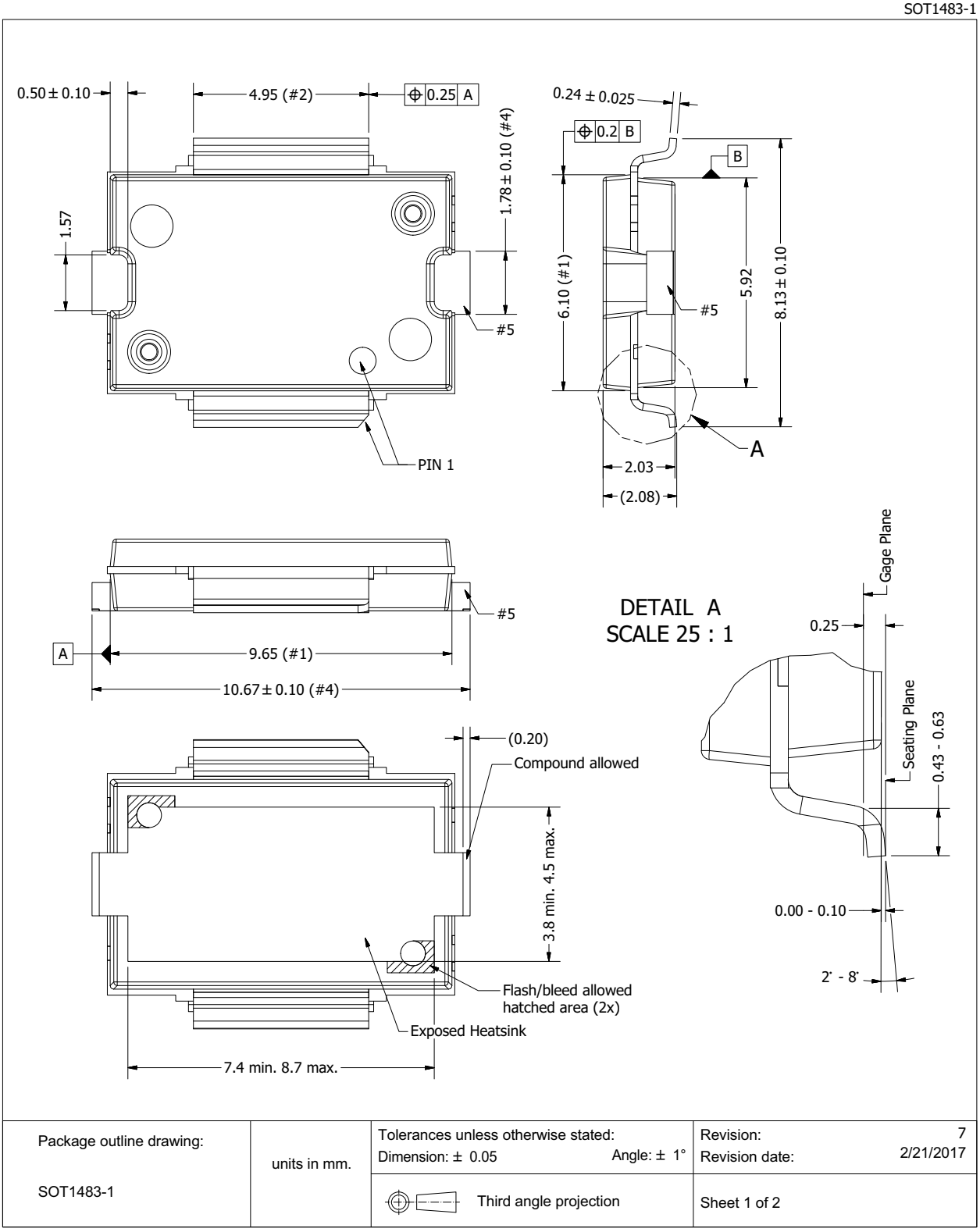
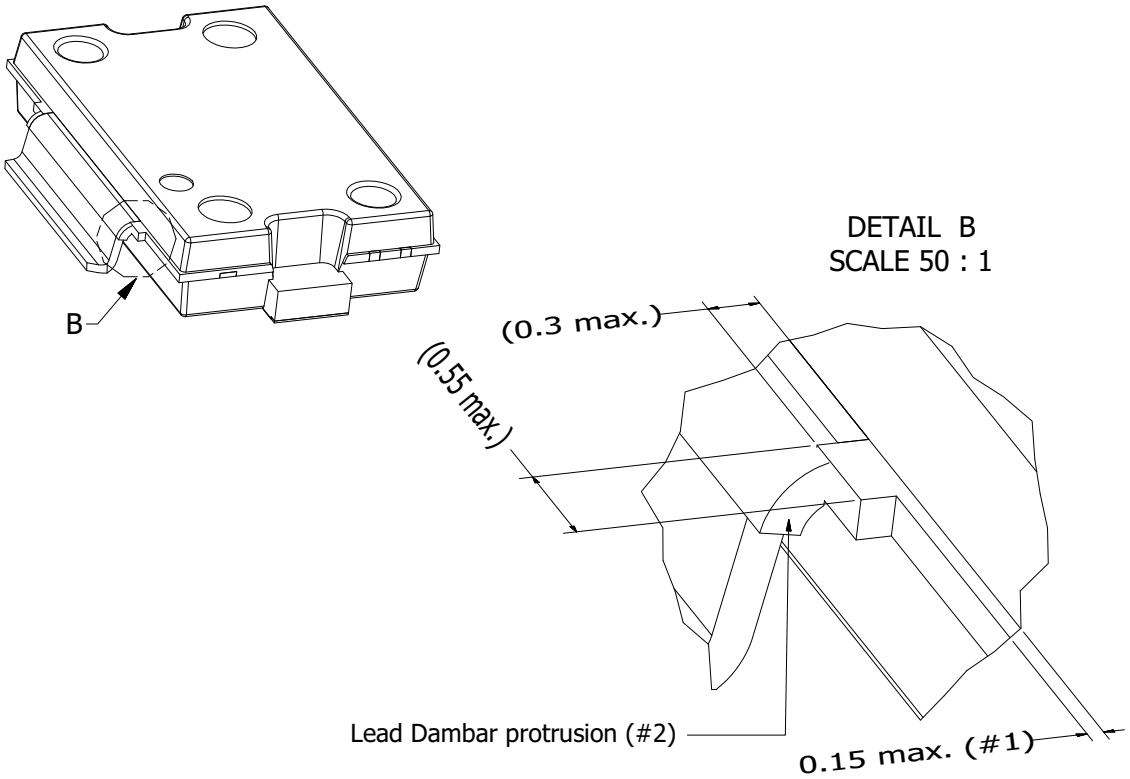


Fig 10. Package outline SOT1483-1 (sheet 1 of 2)

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SOT1483-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. The mold protrusion is maximum 0.15 mm per side. See also detail B. In the dambar area max. protrusion is 0.55mm max. in lenght and 0.3 mm max. in width (4x) See also detail B.
(2)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(3)	The leads and exposed heatsink are plated with matte Tin (Sn).
(4)	Dimensions (Heatsink ears) 10,67 and 1,78 do not include mouldprotrusion. Overall Max. dimensions incl. mould protrusions is 10,92 mm. (max.) and 2,03 mm. (max.).
(5)	Surfaces may remain unplated (not solderable surfaces).



Package outline drawing: SOT1483-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1° Third angle projection	Revision: 7 Revision date: 2/21/2017 Sheet 2 of 2

Fig 11. Package outline SOT1483-1 (sheet 2 of 2)

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
FDD	Frequency Division Duplex
GSM	Global System for Mobile Communication
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MC-GSM	Multi Carrier GSM
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
TDD	Time Division Duplex
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

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11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP9H10-30G v.1	20180720	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 2
2 Pinning information 2
3 Ordering information 2
4 Limiting values 2
5 Thermal characteristics 2
6 Characteristics 3
7 Test information 3
7.1 Ruggedness in class-AB operation 3
7.2 Impedance information 4
7.3 Test circuit 5
7.4 Graphical data 6
7.4.1 Pulsed CW 6
7.4.2 1-Carrier W-CDMA 7
7.4.3 2-Tone VBW 8
7.4.4 Group delay 8
8 Package outline 9
9 Handling information 11
10 Abbreviations 11
11 Revision history 12
12 Legal information 13
12.1 Data sheet status 13
12.2 Definitions 13
12.3 Disclaimers 13
12.4 Trademarks 14
13 Contact information 14
14 Contents 15

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