P-Channel Power MOSFET

-60V, -140mA, 8Ω

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

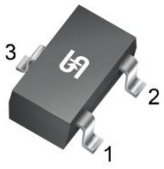
APPLICATIONS

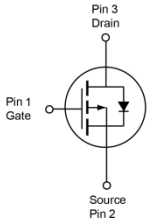
- Low Side Load Switching
- Level Shift Circuits
- General Switch Circuits

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-60	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	8	Ω
	V_{GS} = -4.5V	10	
Q_g		1	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOT-323





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_A = 25°C	I_D	-140	mA
	T_A = 125°C		-61	
Pulsed Drain Current		I_{DM}	-0.56	A
Total Power Dissipation	T_A = 25°C	P_D	298	mW
	T_A = 125°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	420	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. The $R_{\Theta JA}$ limit presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	$V_{GS(TH)}$	-0.9	-1.5	-2.0	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = -60V	I_{DSS}	--	--	-1	μA
	V_{GS} = 0V, V_{DS} = -60V T_J =125°C		--	--	-100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = -10V, I_D = -140mA	$R_{DS(on)}$	--	3.6	8	Ω
	V_{GS} = -4.5V, I_D = -120mA		--	3.9	10	
Forward Transconductance (Note 3)	V_{DS} = -5V, I_D = -140mA	g_{fs}	--	0.5	--	S
Dynamic (Note 3)						
Total Gate Charge	V_{GS} = -10V, V_{DS} = -30V, I_D = -140mA	Q_g	--	1.9	--	nC
Total Gate Charge	V_{GS} = -4.5V, V_{DS} = -30V, I_D = -120mA	Q_g	--	1	--	
Gate-Source Charge		Q_{gs}	--	0.3	--	
Gate-Drain Charge		Q_{gd}	--	0.3	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = -30V f = 1.0MHz	C_{iss}	--	37	--	pF
Output Capacitance		C_{oss}	--	15	--	
Reverse Transfer Capacitance		C_{rss}	--	7	--	
Switching (Note 3)						
Turn-On Delay Time	V_{GS} = -10V, V_{DS} = -30V, I_D = -140mA, R_G = 6Ω	$t_{d(on)}$	--	10	--	ns
Turn-On Rise Time		t_r	--	15	--	
Turn-Off Delay Time		$t_{d(off)}$	--	21	--	
Turn-Off Fall Time		t_f	--	78	--	
Source-Drain Diode						
Forward Voltage (Note 2)	V_{GS} = 0V, I_S = -140mA	V_{SD}	--	--	-1.2	V
Reverse Recovery Time	I_S = -140mA , dI/dt = 100A/μs	t_{rr}	--	24	--	ns
Reverse Recovery Charge		Q_{rr}	--	14	--	nC

Notes:

1. Silicon limited current only.
2. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
3. Switching time is essentially independent of operating temperature.

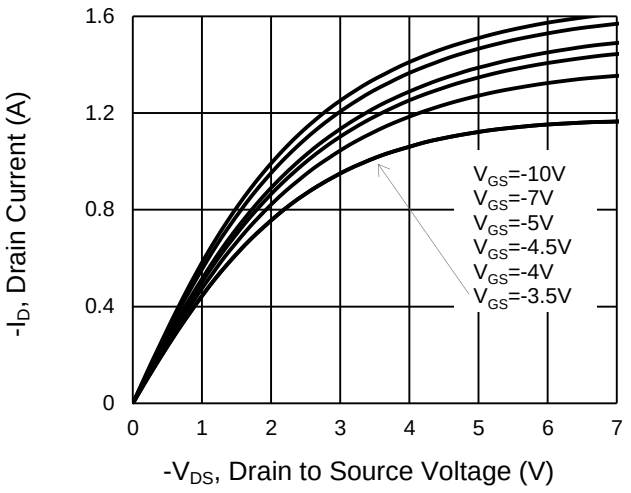
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
BSS84W RFG	SOT-323	3,000pcs / 7” Reel

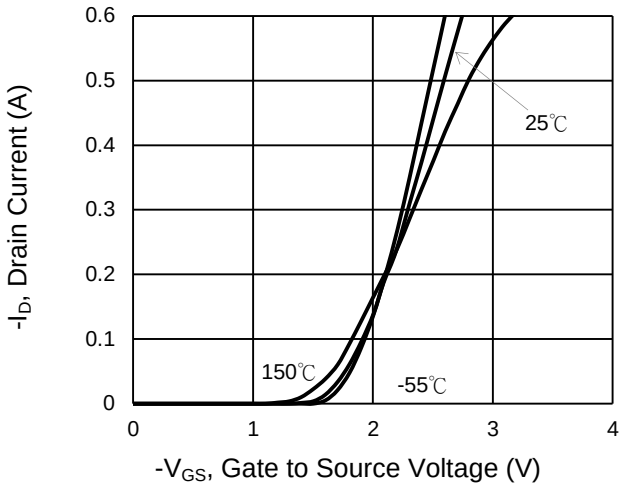
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

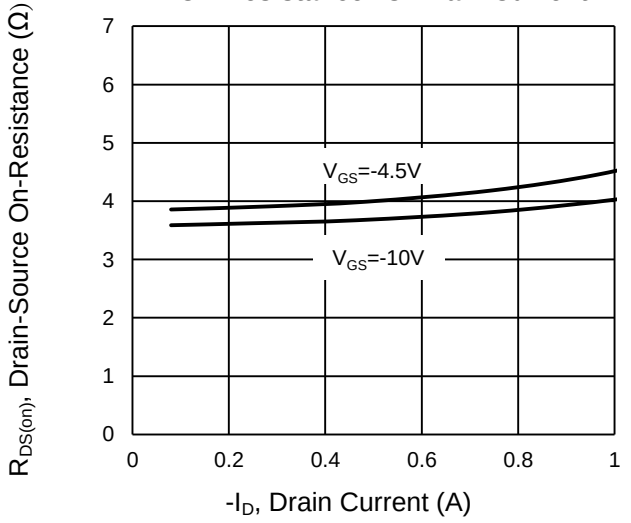
Output Characteristics



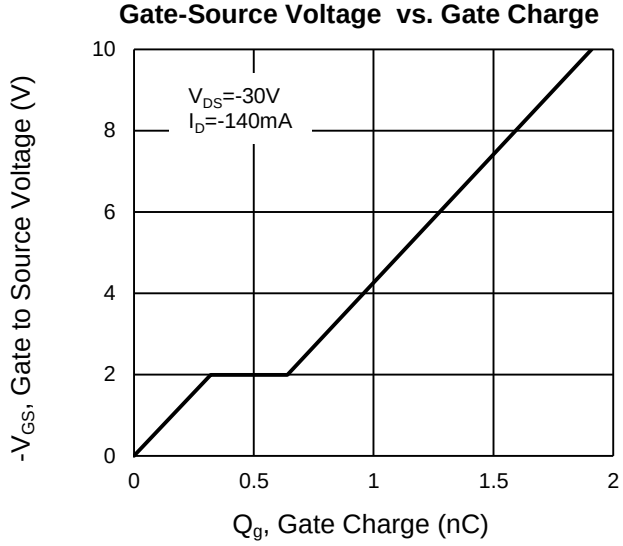
Transfer Characteristics



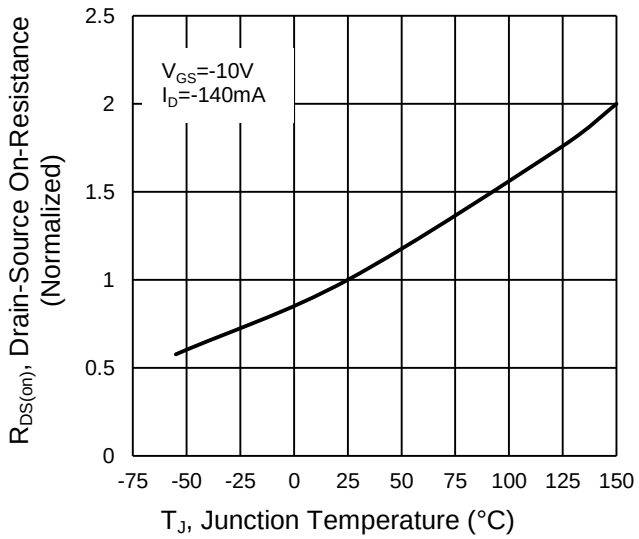
On-Resistance vs. Drain Current



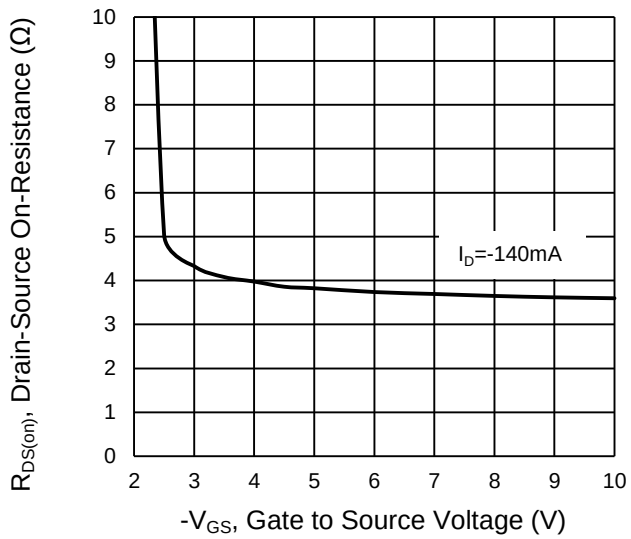
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



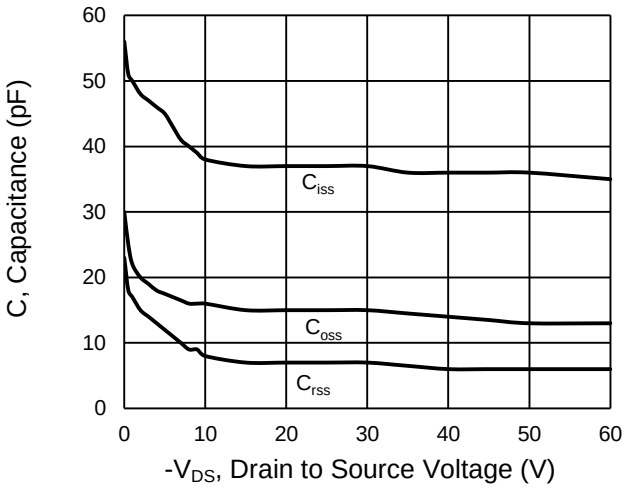
On-Resistance vs. Gate-Source Voltage



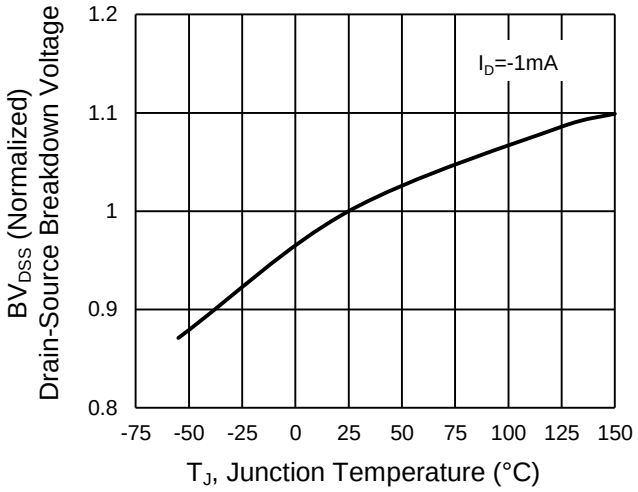
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

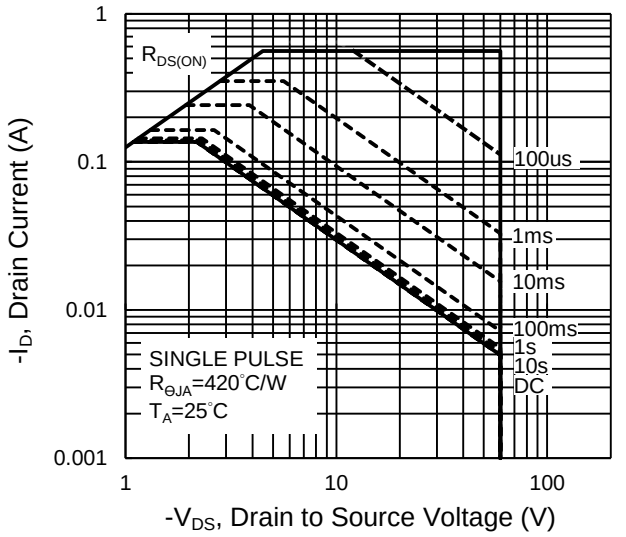
Capacitance vs. Drain-Source Voltage



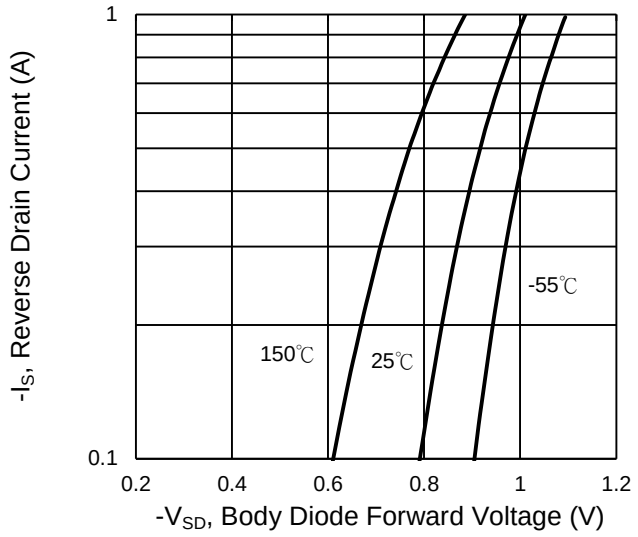
BV_{DSS} vs. Junction Temperature



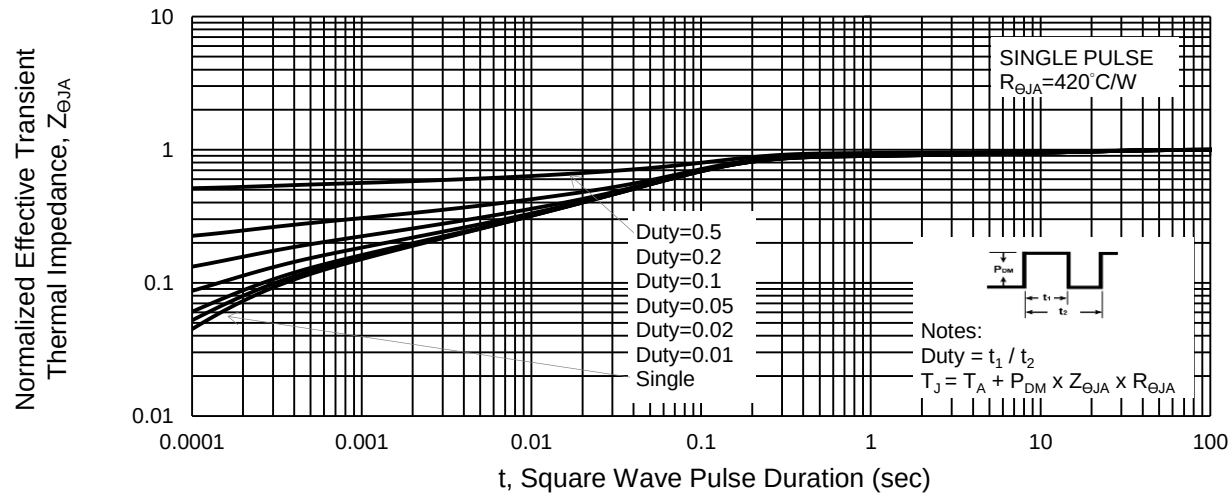
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage

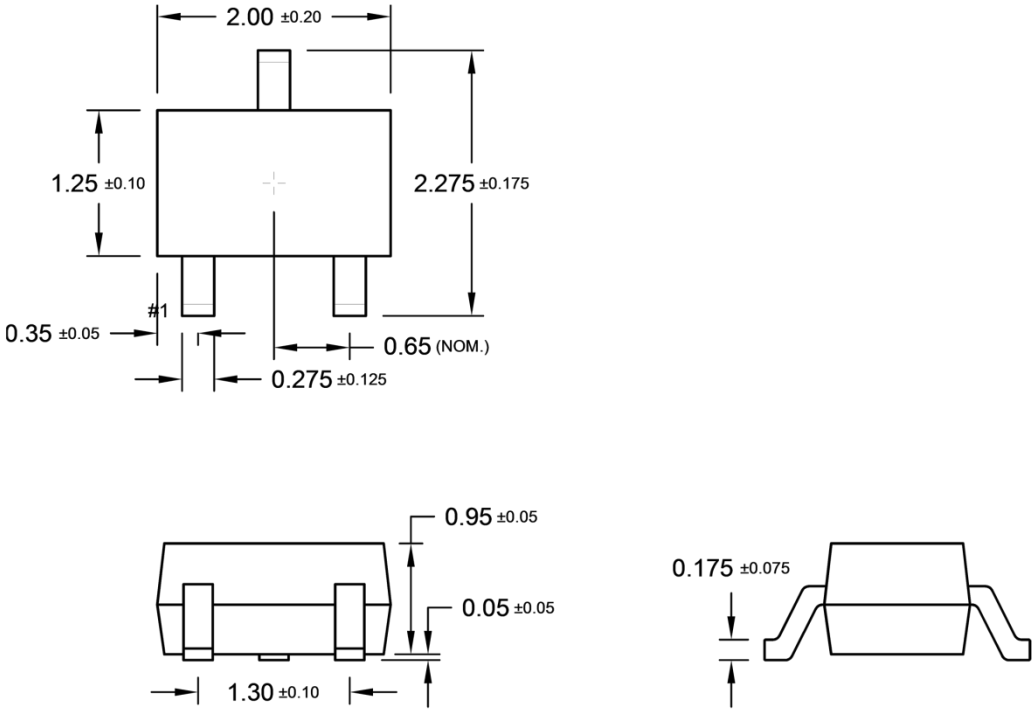


Normalized Thermal Transient Impedance, Junction-to-Ambient

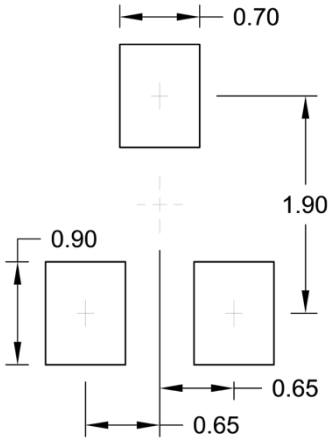


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

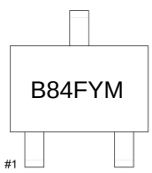
SOT-323



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



B84 = Device code
F = Site Code
Y = Year Code
M = Month code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

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