# 20V N-CHANNEL ENHANCEMENT MODE MOSFET

## Product Summary

| $BV_{DSS}$ | $R_{DS(ON)}$ Max | $I_D$ Max $T_A$ = +25°C |
|---|---|---|
| 20V | 0.99Ω @ $V_{GS}$ = 4.5V | 0.55A |
| | 1.2Ω @ $V_{GS}$ = 2.5V | 0.50A |
| | 1.8Ω @ $V_{GS}$ = 1.8V | 0.41A |
| | 2.4Ω @ $V_{GS}$ = 1.5V | 0.35A |

## Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

## Applications

- General-purpose interfacing switches
- Power-management functions
- Analog switches

## Features and Benefits

- Low Package Profile, 0.42mm Maximum Package Height
- 0.62mm × 0.62mm Package Footprint
- Low On-Resistance
- Very Low Gate Threshold Voltage, 1.0V Maximum
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under separate datasheet (DMN2991UFZQ)**

## Mechanical Data

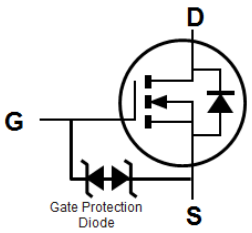
- Package: X2-DFN0606-3
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.001 grams (Approximate)



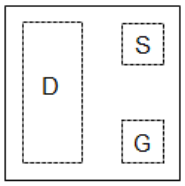

X2-DFN0606-3



Bottom View




Equivalent Circuit




Top View
Package Pin Configuration

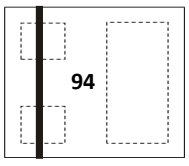
## Ordering Information (Note 4)

| Part Number | Package | Packing | |
|---|---|---|---|
| | | Qty. | Carrier |
| DMN2991UFZ-7B | X2-DFN0606-3 | 10k | Tape & Reel |

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## Marking Information

X2-DFN0606-3




94 = Product Type Marking Code
Bar Denotes Gate and Source Side

Top View


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## Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DSS}$ | 20 | V |
| Gate-Source Voltage | | | $V_{GSS}$ | ±8 | V |
| Continuous Drain Current (Note 5) $V_{GS}$ = 4.5V | Steady State | $T_A$ = +25°C<br>$T_A$ = +75°C | $I_D$ | 0.55<br>0.44 | A |
| Maximum Body Diode Forward Current (Note 6) | | | $I_S$ | 0.7 | A |
| Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%) | | | $I_{DM}$ | 1.5 | A |

## Thermal Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Dissipation (Note 5) | Steady State | $P_D$ | 0.45 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | Steady State | $R_{\theta JA}$ | 279 | °C/W |
| Power Dissipation (Note 6) | Steady State | $P_D$ | 0.53 | W |
| Thermal Resistance, Junction to Ambient (Note 6) | Steady State | $R_{\theta JA}$ | 148 | °C/W |
| Operating and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +150 | °C |

## Electrical Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 7) | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 20 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | 1 | µA | $V_{DS}$ = 16V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | 1 | µA | $V_{GS}$ = ±5V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS** (Note 7) | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | 0.4 | 0.8 | 1.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | — | 0.60 | 0.99 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 100mA |
| | | — | 0.75 | 1.2 | | $V_{GS}$ = 2.5V, $I_D$ = 50mA |
| | | — | 0.90 | 1.8 | | $V_{GS}$ = 1.8V, $I_D$ = 20mA |
| | | — | 1.2 | 2.4 | | $V_{GS}$ = 1.5V, $I_D$ = 10mA |
| | | — | 2.0 | — | | $V_{GS}$ = 1.2V, $I_D$ = 1mA |
| Diode Forward Voltage | $V_{SD}$ | — | 0.6 | 1.0 | V | $V_{GS}$ = 0V, $I_S$ = 150mA |
| **DYNAMIC CHARACTERISTICS** (Note 8) | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 21.5 | — | pF | $V_{DS}$ = 16V, $V_{GS}$ = 0V, f = 1.0MHz |
| Output Capacitance | $C_{oss}$ | — | 4.9 | — | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 3.7 | — | pF | |
| Total Gate Charge | $Q_g$ | — | 0.35 | — | nC | $V_{GS}$ = 4.5V, $V_{DS}$ = 10V, $I_D$ = 250mA |
| Gate-Source Charge | $Q_{gs}$ | — | 0.07 | — | nC | |
| Gate-Drain Charge | $Q_{gd}$ | — | 0.08 | — | nC | |
| Turn-On Delay Time | $t_{D(ON)}$ | — | 5.6 | — | ns | $V_{DD}$ = 10V, $V_{GS}$ = 4.5V, $R_L$ = 47Ω, $R_g$ = 10Ω, $I_D$ = 200mA |
| Turn-On Rise Time | $t_R$ | — | 4.9 | — | ns | |
| Turn-Off Delay Time | $t_{D(OFF)}$ | — | 60.6 | — | ns | |
| Turn-Off Fall Time | $t_F$ | — | 27.6 | — | ns | |
| Reverse Recovery Time | $t_{RR}$ | — | 12.3 | — | ns | $I_F$ = 1.0A, di/dt = 100A/µs |
| Reverse Recovery Charge | $Q_{RR}$ | — | 1.1 | — | nC | $I_F$ = 1.0A, di/dt = 100A/µs |

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.


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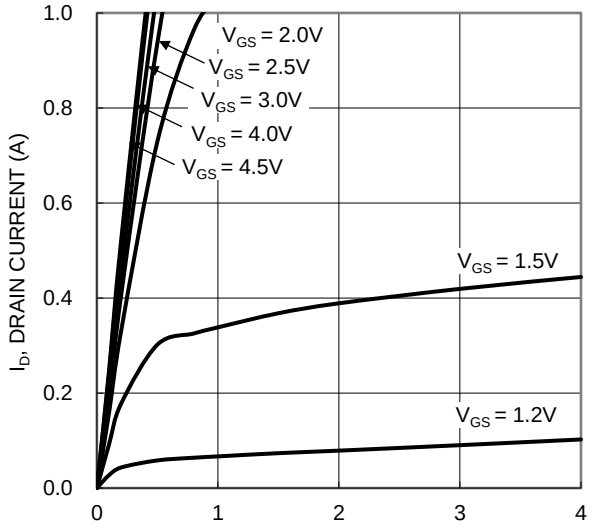



Figure 1. Typical Output Characteristic

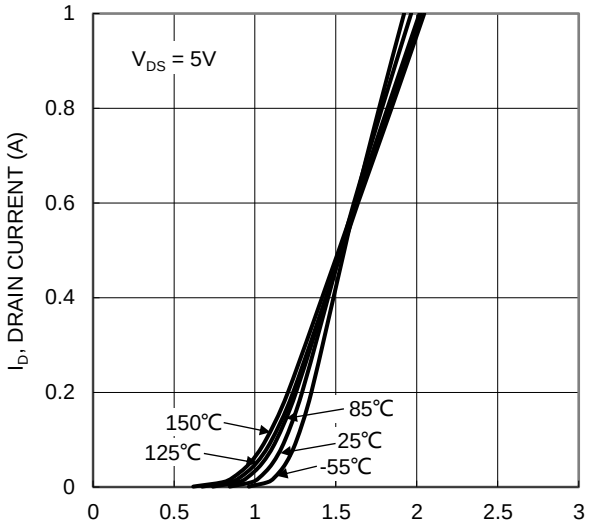



Figure 2. Typical Transfer Characteristic

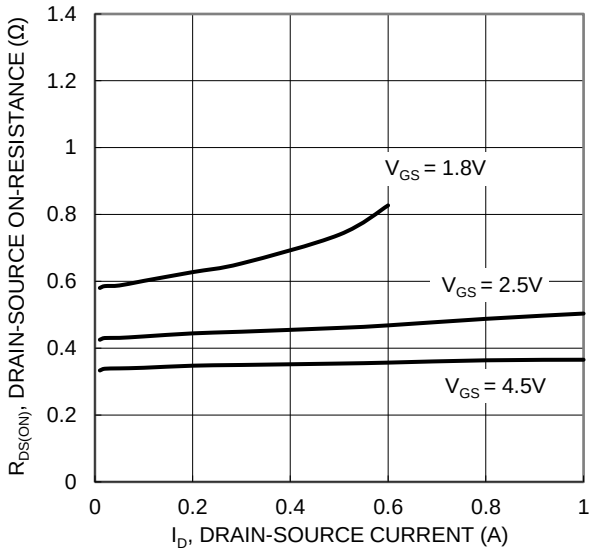



Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

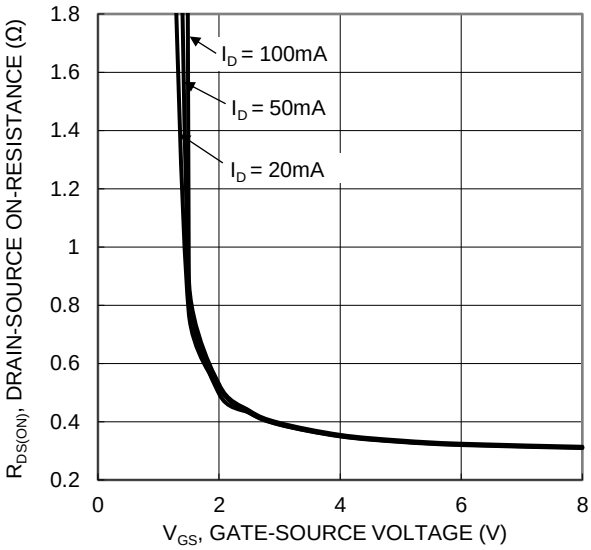



Figure 4. Typical Transfer Characteristic

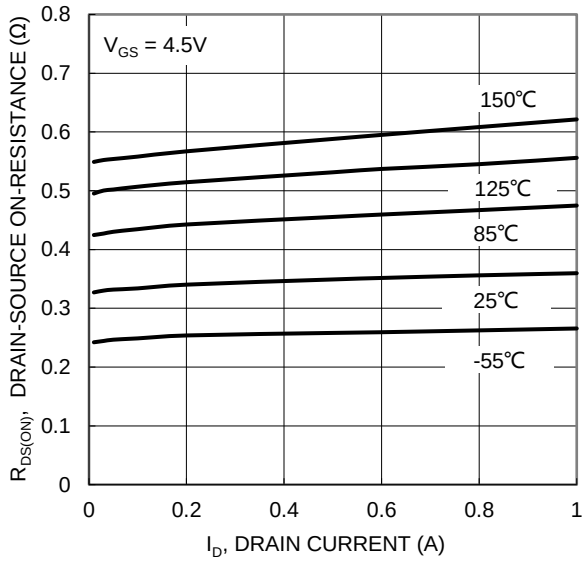



Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

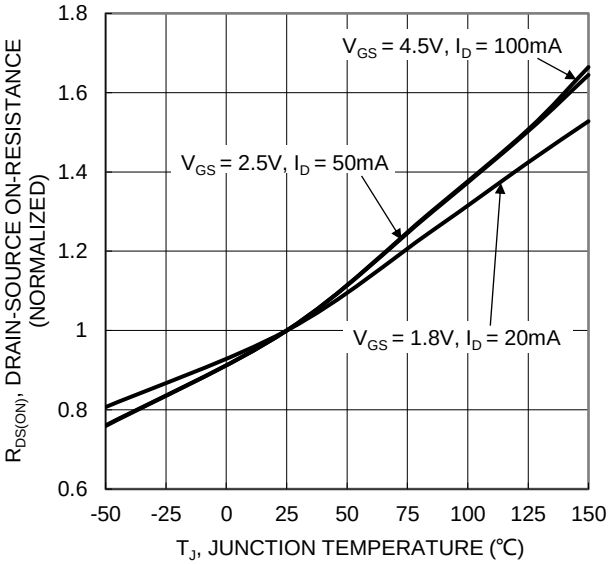



Figure 6. On-Resistance Variation with Junction Temperature


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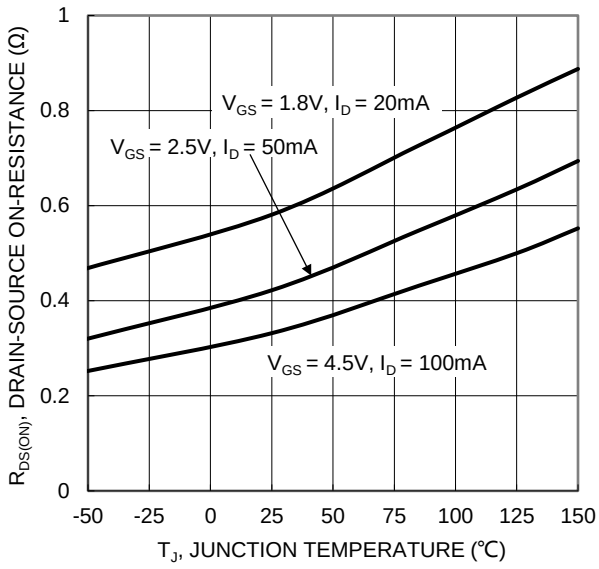



Figure 7. On-Resistance Variation with Junction Temperature

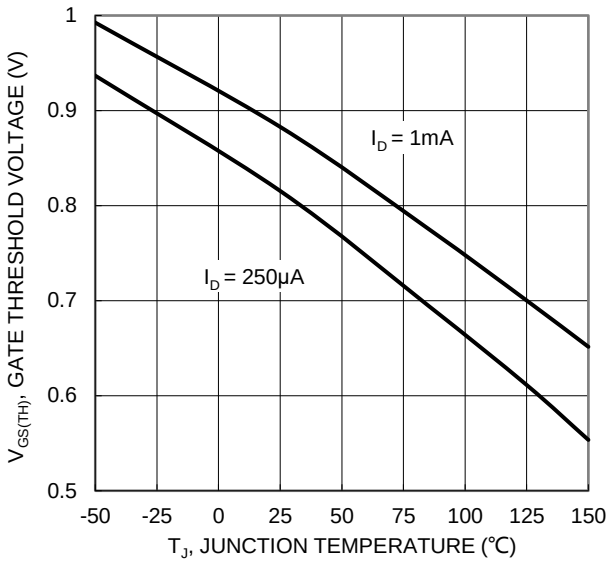



Figure 8. Gate Threshold Variation vs. Junction Temperature

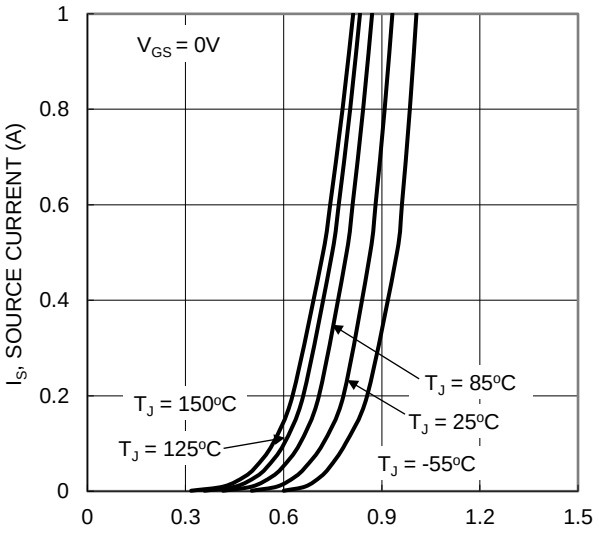



Figure 9. Diode Forward Voltage vs. Current

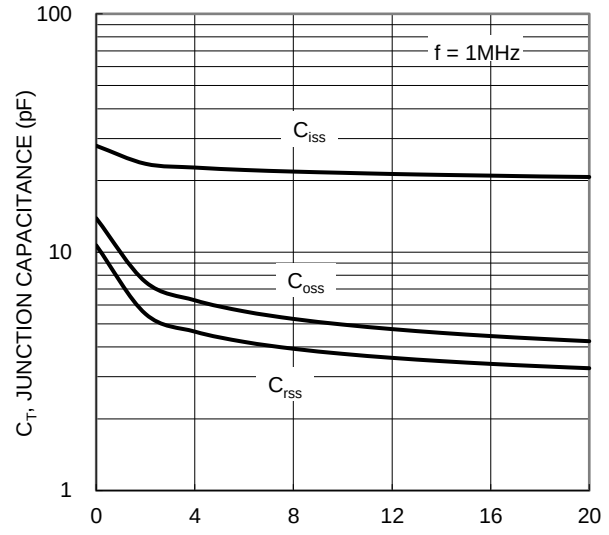



Figure 10. Typical Junction Capacitance

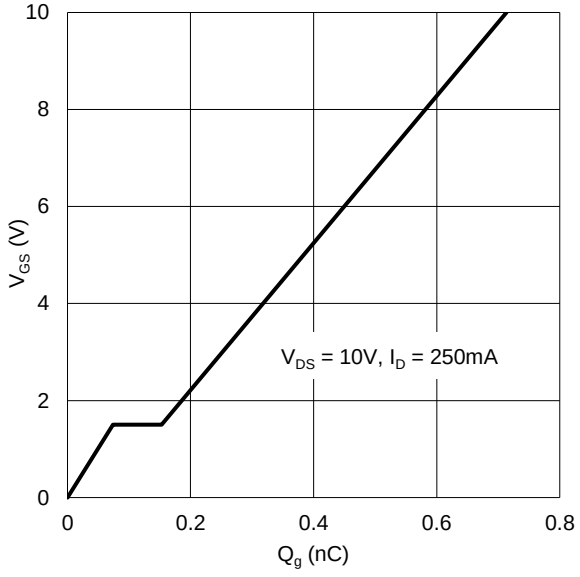



Figure 11. Gate Charge

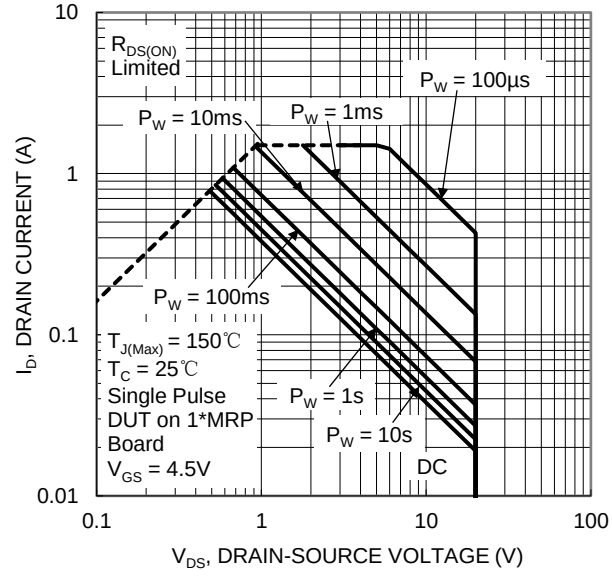



Figure 12. SOA, Safe Operation Area


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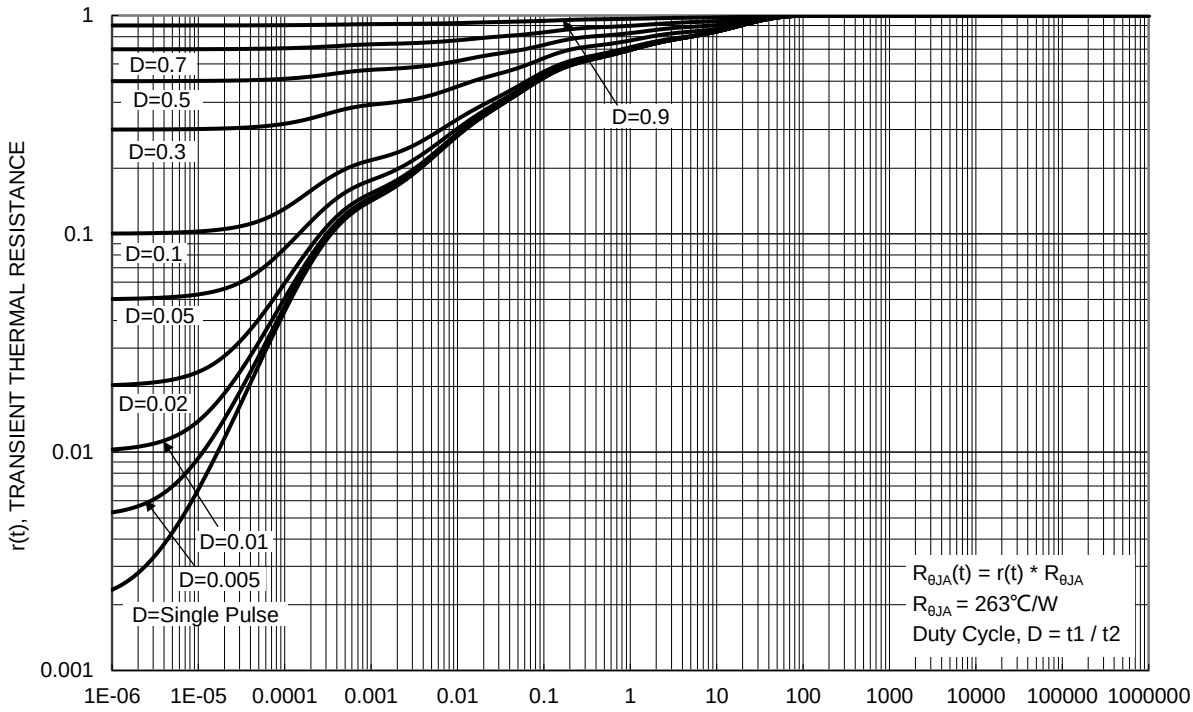


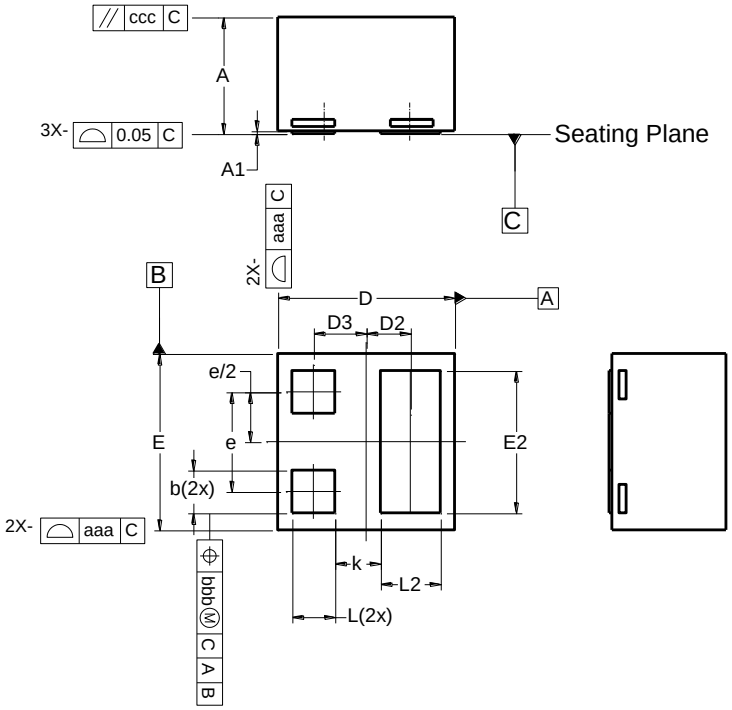

Figure 13. Transient Thermal Resistance


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## Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

**X2-DFN0606-3**

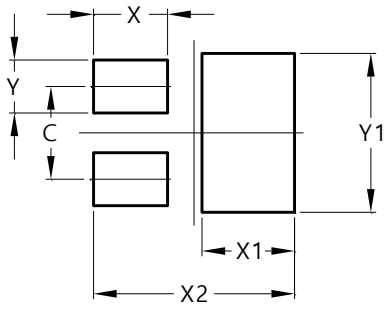



| X2-DFN0606-3 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 0.36 | 0.40 | 0.39 |
| **A1** | 0.00 | 0.05 | 0.02 |
| **b** | 0.10 | 0.20 | 0.15 |
| **D** | 0.57 | 0.67 | 0.62 |
| **D2** | 0.155 BSC | | |
| **D3** | 0.185 BSC | | |
| **E** | 0.57 | 0.67 | 0.62 |
| **E2** | 0.40 | 0.60 | 0.50 |
| **e** | 0.35 BSC | | |
| **k** | 0.16 REF | | |
| **L** | 0.10 | 0.20 | 0.15 |
| **L2** | 0.11 | 0.31 | 0.21 |
| **aaa** | 0.08 | | |
| **bbb** | 0.07 | | |
| **ccc** | 0.05 | | |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**X2-DFN0606-3**




| Dimensions | Value (in mm) |
|---|---|
| **C** | 0.350 |
| **X** | 0.280 |
| **X1** | 0.350 |
| **X2** | 0.760 |
| **Y** | 0.200 |
| **Y1** | 0.600 |


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