20V P-CHANNEL ENHANCEMENT MODE MOSFET
POWERDI®

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max T_A = +25°C
-20V	8mΩ @ V_{GS} = -4.5V	-14A
	9.8mΩ @ V_{GS} = -2.5V	-10A
	13mΩ @ V_{GS} = -1.8V	-9.3A
	17mΩ @ V_{GS} = -1.5V	-8.3A

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Load Switch
- Power Management Functions

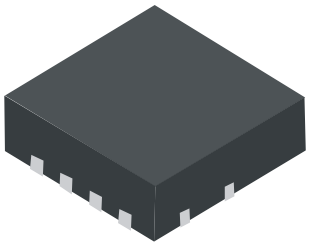
Features

- Low $R_{DS(ON)}$ – ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

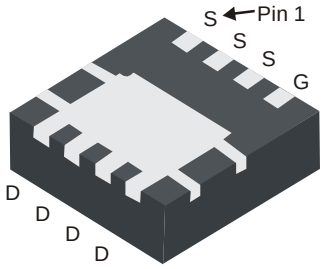
Mechanical Data

- Case: POWERDI3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (approximate)

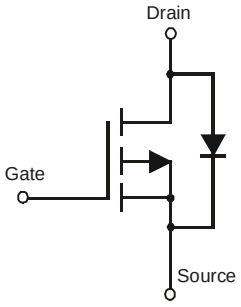
POWERDI3333-8



Top View



Bottom View



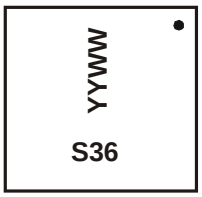
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2008UFG-7	POWERDI3333-8	2000/Tape & Reel
DMP2008UFG-13	POWERDI3333-8	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



S36 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last digit of year (ex: 11 = 2011)
WW = Week code (01 ~ 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage (Note 5)			V_{GSS}	±8	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C T_C = +25°C	I_D	-14 -11 -54	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I_{DM}	-80	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-2.2	A
Avalanche Current (Note 8)			I_{AS}	-15	A
Avalanche Energy (Note 8)			E_{AS}	-113	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.4	W
	T_C = +25°C		41	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	52	°C/W
	(Note 6)		137	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	3.0	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	—	8	mΩ	V_{GS} = -4.5V, I_D = -12A
		—	—	9.8		V_{GS} = -2.5V, I_D = -10A
		—	—	13		V_{GS} = -1.8V, I_D = -9.3A
		—	—	17		V_{GS} = -1.5V, I_D = -8.3A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	42	—	S	V_{DS} = -5V, I_D = -12A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	6909	—	pF	V_{DS} = -10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	635	—		
Reverse Transfer Capacitance	C_{rss}	—	563	—		
Gate Resistance	R_G	—	2.5	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	72	—	nC	V_{DD} = -10V, I_D = -12A
Total Gate Charge (V_{GS} = -2.5V)	Q_g	—	40	—		
Gate-Source Charge	Q_{gs}	—	8.6	—		
Gate-Drain Charge	Q_{gd}	—	14.5	—		
Turn-On Delay Time	$t_{D(on)}$	—	22	—	ns	V_{GS} = -4.5V, V_{DD} = -10V, R_G = 6Ω, I_D = -12A
Turn-On Rise Time	t_r	—	33	—		
Turn-Off Delay Time	$t_{D(off)}$	—	291	—		
Turn-Off Fall Time	t_f	—	124	—		
BODY DIODE CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	—	-0.7	—	V	V_{GS} = 0V, I_S = -12A
		—	-0.7	—	V	V_{GS} = 0V, I_S = -2A
Reverse Recovery Time (Note 10)	t_{rr}	—	25	—	ns	I_F = -12A, di/dt = 100A/µs
Reverse Recovery Charge (Note 10)	Q_{rr}	—	15	—	nC	I_F = -12A, di/dt = 100A/µs

Notes:
5. AEC-Q101 V_{GS} maximum is ±6.4V.
6. $R_{\theta JA}$ is determined with the device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
8. .UIS in production with L = 1mH, T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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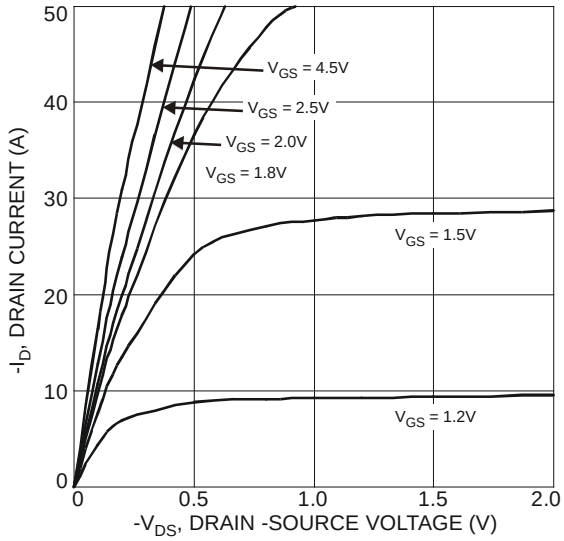


Fig. 1 Typical Output Characteristics

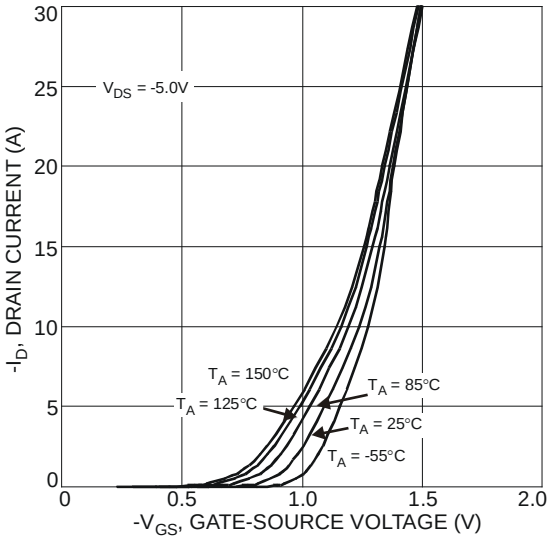


Fig. 2 Typical Transfer Characteristics

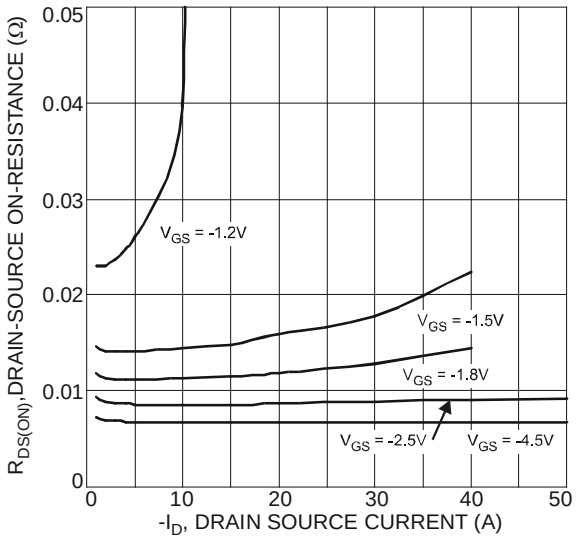


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

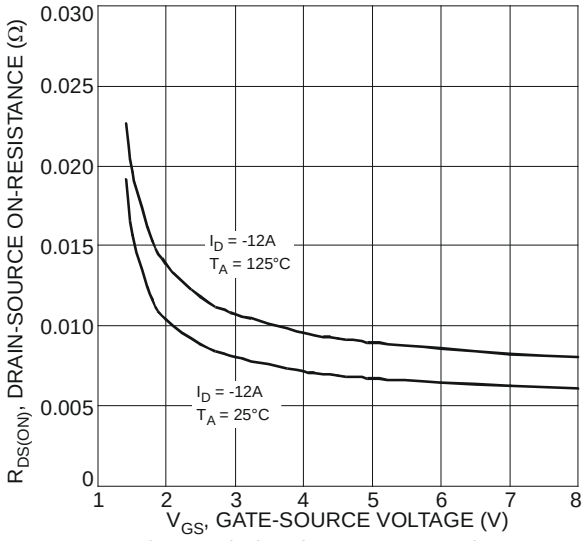


Fig. 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

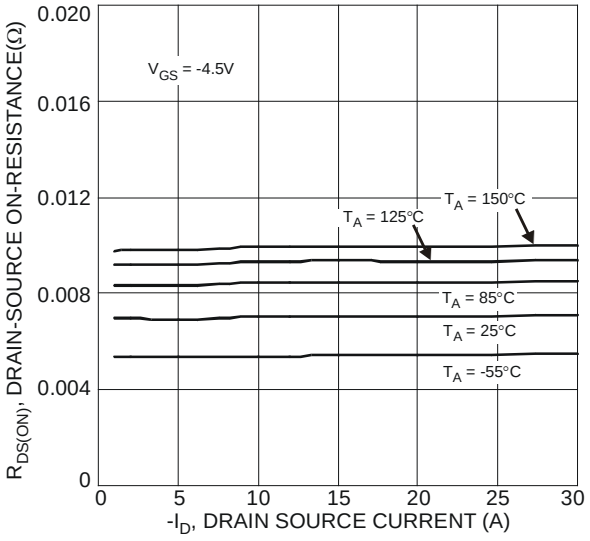


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

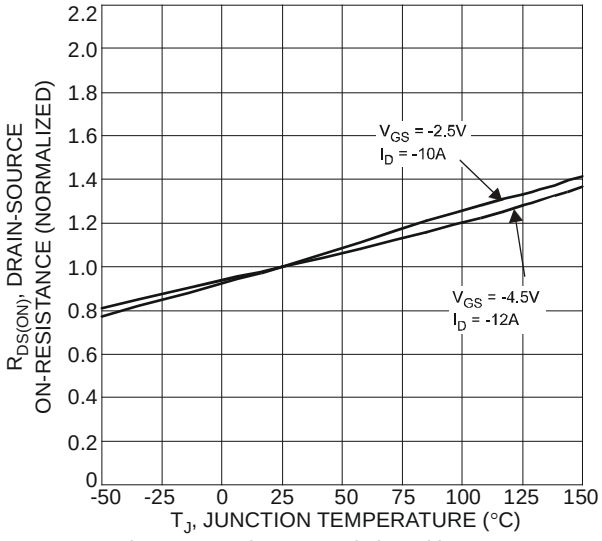


Fig. 6 On-Resistance Variation with Temperature

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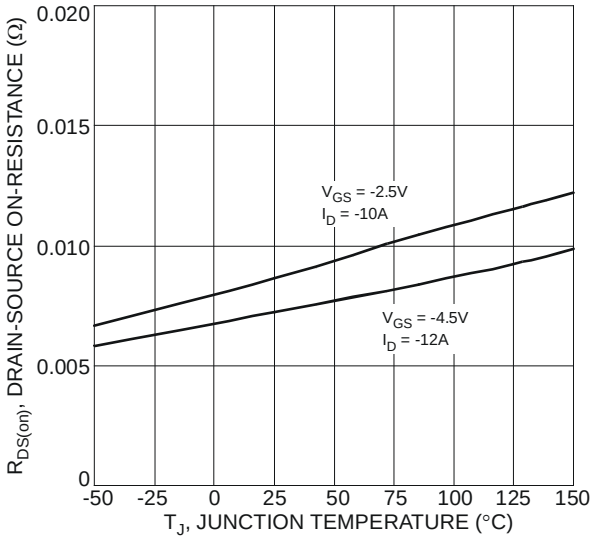


Fig. 7 On-Resistance Variation with Temperature

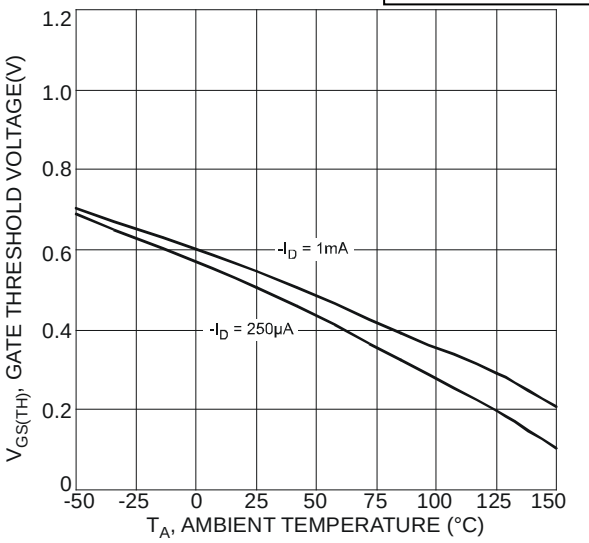


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

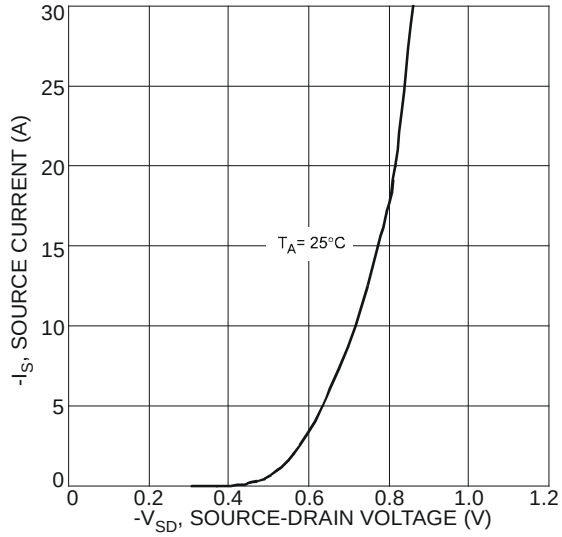


Fig. 9 Diode Forward Voltage vs. Current

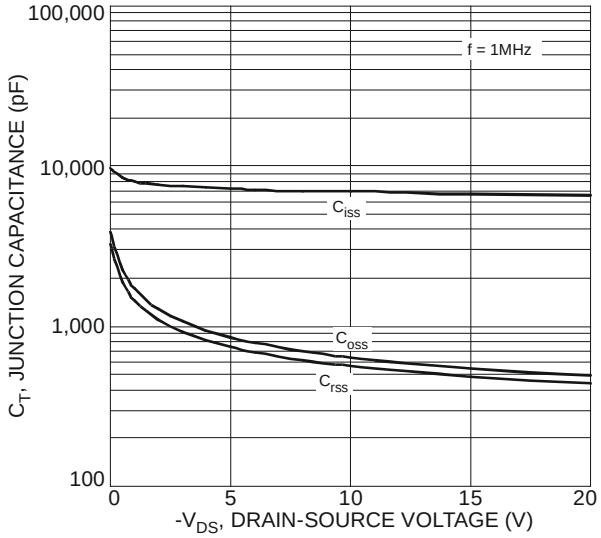


Fig. 10 Typical Junction Capacitance

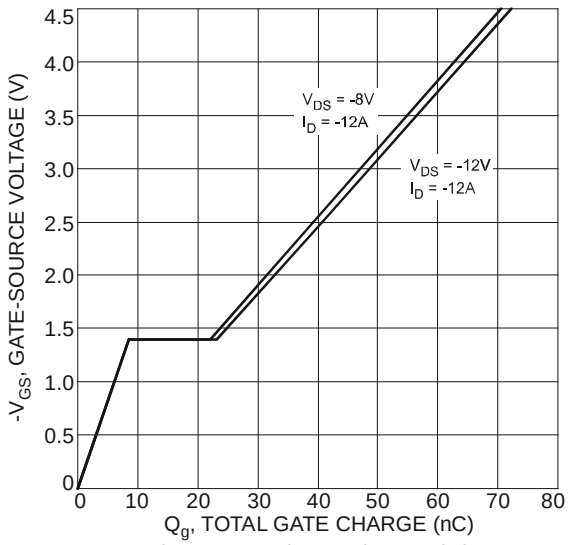


Fig. 11 Gate-Charge Characteristics

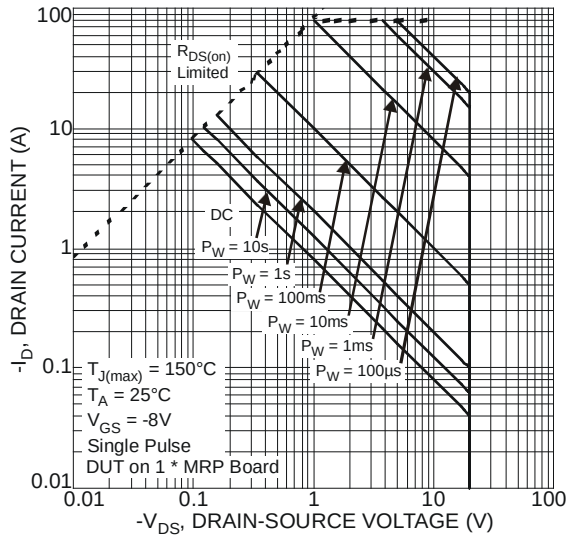


Fig. 12 SOA, Safe Operation Area

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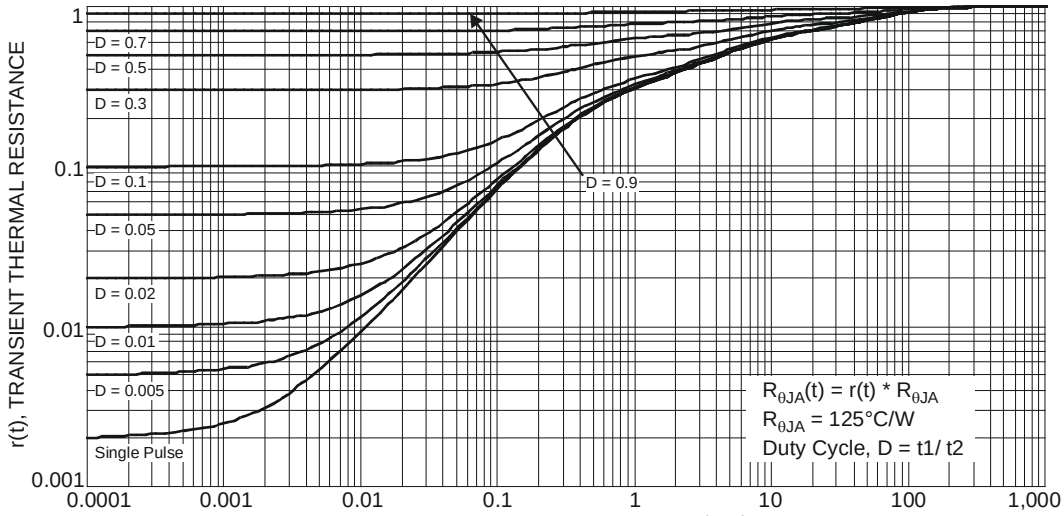
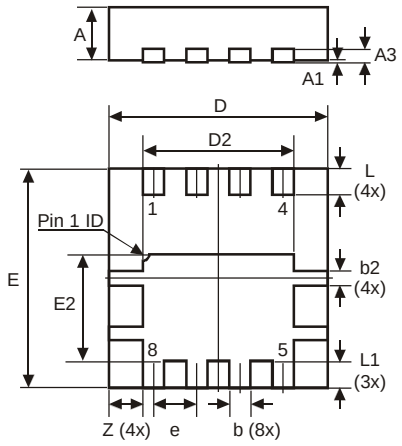


Fig. 13 Transient Thermal Resistance

Package Outline Dimensions

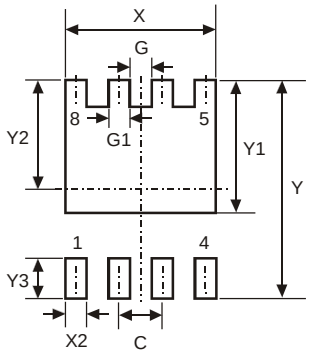
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



POWERDI3333-8			
Dim	**Min**	**Max**	**Typ**
D	3.25	3.35	3.30
E	3.25	3.35	3.30
D2	2.22	2.32	2.27
E2	1.56	1.66	1.61
A	0.75	0.85	0.80
A1	0	0.05	0.02
A3	–	–	0.203
b	0.27	0.37	0.32
b2	–	–	0.20
L	0.35	0.45	0.40
L1	–	–	0.39
e	–	–	0.65
Z	–	–	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.650
G	0.230
G1	0.420
Y	3.700
Y1	2.250
Y2	1.850
Y3	0.700
X	2.370
X2	0.420

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