THE DMP2100UQ IS NOT RECOMMENDED FOR NEW DESIGNS.
PLEASE USE THE DMP2070UQ.

Lead-free Green

DMP2100UQ

P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	Package	I_D T_A = +25°C
-20V	38mΩ @ V_{GS} = -10V	SOT23	-4.3A
	43mΩ @ V_{GS} = -4.5V		-4.0A
	75mΩ @ V_{GS} = -2.5V		-2.8A

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMP2100UQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Load switches
- Power-management functions
- Motor controls

Mechanical Data

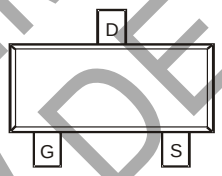
- Package: SOT23
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminals Connections: See Diagram Below
- Weight: 0.008 grams (Approximate)



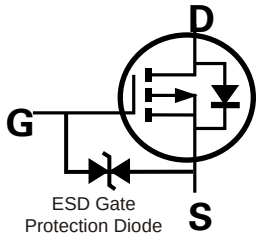
SOT23



Top View



Top View
Pin Configuration



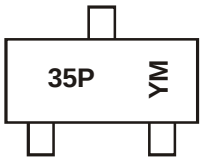
Equivalent Circuit
(Note 4)

Ordering Information (Note 5)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMP2100UQ-7	SOT23	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. The ESD gate protection diode is only designed to protect against ESD events. No gate-source voltage greater than the maximum V_{GSS} rating (given on page 2) can be applied.
5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



35P = Product Type Marking Code
YM or $\overline{Y}$M = Date Code Marking
Y or $\overline{Y}$ = Year (ex: L = 2024)
M = Month (ex: 9 = September)

Date Code Key

Year	2019	-	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	G	-	L	M	N	P	R	S	T	U	V	W

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage (Note 6)			V_{GSS}	±10	V
Continuous Drain Current (Note 8) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-4.3 -3.4	A
	t<5s	T_A = +25°C T_A = +70°C	I_D	-5.5 -4.3	A
Maximum Continuous Body Diodes Forward Current (Note 8)			I_S	-2	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-30	A
Pulsed Body Diodes Forward Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	-30	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 7)	T_A = +25°C	P_D	0.8	W
	T_A = +70°C		0.5	
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	161	°C/W
	t<5s		96	
Total Power Dissipation (Note 8)	T_A = +25°C	P_D	1.3	W
	T_A = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 8)	Steady State	$R_{\theta JA}$	99	°C/W
	t<5s		60	
Thermal Resistance, Junction to Case (Note 8)		$R_{\theta JC}$	15	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.3	—	-1.4	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	25	38	mΩ	V_{GS} = -10V, I_D = -3.5A
		—	29	43		V_{GS} = -4.5V, I_D = -3A
		—	37	75		V_{GS} = -2.5V, I_D = -1A
		—	47	—		V_{GS} = -1.8V, I_D = -0.5A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	3	—	S	V_{DS} = -5V, I_D = -4A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	216	—	pF	V_{DS} = -15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	90	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	24	—	pF	
Gate Resistance	R_g	—	250	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
SWITCHING CHARACTERISTICS (Note 10)						
Total Gate Charge	Q_g	—	9.1	—	nC	V_{GS} = -4.5V, V_{DS} = -10V I_D = -4A
Gate-Source Charge	Q_{gs}	—	1.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	80	—	ns	V_{DS} = -10V, V_{GS} = -4.5V, R_D = 2.5Ω, R_G = 3.0Ω
Turn-On Rise Time	t_R	—	155	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	688	—	ns	
Turn-Off Fall Time	t_F	—	423	—	ns	

Notes:
6. AEC-Q101 V_{GS} maximum is ±9.6V.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
8. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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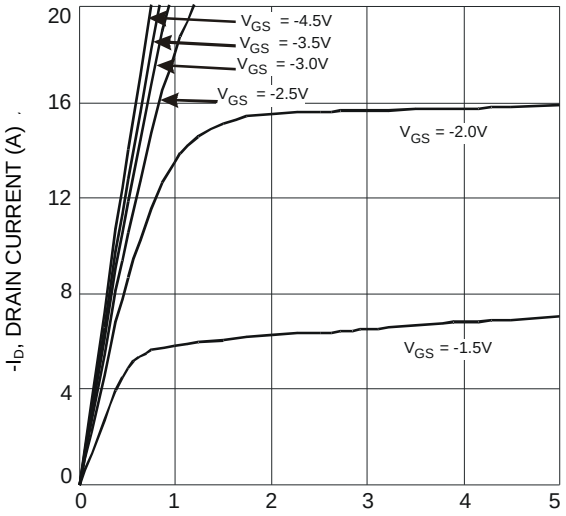


Fig. 1 Typical Output Characteristic

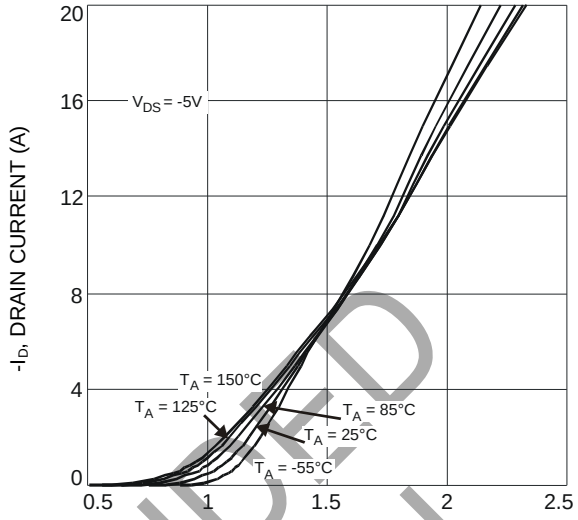


Fig. 2 Typical Transfer Characteristic

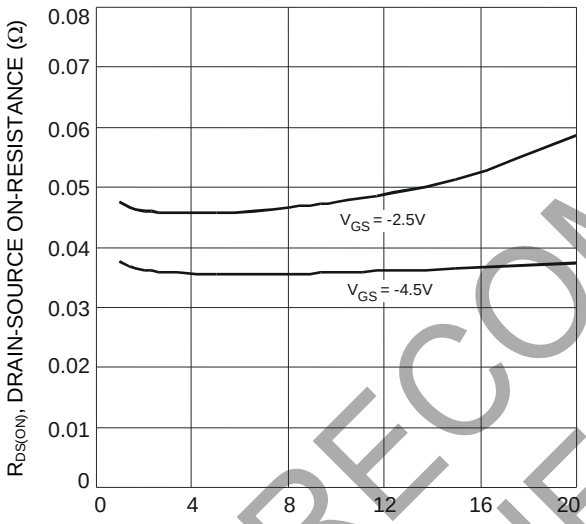


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

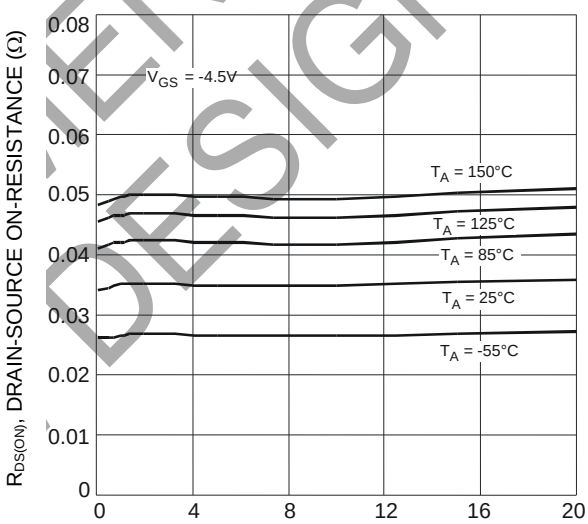


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

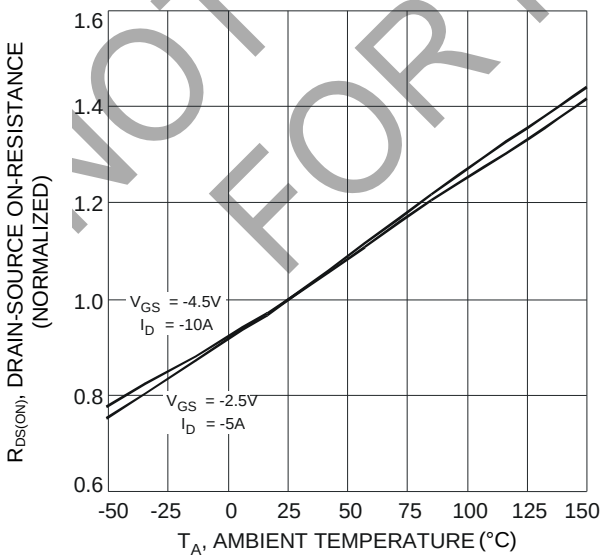


Fig. 5 On-Resistance Variation with Temperature

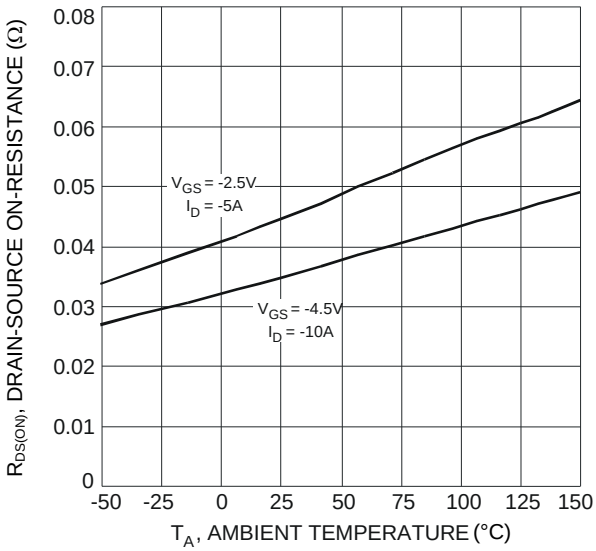


Fig. 6 On-Resistance Variation with Temperature

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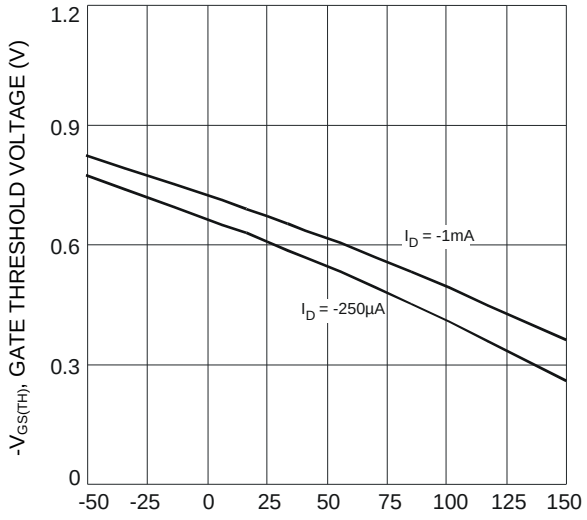


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

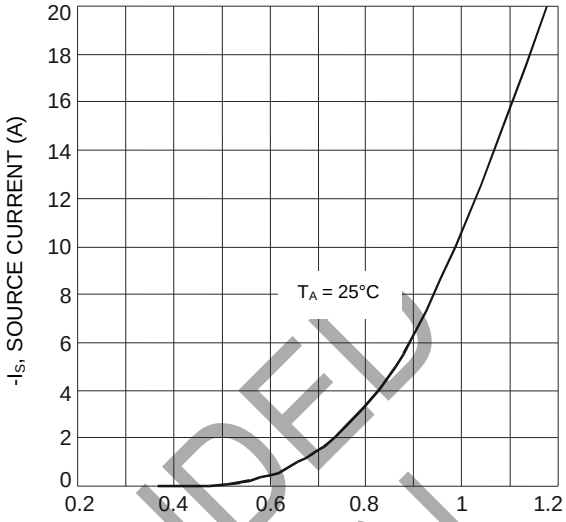


Fig. 8 Diode Forward Voltage vs. Current

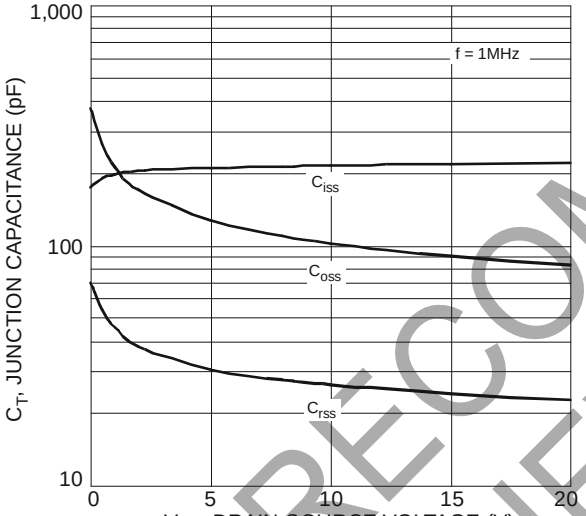


Fig. 9 Typical Junction Capacitance

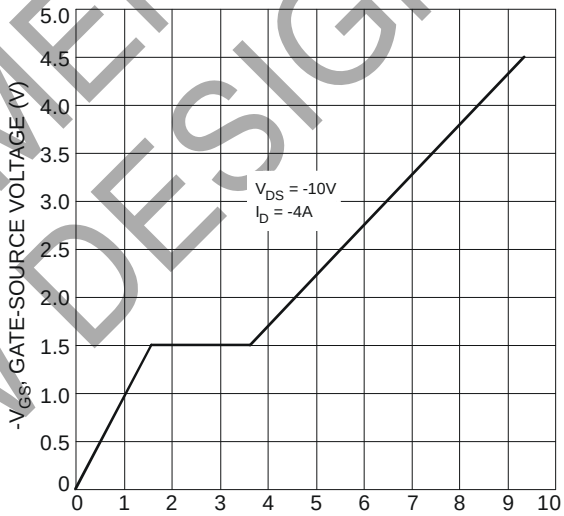


Fig. 10 Gate-Charge Characteristics

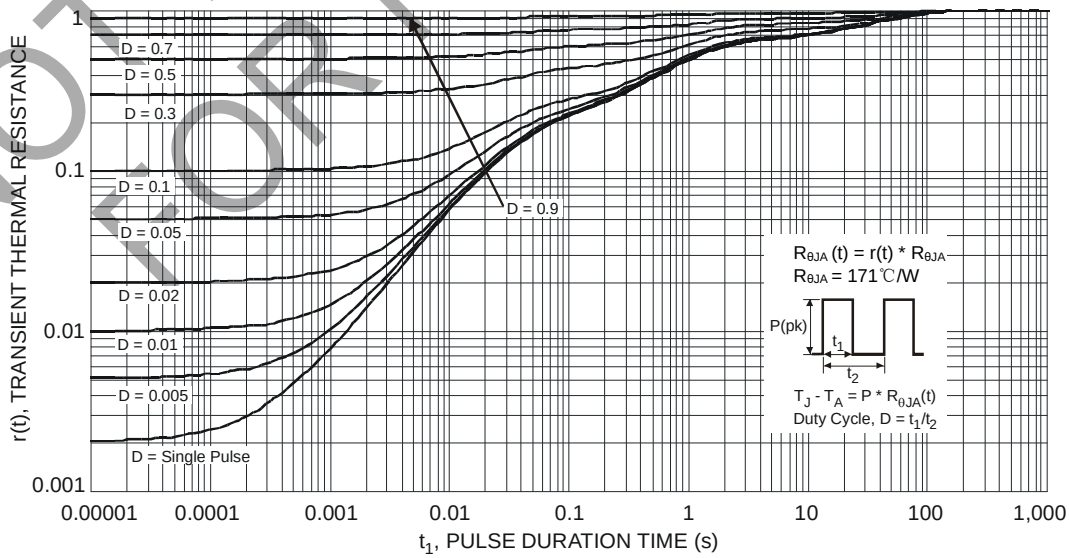


Fig. 11 Transient Thermal Response

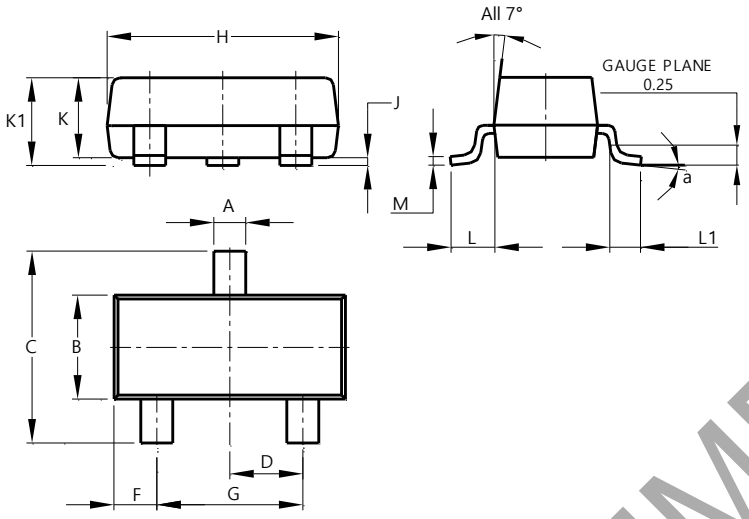
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Package Outline Dimensions

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SOT23



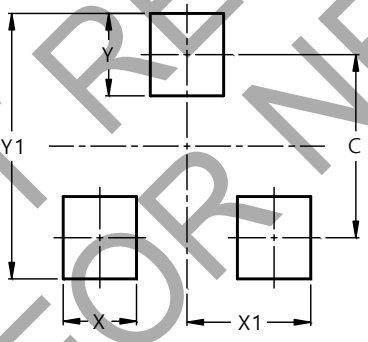
SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

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Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9

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