# DMP22D5UFO

## 20V P-CHANNEL ENHANCEMENT MODE MOSFET

## Product Summary

| $BV_{DSS}$ | $R_{DS(ON)}$ Max | $I_D$ Max $T_A$ = +25°C |
|---|---|---|
| -20V | 1.9Ω @ $V_{GS}$ = -4.5V | -0.53A |
| | 2.4Ω @ $V_{GS}$ = -2.5V | -0.46A |
| | 3.4Ω @ $V_{GS}$ = -1.8V | -0.38A |
| | 5.0Ω @ $V_{GS}$ = -1.5V | -0.31A |

## Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Features and Benefits

- Low Package Profile
- 0.6mm × 0.4mm Package Footprint
- Low On-Resistance
- Very Low Gate Threshold Voltage: -1.0V Max
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

## Applications

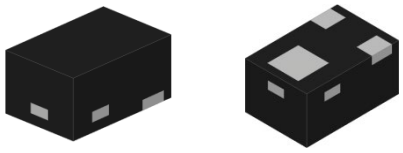
- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

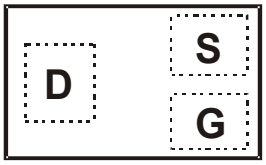
## Mechanical Data

- Case: X2-DFN0604-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.001 grams (Approximate)

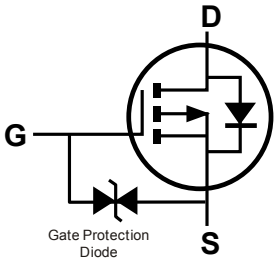
X2-DFN0604-3






Top View
Package Pin Configuration



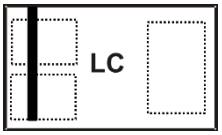

Equivalent Circuit

## Ordering Information (Note 4)

| Part Number | Case | Packaging |
|---|---|---|
| DMP22D5UFO-7B | X2-DFN0604-3 | 10,000/Tape & Reel |

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## Marking Information




Top View
Bar Denotes Gate and Source Side

LC = Product Type Marking Code


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## Maximum Ratings (@ $T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DSS}$ | -20 | V |
| Gate-Source Voltage | | | $V_{GSS}$ | ±8 | V |
| Continuous Drain Current (Note 5) $V_{GS}$ = -4.5V | Steady State | $T_A$ = +25°C<br>$T_A$ = +85°C | $I_D$ | -0.53<br>-0.38 | A |
| Pulsed Drain Current (Note 6) | | | $I_{DM}$ | -0.6 | A |

## Thermal Characteristics (@ $T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Total Power Dissipation (Note 5) | Steady State | $P_D$ | 0.77 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | Steady State | $R_{\theta JA}$ | 163 | °C/W |
| Total Power Dissipation (Note 6) | Steady State | $P_D$ | 0.34 | W |
| Thermal Resistance, Junction to Ambient (Note 6) | Steady State | $R_{\theta JA}$ | 368 | °C/W |
| Operating and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +150 | °C |

## Electrical Characteristics (@ $T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 7) | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | -20 | — | — | V | $V_{GS}$ = 0V, $I_D$ = -250µA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | -1 | µA | $V_{DS}$ = -16V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±5V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS** (Note 7) | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | -0.4 | — | -1.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | — | 0.95 | 1.9 | Ω | $V_{GS}$ = -4.5V, $I_D$ = -100mA |
| | | — | 1.2 | 2.4 | | $V_{GS}$ = -2.5V, $I_D$ = -50mA |
| | | — | 1.4 | 3.4 | | $V_{GS}$ = -1.8V, $I_D$ = -20mA |
| | | — | 1.7 | 5.0 | | $V_{GS}$ = -1.5V, $I_D$ = -10mA |
| Diode Forward Voltage | $V_{SD}$ | — | -0.5 | -1.1 | V | $V_{GS}$ = 0V, $I_S$ = -10mA |
| **DYNAMIC CHARACTERISTICS** (Note 8) | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 17 | — | pF | $V_{DS}$ = -16V, $V_{GS}$ = 0V, f = 1.0MHz |
| Output Capacitance | $C_{oss}$ | — | 4.1 | — | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 2.7 | — | pF | |
| Gate Resistance | $R_g$ | — | 3.3 | — | kΩ | $V_{DS}$ = 0V, $V_{GS}$ = 0V, f = 1.0MHz |
| Total Gate Charge | $Q_g$ | — | 0.3 | — | nC | $V_{GS}$ = -4.5V, $V_{DS}$ = -10V, $I_D$ = -250mA |
| Gate-Source Charge | $Q_{gs}$ | — | 0.04 | — | nC | |
| Gate-Drain Charge | $Q_{gd}$ | — | 0.1 | — | nC | |
| Turn-On Delay Time | $t_{D(ON)}$ | — | 7.3 | — | ns | $V_{DD}$ = -15V, $V_{GS}$ = -4.5V, $R_G$ = 2Ω, $I_D$ = -200mA |
| Turn-On Rise Time | $t_R$ | — | 20.7 | — | ns | |
| Turn-Off Delay Time | $t_{D(OFF)}$ | — | 185 | — | ns | |
| Turn-Off Fall Time | $t_F$ | — | 97 | — | ns | |

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided. 10µs pulse duty cycle = 1%.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.


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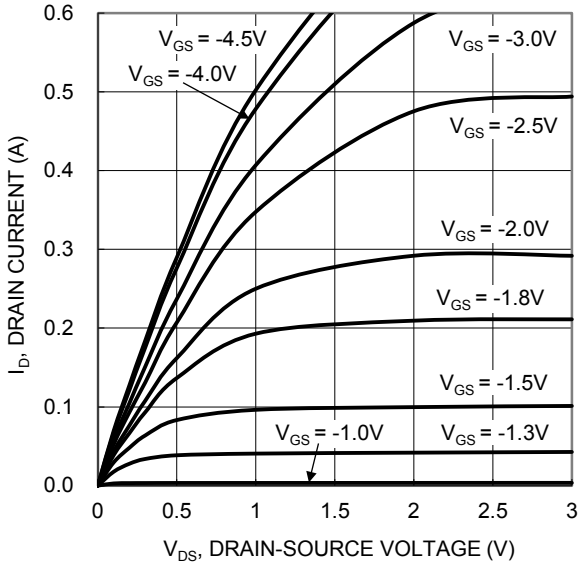



Figure 1. Typical Output Characteristic

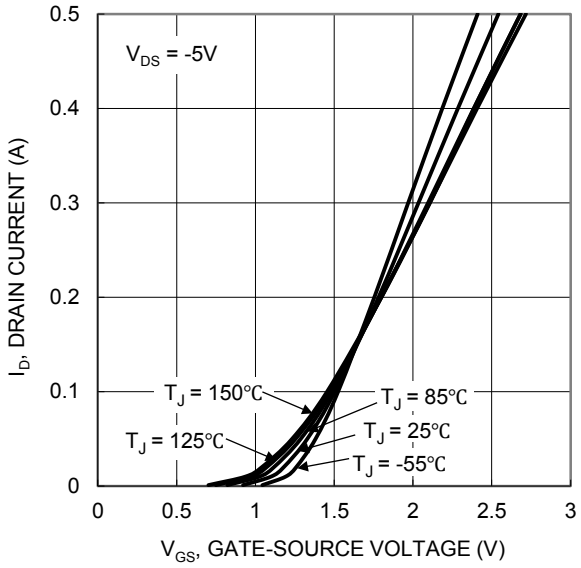



Figure 2. Typical Transfer Characteristic

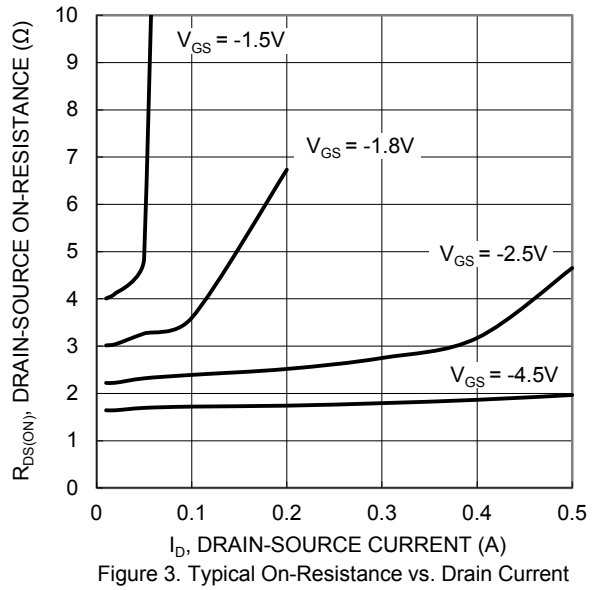



Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

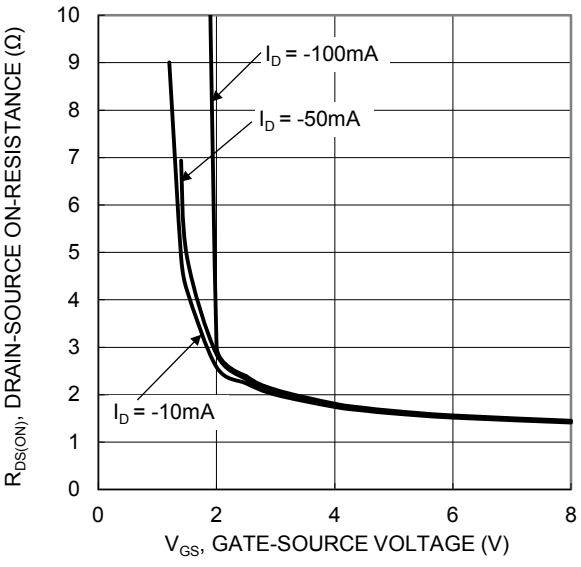



Figure 4. Typical Transfer Characteristic

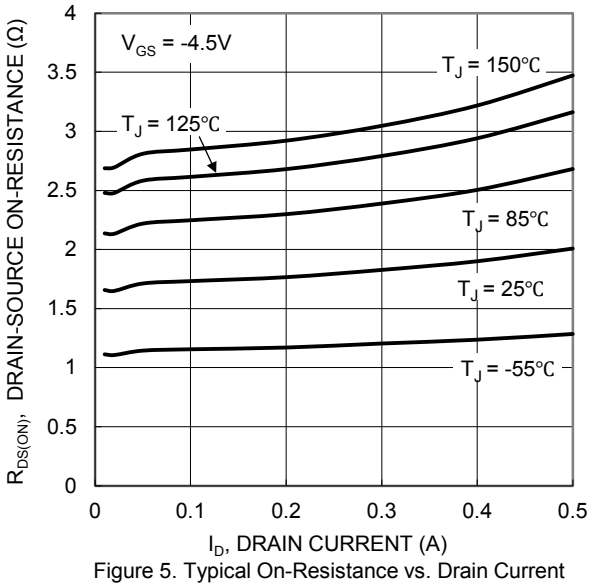



Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

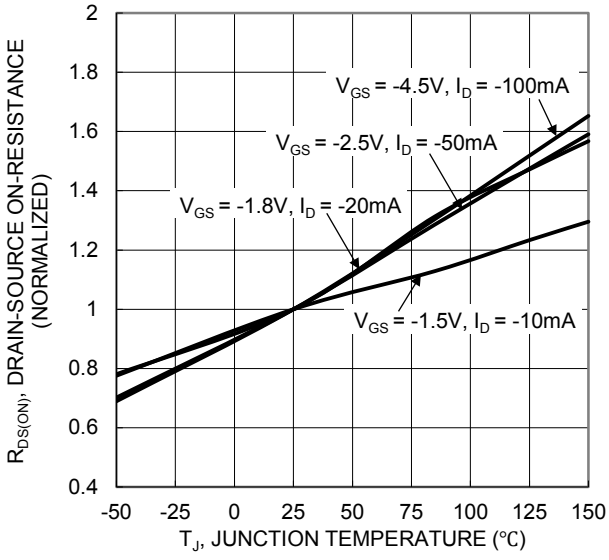



Figure 6. On-Resistance Variation with Junction Temperature


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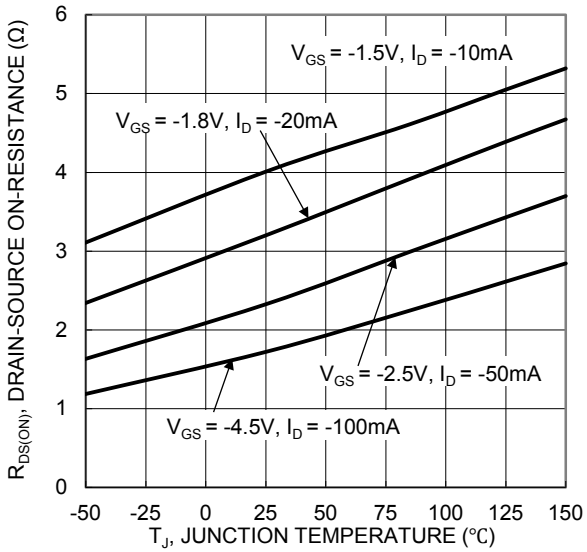



Figure 7. On-Resistance Variation with Junction Temperature

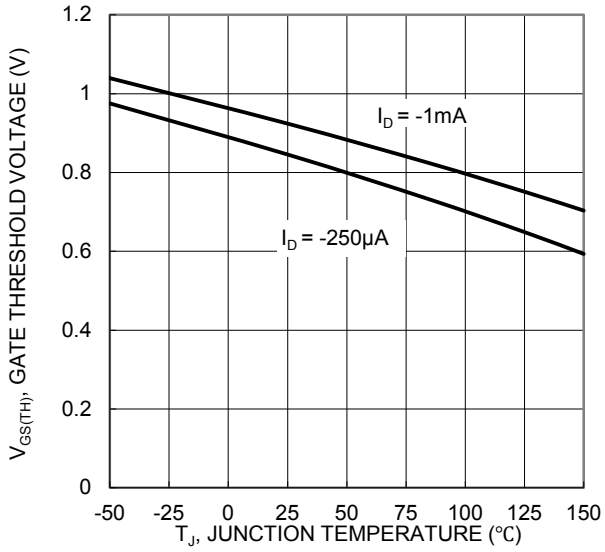



Figure 8. Gate Threshold Variation vs. Junction Temperature

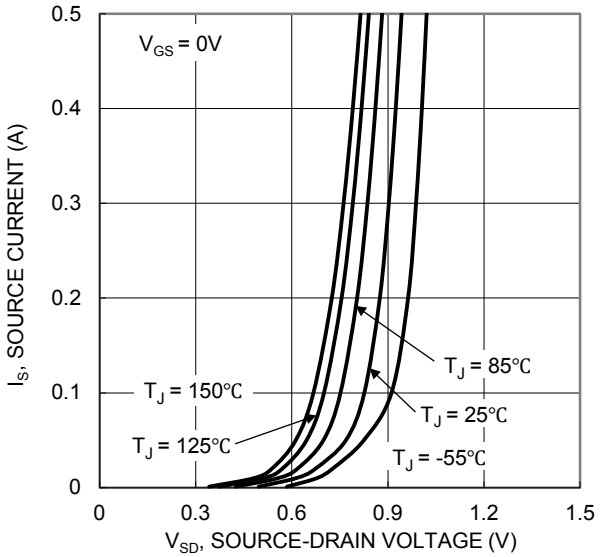



Figure 9. Diode Forward Voltage vs. Current

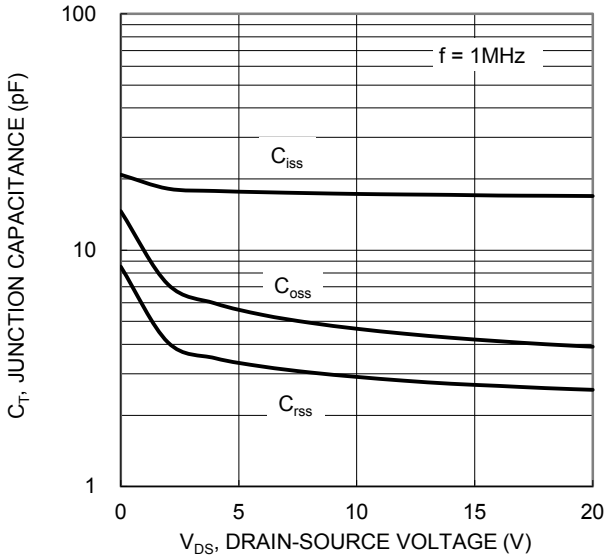



Figure 10. Typical Junction Capacitance

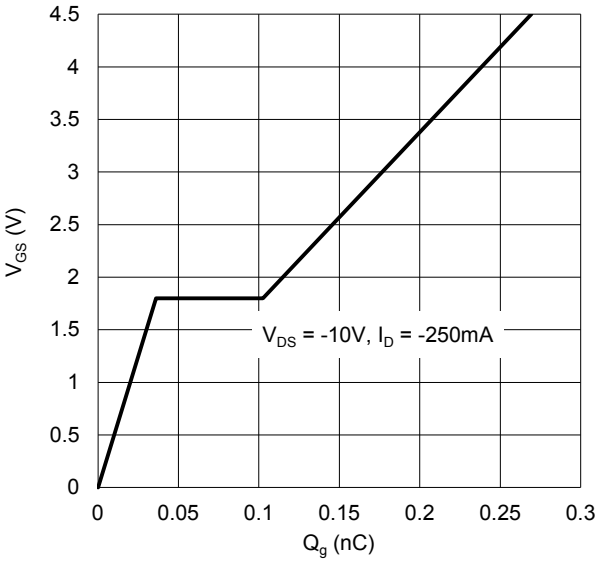



Figure 11. Gate Charge

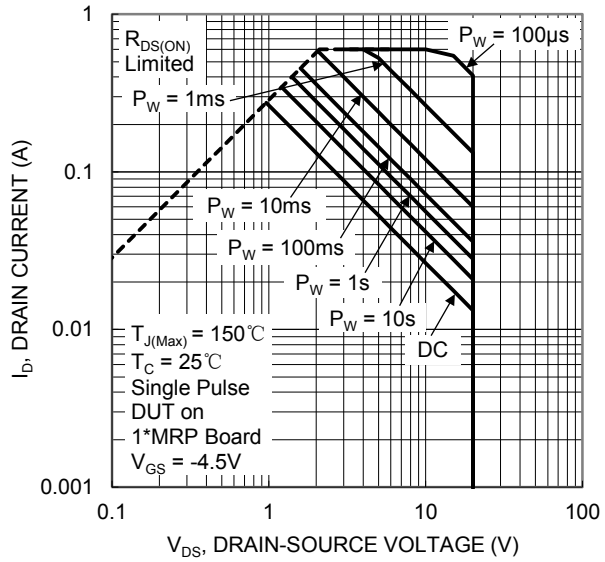



Figure 12. SOA, Safe Operation Area


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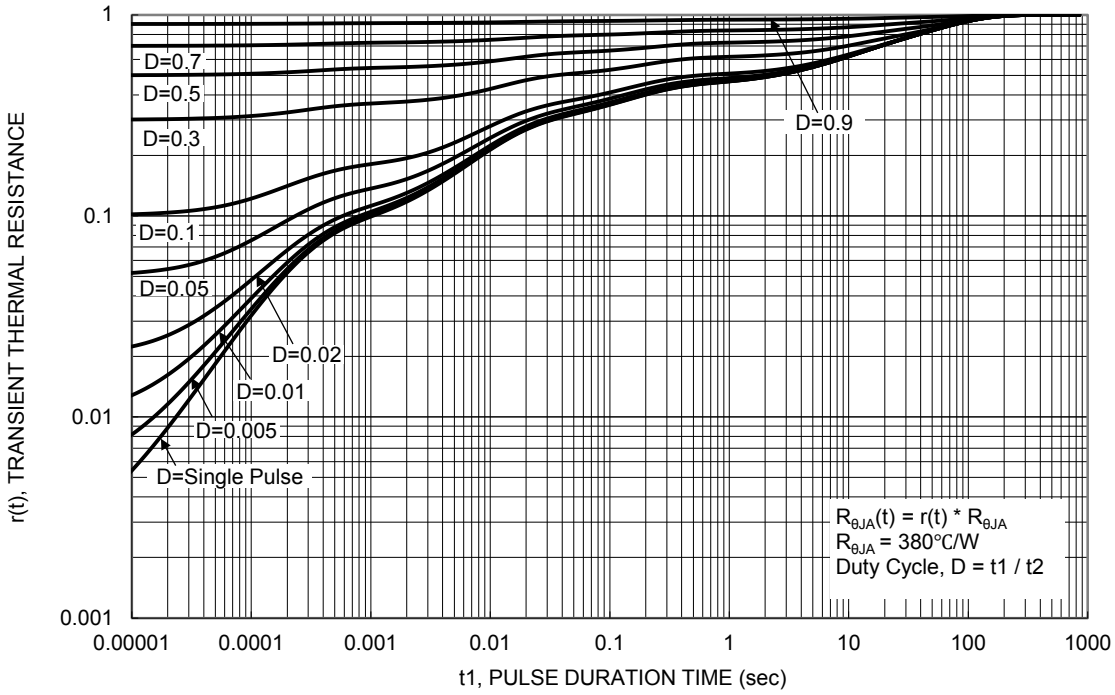
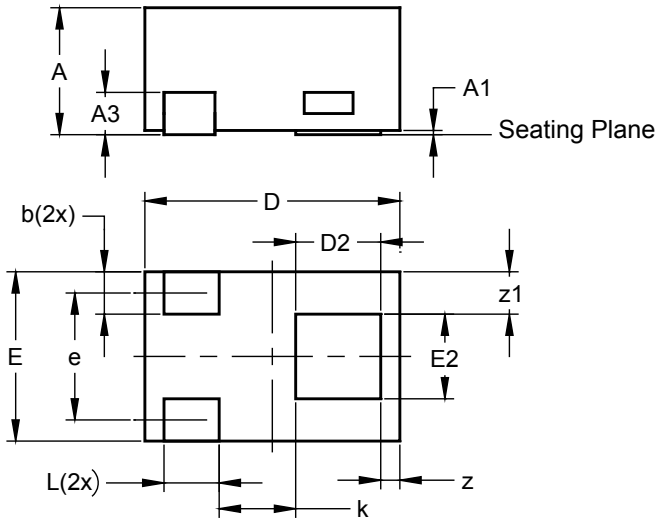



Figure 13. Transient Thermal Resistance


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## Package Outline Dimensions

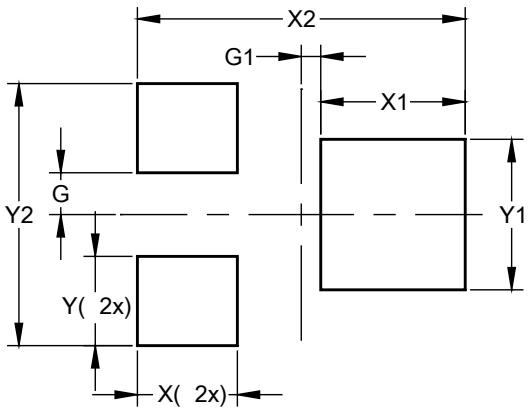
Please see http://www.diodes.com/package-outlines.html for the latest version.




| X2-DFN0604-3 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | -- | 0.40 | 0.36 |
| **A1** | 0.00 | 0.03 | 0.02 |
| **A3** | -- | -- | 0.10 |
| **b** | 0.07 | 0.15 | 0.10 |
| **D** | 0.55 | 0.65 | 0.60 |
| **D2** | 0.15 | 0.25 | 0.20 |
| **E** | 0.35 | 0.45 | 0.40 |
| **E2** | 0.15 | 0.25 | 0.20 |
| **e** | -- | -- | 0.30 |
| **k** | 0.15 | -- | -- |
| **L** | 0.10 | 0.18 | 0.13 |
| **z** | -- | -- | 0.045 |
| **z1** | -- | -- | 0.10 |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.




| Dimensions | Value (in mm) |
|---|---|
| **G** | 0.075 |
| **G1** | 0.035 |
| **X** | 0.180 |
| **X1** | 0.260 |
| **X2** | 0.590 |
| **Y** | 0.160 |
| **Y1** | 0.270 |
| **Y2** | 0.470 |


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