250V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
-250V	14Ω @ V_{GS} = -10V	-0.26A
	18Ω @ V_{GS} = -3.5V	-0.23A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- General Purpose Interfacing Switch
- Load Switching
- Battery Management Application
- Power Management Functions

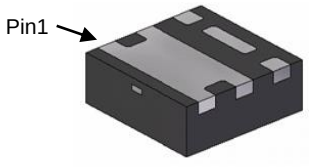
Features and Benefits

- 0.6mm Profile – Ideal for Low-Profile Applications
- PCB Footprint of 4mm^2
- Low Gate Threshold Voltage
- Low On-Resistance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

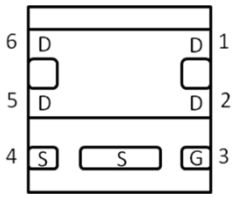
Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0065 grams (Approximate)

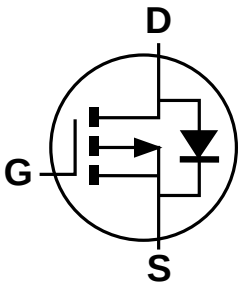
U-DFN2020-6 (Type E)



Bottom View



Pin Out
Bottom View



Equivalent Circuit

Ordering Information (Note 4)

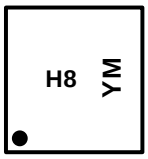
Part Number	Marking	Reel Size (inches)	Quantity per Reel
DMP25H18DLFDE-7	H8	7	3,000
DMP25H18DLFDE-13	H8	13	10,000

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information

Site 1



H8 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Date Code Key

Year	2014	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	B	…	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2



H8 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2014	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	4	…	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-250	V
Gate-Source Voltage			V_{GSS}	±40	V
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-0.26 -0.21	A
Pulsed Drain Current (10µs Pulse, Duty Cycle ≦1%)			I_{DM}	-1.0	A
Maximum Body Diode Continuous Current (Note 6)			I_S	-0.26	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation	(Note 5)	P_D	0.6	W
	(Note 6)		1.4	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	191	°C/W
	(Note 6)		86	
Thermal Resistance, Junction to Case	(Note 6)	$R_{\theta JC}$	17	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-250	—	—	V	V_{GS} = 0V, I_D = -1mA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -250V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±40V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.5	-1.7	-2.5	V	V_{DS} = V_{GS}, I_D = -1mA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	10	14	Ω	V_{GS} = -10V, I_D = -200mA
			13	18		V_{GS} = -3.5V, I_D = -100mA
Diode Forward Voltage	V_{SD}	—	-0.8	-1.2	V	V_{GS} = 0V, I_S = -200mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	81	—	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	14	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	4	—	pF	
Gate Resistance	R_g	—	13	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -10V)	Q_g	—	2.8	—	nC	V_{DS} = -25V, I_D = -200mA
Gate-Source Charge	Q_{gs}	—	0.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.6	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	7.5	—	ns	V_{DS} = -30V, I_D = -200mA, V_{GS} = -10V, R_G = 50Ω
Turn-On Rise Time	t_R	—	25	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	124	—	ns	
Turn-Off Fall Time	t_F	—	95	—	ns	
Reverse Recovery Time	t_{RR}	—	85	—	ns	I_F = -1.0A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	294	—	µC	

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

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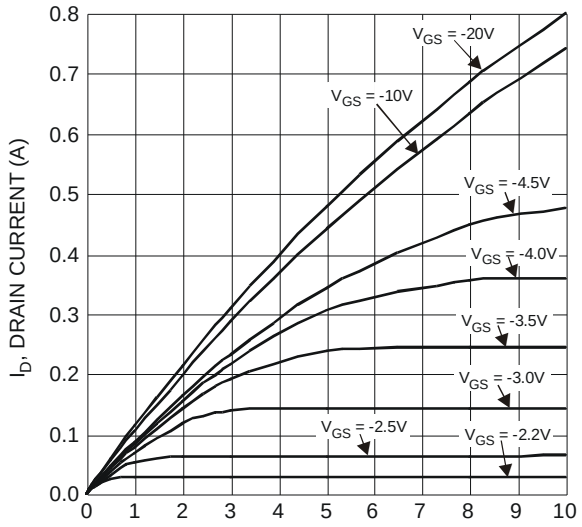


Figure 1 Typical Output Characteristics

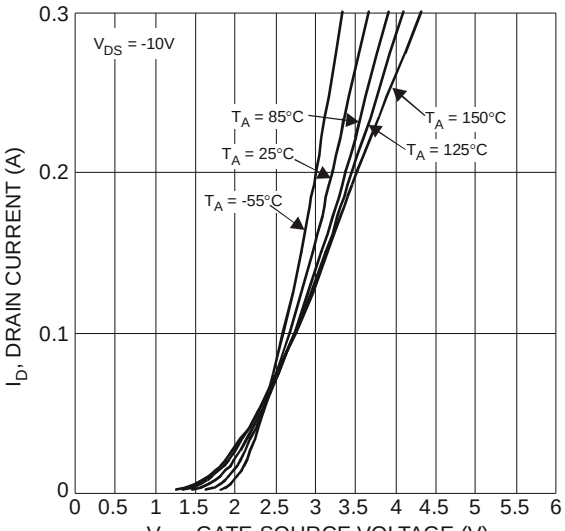


Figure 2 Typical Transfer Characteristics

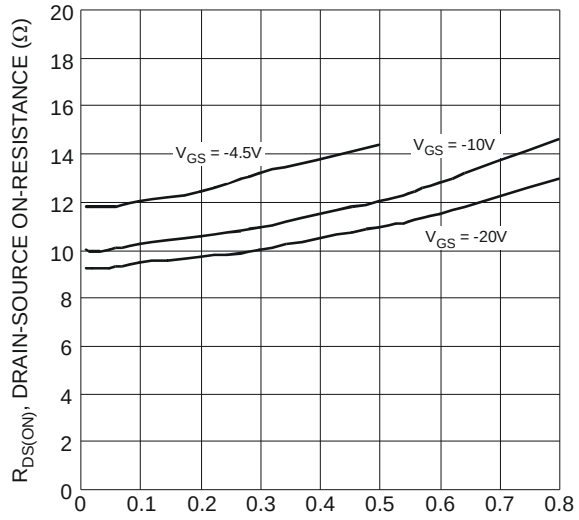


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

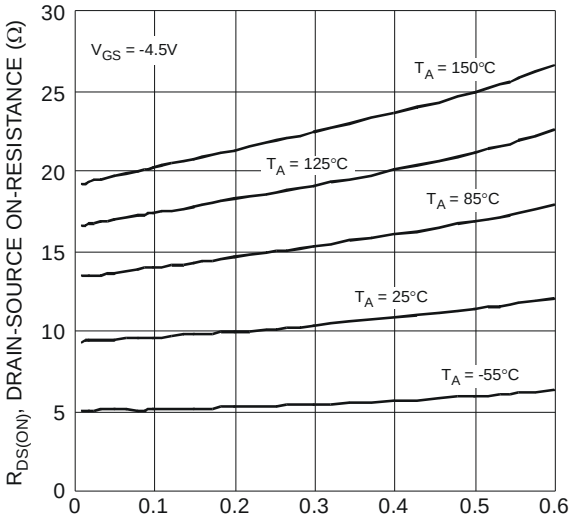


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

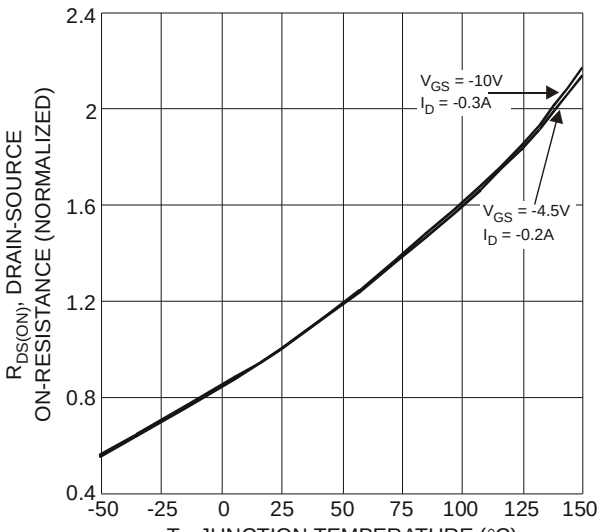


Figure 5 On-Resistance Variation with Temperature

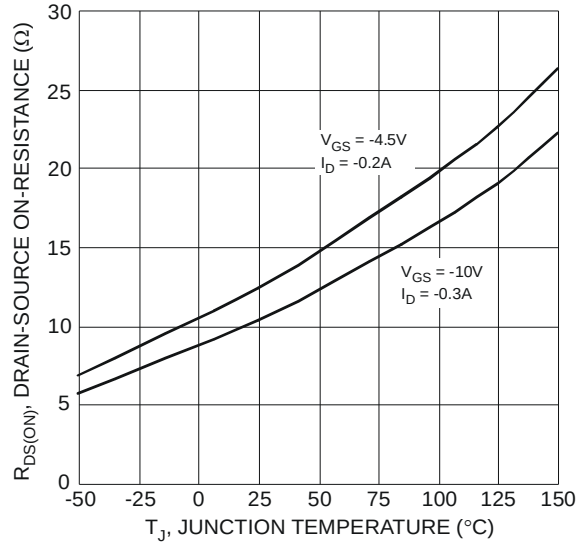


Figure 6 On-Resistance Variation with Temperature

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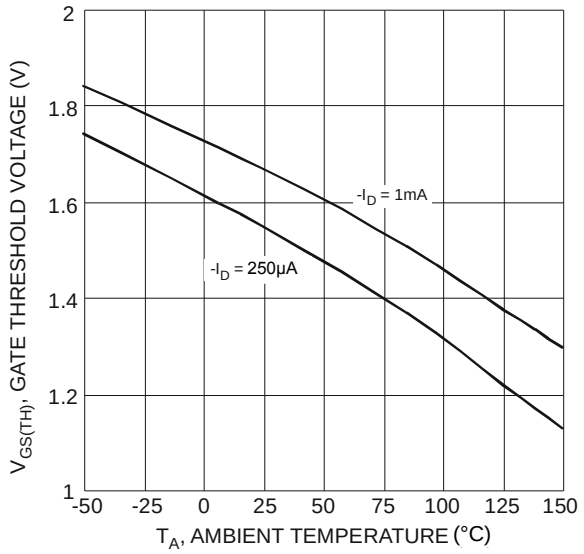


Figure 7 Gate Threshold Variation vs. Ambient Temperature

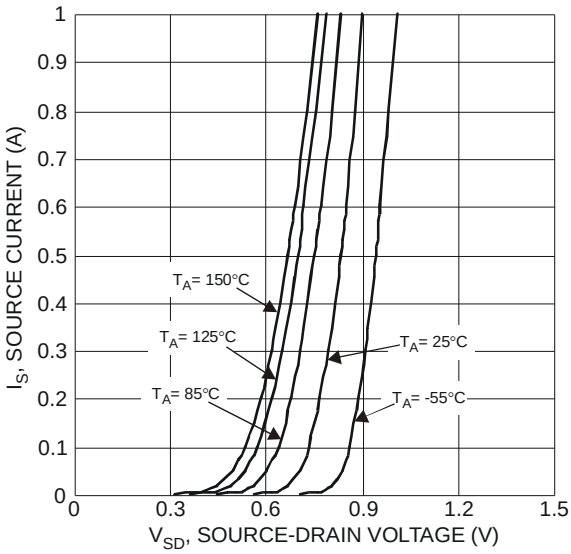


Figure 8 Diode Forward Voltage vs. Current

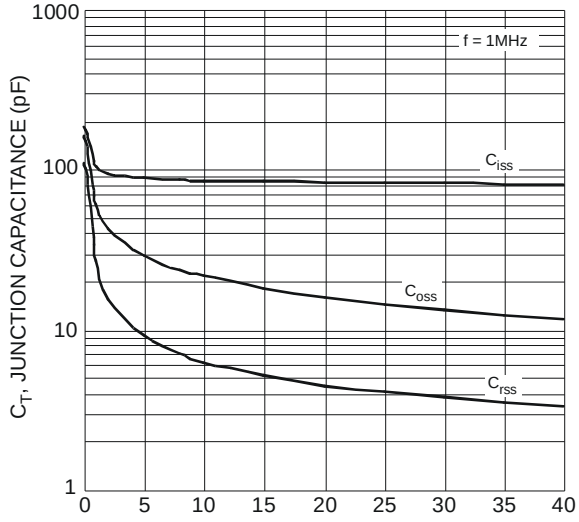


Figure 9 Typical Junction Capacitance

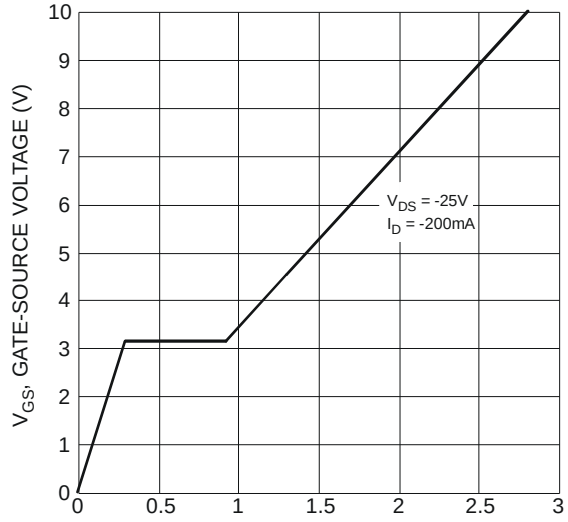


Figure 10 Gate-Charge Characteristics

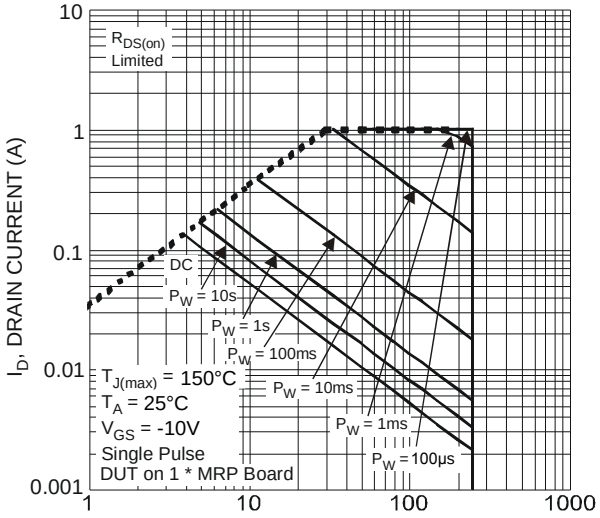


Figure 11 SOA, Safe Operation Area

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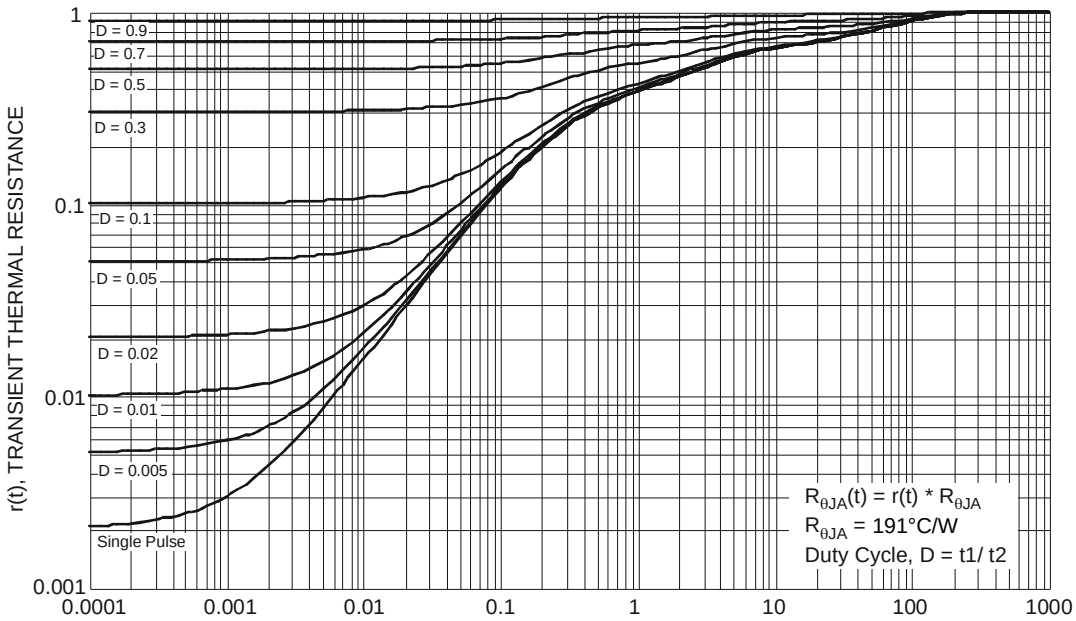


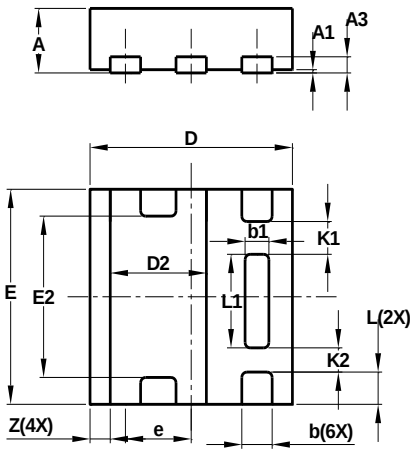
Figure 12 Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)

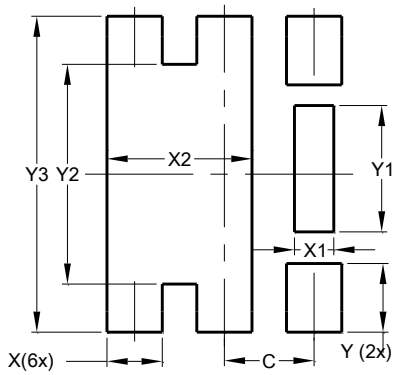


U-DFN2020-6 Type E			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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