115V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	BV_{DSS}@ $T_{J\ Max}$	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
115V	120V	85mΩ @ V_{GS} = 4.5V	3.5A
		90mΩ @ V_{GS} = 2.5V	3.4A

Features and Benefits

- Low Q_g & Q_{gd}
- Small Footprint 1.5mm × 1.5mm
- ESD Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), making it ideal for high-efficiency power-management applications.

- Battery management
- Load switches
- Battery protections

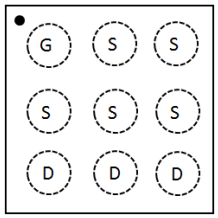
Mechanical Data

- Package: X4-DSN1515-9
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- UBM Size: 250µm
- Terminal Material: Finish – NiAu. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0006 grams (Approximate)

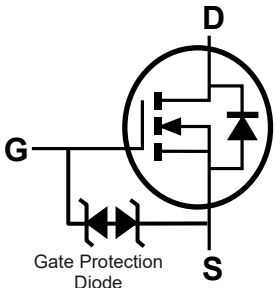


ESD PROTECTED

X4-DSN1515-9



Top View
Pin Configuration



Equivalent Circuit

Ordering Information (Notes 4 & 5)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMT12H060LCA9-7	X4-DSN1515-9	3000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Device with exposed silicon sidewall is non-isolated area.
5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



6A = Product Type Marking Code
YW = Date Code Marking
$\overline{Y}$ = Year (ex: 6 = 2026)
W = Week (ex: a =week 27; z represents week 52 and 53)

Date Code Key

Year	2022	-	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Code	2	-	6	7	8	9	0	1	2	3	4	5

Week	1-26	27-52	53
Code	A-Z	a-z	z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	115	V
Gate-Source Voltage		V_{GSS}	±5.5	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	T_A = +25°C T_A = +70°C	I_D	3.5 2.8	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	26	A
Maximum Body Diode Continuous Current (Note 6)		I_S	3.5	A
Pulsed Body Diode Continuous Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	26	A
Avalanche Current, L = 0.3mH (Note 7)		I_{AS}	10	A
Avalanche Energy, L = 0.3mH (Note 7)		E_{AS}	15	mJ

ESD Ratings (Note 11)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	2000	V	1C
Electrostatic Discharge - Machine Model	ESD MM	200	V	M2

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 8)	P_D	1.1	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 8)	$R_{\theta JA}$	115	°C/W
Power Dissipation (Note 6)	P_D	1.9	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{\theta JA}$	65	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	115	—	—	V	V_{GS} = 0V, I_D = 10mA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 92V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±50	µA	V_{GS} = ±8V, V_{DS} = 0V
		—	—	±10	µA	V_{GS} = ±5.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.4	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	56	85	mΩ	V_{GS} = 4.5V, I_D = 3A
		—	61	90		V_{GS} = 2.5V, I_D = 2A
		—	75	130		V_{GS} = 1.5V, I_D = 50mA
Diode Forward Voltage	V_{SD}	—	0.7	1.0	V	V_{GS} = 0V, I_S = 1A
Reverse-Recovery Charge	Q_{RR}	—	53	—	nC	I_F = 4.5A, di/dt = 300A/µs
Reverse-Recovery Time	t_{RR}	—	30	—	ns	
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	560	—	pF	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	80	—		
Reverse Transfer Capacitance	C_{rss}	—	9.5	—		
Series Gate Resistance	R_g	—	4.4	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	8	—	nC	V_{DS} = 50V, I_D = 4.5A V_{GS} = 5V
Gate-Source Charge	Q_{gs}	—	1	—		
Gate-Drain Charge	Q_{gd}	—	2.4	—		
Gate Charge at V_{TH}	$Q_{g(TH)}$	—	0.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	2	—	ns	V_{DS} = 50V, R_L = 11Ω V_{GS} = 5V, R_{GEN} = 3Ω
Turn-On Rise Time	t_R	—	8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	29	—		
Turn-Off Fall Time	t_F	—	11	—		

Notes:
6. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.
7. Repetitive rating, pulse width limited by junction temperature.
8. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to production testing.
11. Refer to ANSI/ESDA/JEDEC specifications JS-001-2017 and AEC-Q100-003-Rev-E.

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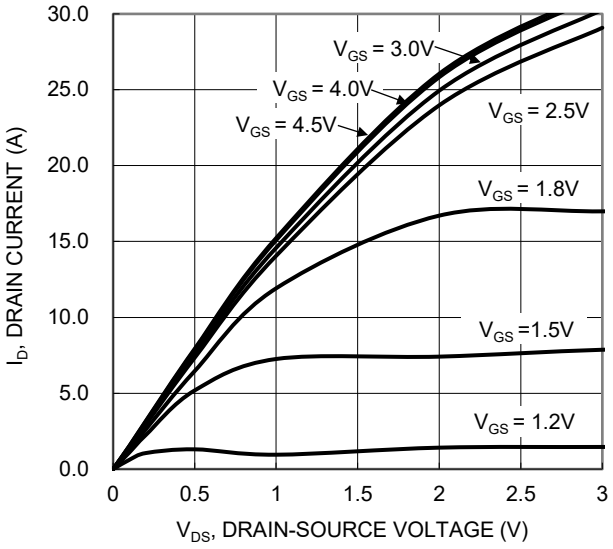


Figure 1. Typical Output Characteristic

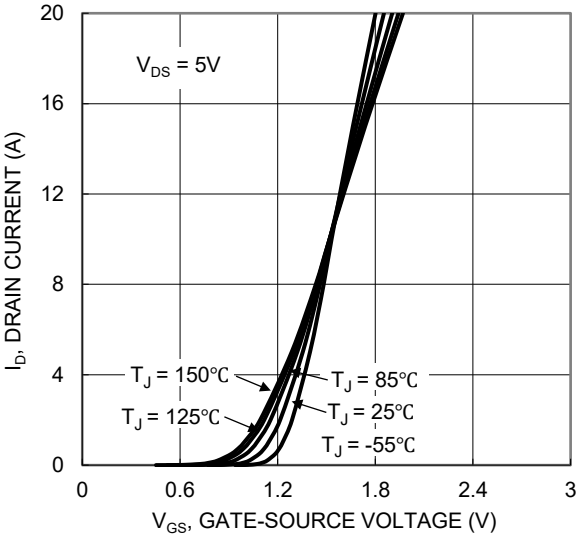


Figure 2. Typical Transfer Characteristic

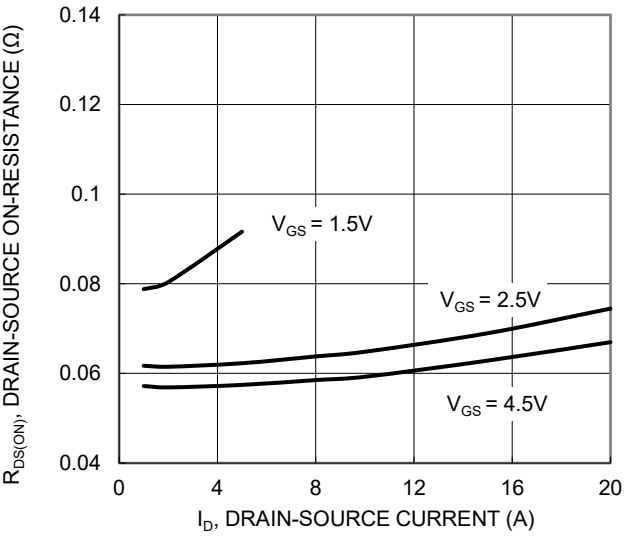


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

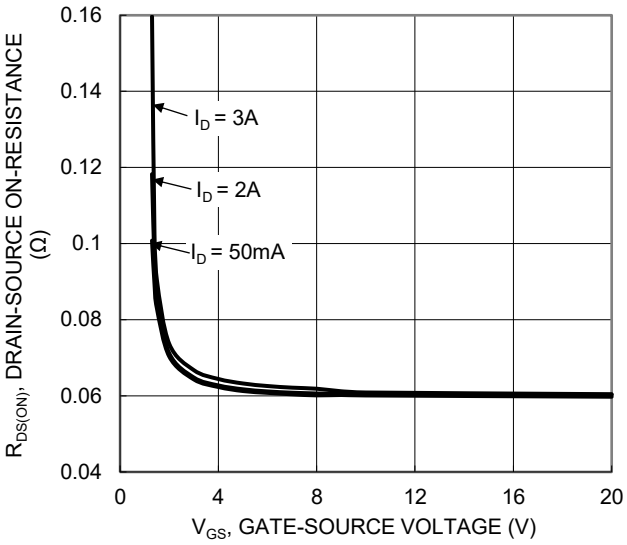


Figure 4. Typical Transfer Characteristic

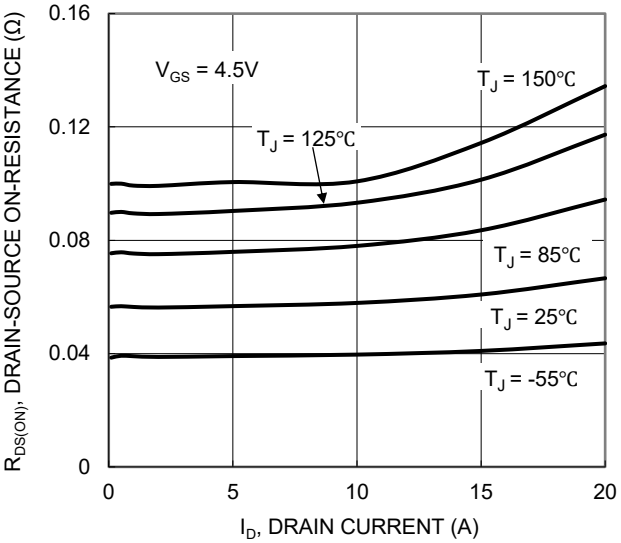


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

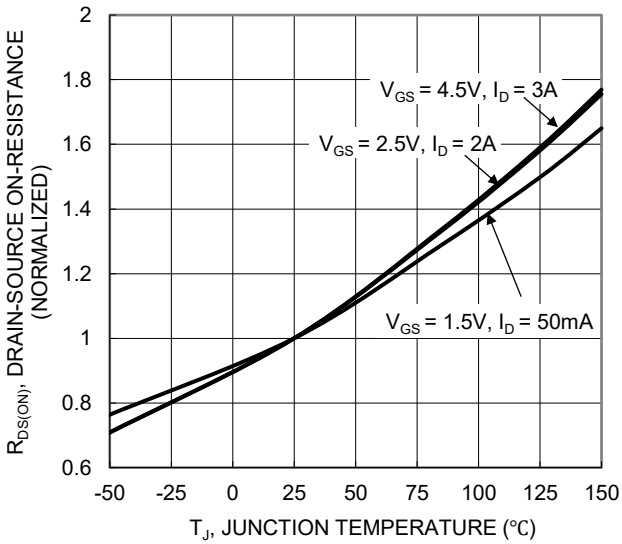


Figure 6. On-Resistance Variation with Temperature

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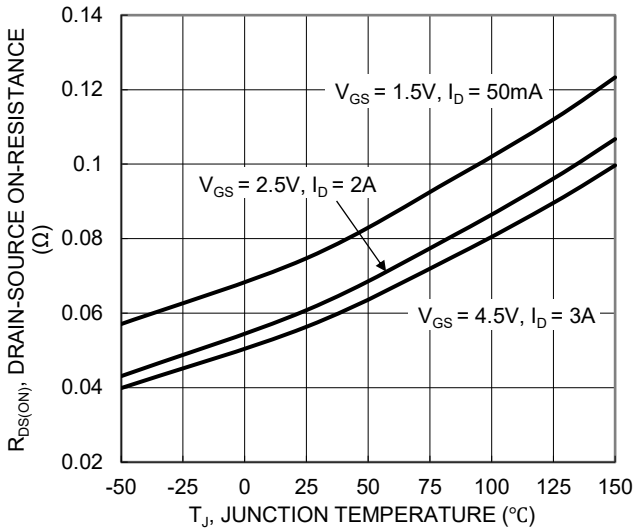


Figure 7. On-Resistance Variation with Temperature

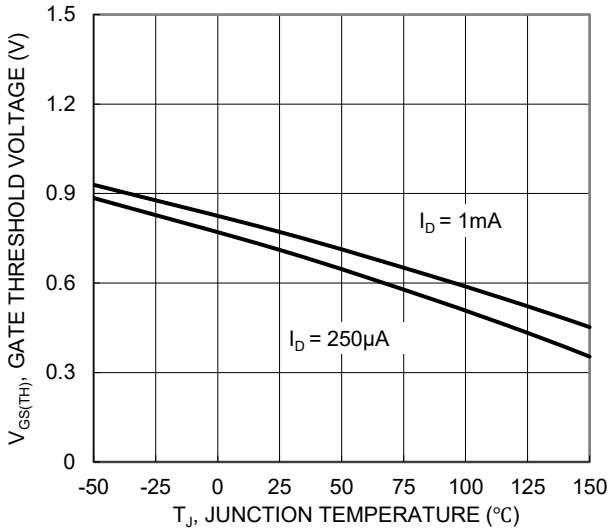


Figure 8. Gate Threshold Variation vs. Junction Temperature

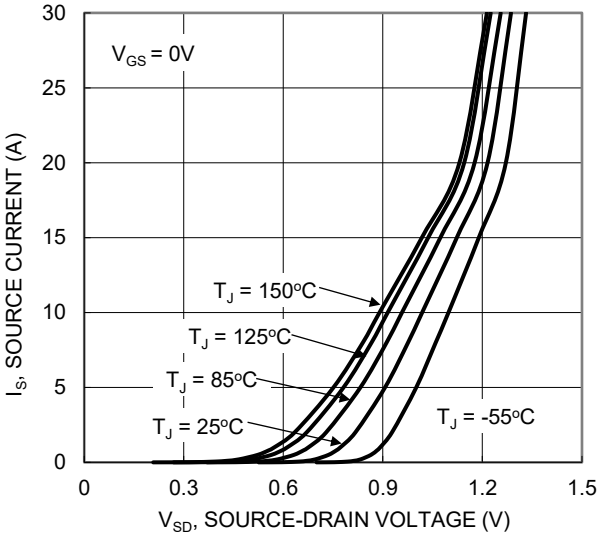


Figure 9. Diode Forward Voltage vs. Current

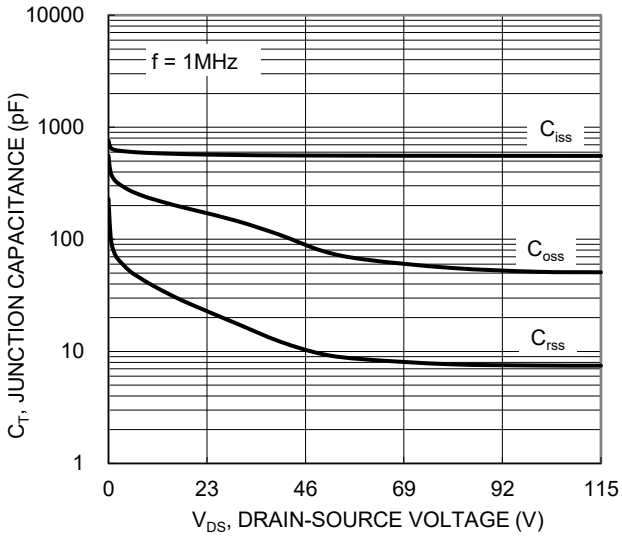


Figure 10. Typical Junction Capacitance

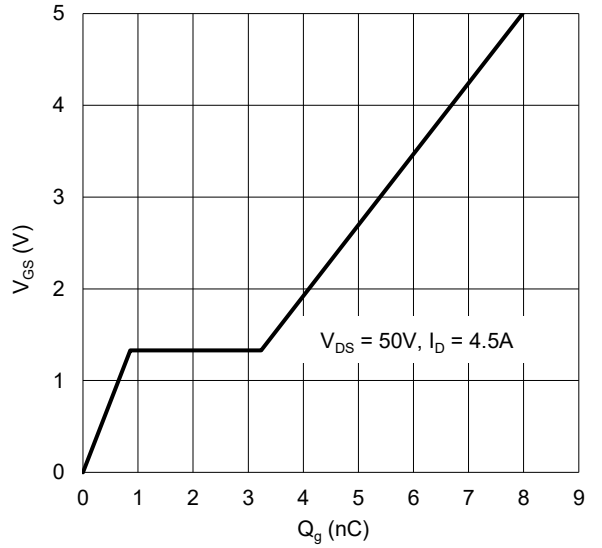


Figure 11. Gate Charge

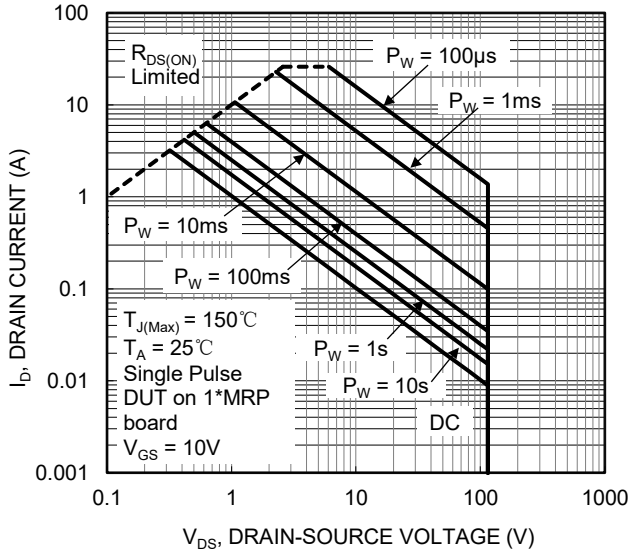


Figure 12. SOA, Safe Operation Area

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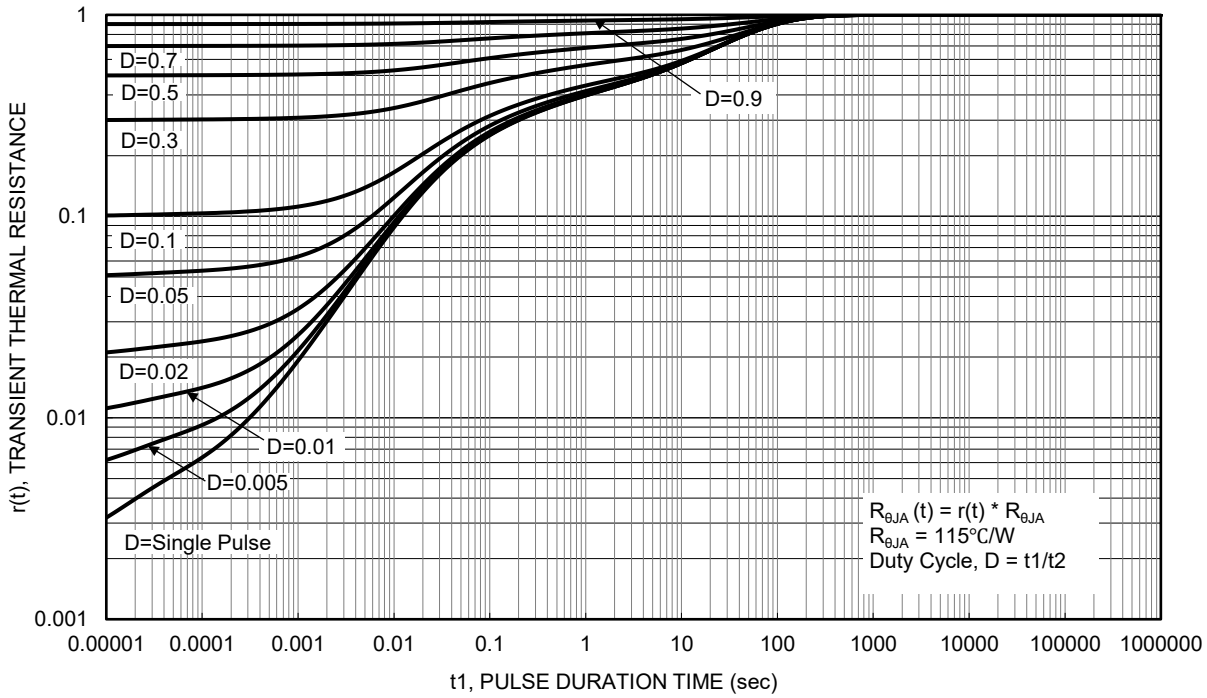


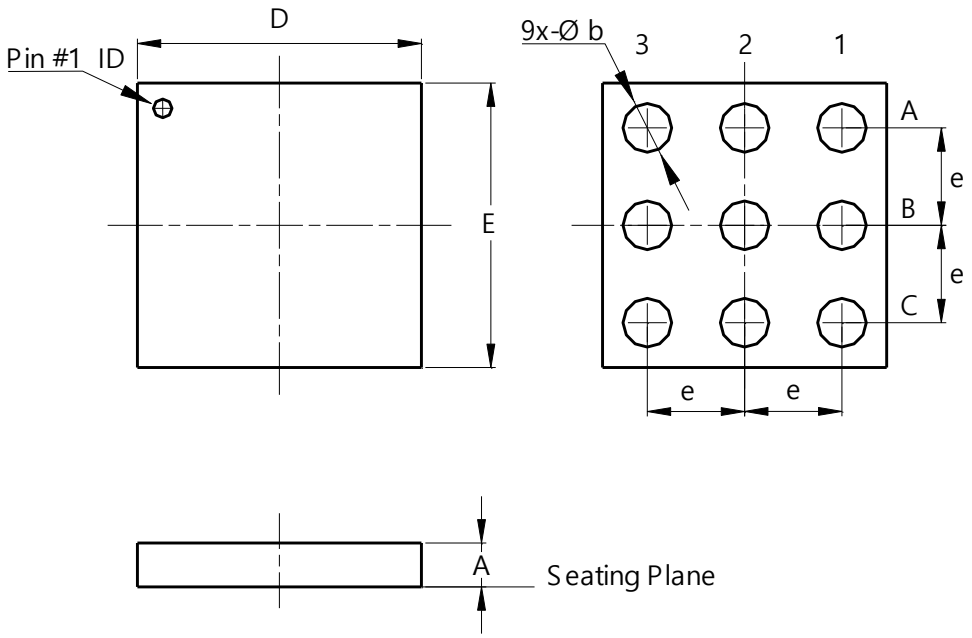
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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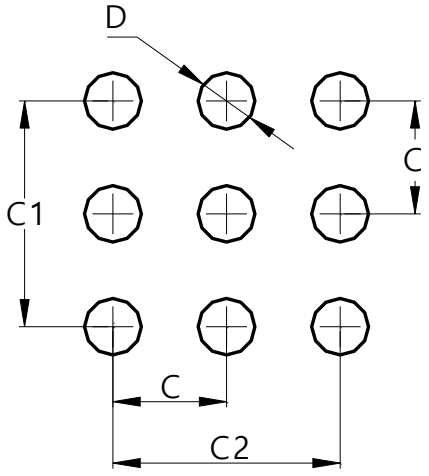


X4-DSN1515-9			
Dim	**Min**	**Max**	**Typ**
A	0.17	0.25	0.225
b	0.21	0.29	0.25
D	1.420	1.50	1.46
E	1.420	1.50	1.46
e	--	--	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN1515-9



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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